# Renesas Electronics America Inc - UPD70F3778GF-GAT-AX Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | V850ES |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB |
| Peripherals | DMA, LVD, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 76K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.85V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3778gf-gat-ax |

### 4.3.2 Port 2

Port 2 is a 7-bit (V850ES/JH3-E)/8-bit (V850ES/JJ3-E) port for which I/O settings can be controlled in 1-bit units.

Port 2 includes the following alternate-function pins.

**Table 4-7. Port 2 Alternate-Function Pins**

| Pin Name | Pin No. | | Alternate-Function Pin Name | I/O | Remark |
|---|---|---|---|---|---|
| | V850ES/JH3-E | V850ES/JJ3-E | | | |
| P20 | 38 | 38 | TIAB02/TOAB02/INTP01 | I/O | Can be specified as an N-ch open-drain output |
| P21 | 39 | 39 | TIAB00/TOAB00/RTCDIV/RTCCL | I/O | |
| P22 | 40 | 40 | TIAB01/TOAB01/RTC1HZ/INTP02 | I/O | |
| P23 | 59 | 65 | SIF1/TXDC1/SDA00/INTP03 | I/O | |
| P24 | 62 | 68 | SOF1/RXDC1/SCL00/INTP04 | Input | |
| P25 | 63 | 69 | $\overline{\text{SCKF1}}$/TIAA30/TOAA30/$\overline{\text{UDMARQ0}}$ | I/O | |
| P26 | 64 | 70 | TIAA31/TOAA31/INTP05/$\overline{\text{UDMAAK0}}$ | I/O | |
| P27 | – | 41 | TIAB03/TOAB03/INTP21 | I/O | |

**Caution The P20 to P27 pins have hysteresis characteristics in the input mode of the alternate-function pin, but do not have the hysteresis characteristics in the port mode.**

#### (1) Port 2 register (P2)

**(a) V850ES/JH3-E**

After reset: 00H (output latch) R/W Address: FFFFF404H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| P2 | 0 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |

| P2n | Output data control (in output mode) (n = 0 to 6) |
|---|---|
| 0 | Outputs 0. |
| 1 | Outputs 1. |

**(b) V850ES/JJ3-E**

After reset: 00H (output latch) R/W Address: FFFFF404H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| P2 | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 |

| P2n | Output data control (in output mode) (n = 0 to 7) |
|---|---|
| 0 | Outputs 0. |
| 1 | Outputs 1. |

After reset: 03H R/W Address: FFFFF828H

| | 7 | <6> | 5 | <4> | <3> | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PCC | FRC | MCK | MFRC | CLS[Note] | CK3 | CK2 | CK1 | CK0 |

| FRC | Use of subclock on-chip feedback resistor |
|---|---|
| 0 | Used |
| 1 | Not used |

| MCK | Main clock oscillator control |
|---|---|
| 0 | Oscillation enabled |
| 1 | Oscillation stopped |

- Even if the MCK bit is set (1) while the system is operating with the main clock as the CPU clock, the operation of the main clock does not stop. It stops after the CPU clock has been changed to the subclock.
- Before setting the MCK bit from 0 to 1, stop the on-chip peripheral functions operating with the main clock.
- When the main clock is stopped and the device is operating with the subclock, clear (0) the MCK bit and secure the oscillation stabilization time by software before switching the CPU clock to the main clock or operating the on-chip peripheral functions.

| MFRC | Use of main clock on-chip feedback resistor |
|---|---|
| 0 | Used |
| 1 | Not used |

| CLS[Note] | Status of CPU clock ($f_{CPU}$) |
|---|---|
| 0 | Main clock operation |
| 1 | Subclock operation |

| CK3 | CK2 | CK1 | CK0 | Clock selection ($f_{CLK}/f_{CPU}$) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $f_{XX}$ |
| 0 | 0 | 0 | 1 | $f_{XX}/2$ |
| 0 | 0 | 1 | 0 | $f_{XX}/4$ |
| 0 | 0 | 1 | 1 | $f_{XX}/8$ |
| 0 | 1 | 0 | 0 | $f_{XX}/16$ |
| 0 | 1 | 0 | 1 | $f_{XX}/32$ |
| 0 | 1 | 1 | × | Setting prohibited |
| 1 | × | × | × | $f_{XT}$ |

**Note** The CLS bit is a read-only bit.

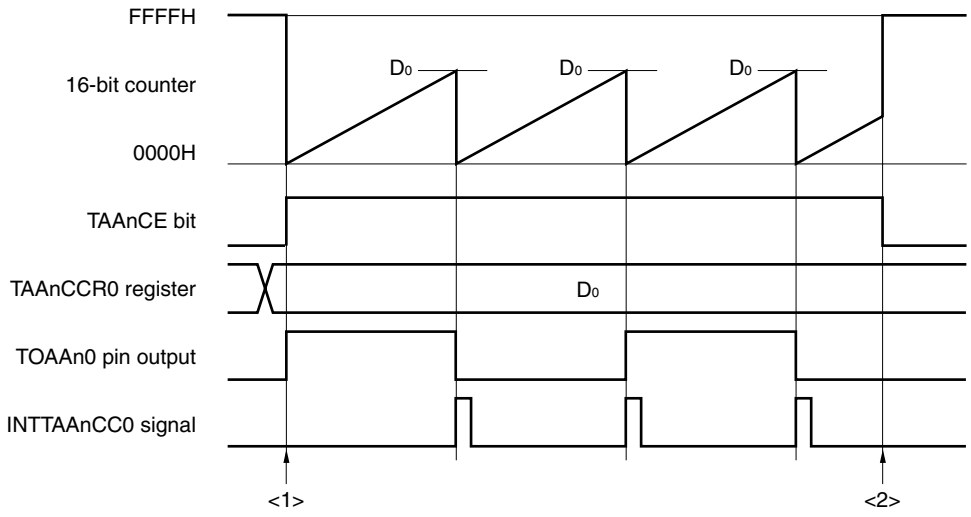
**Cautions 1. Do not change the CPU clock (by using the CK3 to CK0 bits) while CLKOUT is being output.**

**2. Use a bit manipulation instruction to manipulate the CK3 bit. When using an 8-bit manipulation instruction, do not change the set values of the CK2 to CK0 bits.**

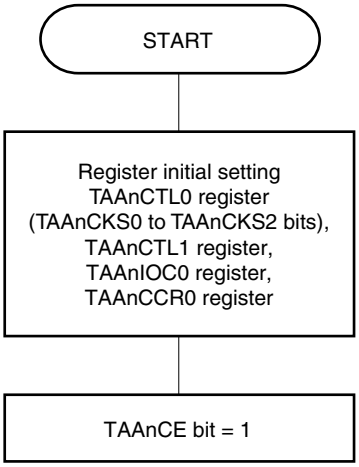
**Remark** ×: don't care

### (1) Interval timer mode operation flow

**Figure 7-10. Software Processing Flow in Interval Timer Mode**



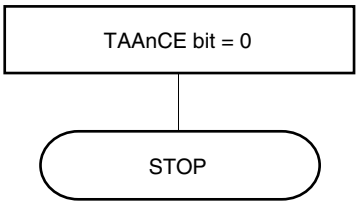

<1> Count operation start flow




Initial setting of these registers is performed before setting the TAAnCE bit to 1.

The TAAnCKS0 to TAAnCKS2 bits can be set at the same time when counting has been started (TAAnCE bit = 1).

<2> Count operation stop flow



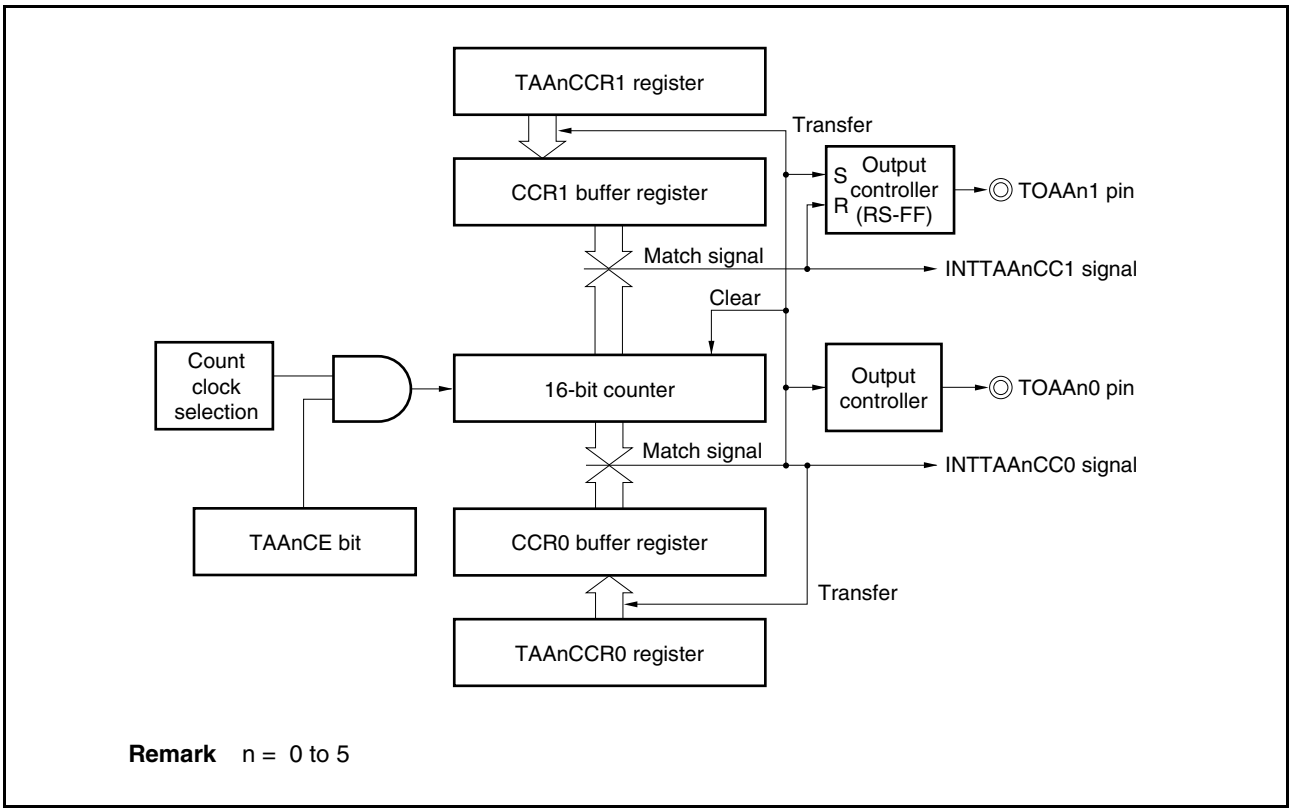

The counter is initialized and counting is stopped by clearing the TAAnCE bit to 0.

**Remark** n = 0 to 5

### 7.5.5 PWM output mode (TAAnMD2 to TAAnMD0 bits = 100)

In the PWM output mode, a PWM waveform is output from the TOAAn1 pin when the TAAnCTL0.TAAnCE bit is set to 1. In addition, a pulse with one cycle of the PWM waveform as half its cycle is output from the TOAAn0 pin.

**Figure 7-29. Configuration in PWM Output Mode**




**Remark** n = 0 to 5

(2/2)

| TT0EOF | Overflow detection flag for TMT0 encoder function |
|---|---|
| Set (1) | Overflow occurs. |
| Reset (0) | Cleared by writing 0 to the TT0EOF bit or when the TT0CTL0.TT0CE bit = 0 |

- The TT0EOF bit is set to 1 when the 16-bit counter overflows from FFFFH to 0000H in the encoder compare mode.
- As soon as the TT0EOF bit has been set to 1, an overflow interrupt request signal (INTTTOV0) is generated. At this time, the TT0OPT0.TT0OVF bit is not set to 1.
- The TT0EOF bit is not cleared to 0 even if the TT0EOF bit or TT0OPT1 register is read when the TT0EOF bit = 1.
- The status of the TT0EOF bit is retained even if the TT0CTL0.TT0CE bit is cleared to 0 when the TT0CTL2.TT0ECC bit = 1.
- Before clearing the TT0EOF bit to 0 after the INTTTOV0 signal is generated, be sure to confirm (read) that the TT0EOF bit is set to 1.
- The TT0EOF bit can be read or written, but it cannot be set to 1 by software. Writing 1 to this bit does not affect the operation of TMT0.

| TT0ESF | TMT0 count-up/-down operation status detection flag |
|---|---|
| 0 | TMT0 is counting up. |
| 1 | TMT0 is counting down. |

- This bit is cleared to 0 if the TT0CTL0.TT0CE bit = 0 when the TT0CTL2.TT0ECC bit = 0.
- The status of the TT0ESF bit is retained even if the TT0CE bit = 0 when the TT0ECC bit = 1.

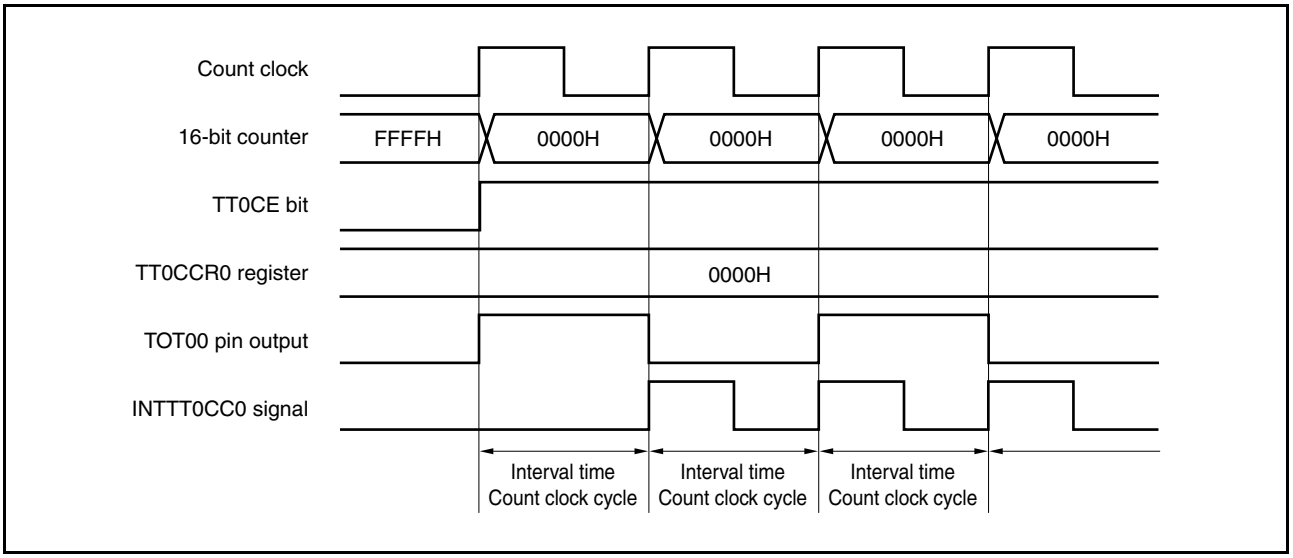
**Caution Be sure to set bits 3 to 7 to “0”.**

### (2) Interval timer mode operation timing

#### (a) Operation if TT0CCR0 register is set to 0000H

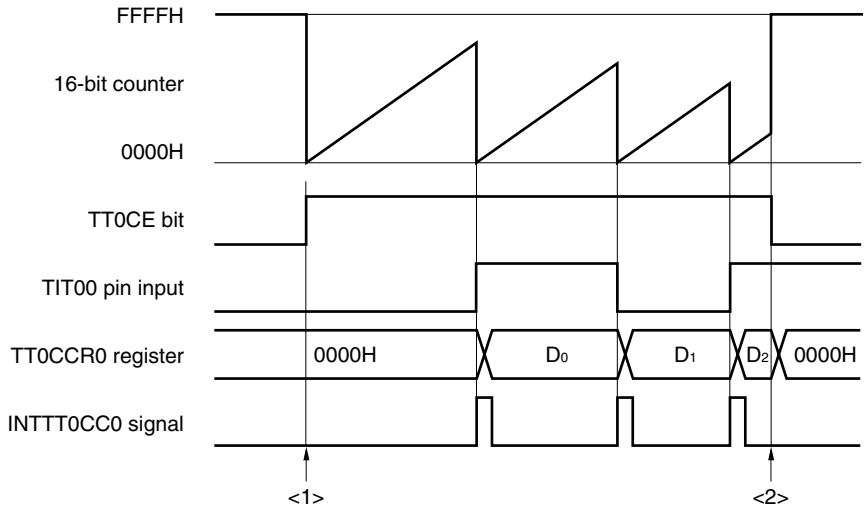
If the TT0CCR0 register is set to 0000H, the INTTT0CC0 signal is generated at each count clock, and the output of the TOT00 pin is inverted.

The value of the 16-bit counter is always 0000H.

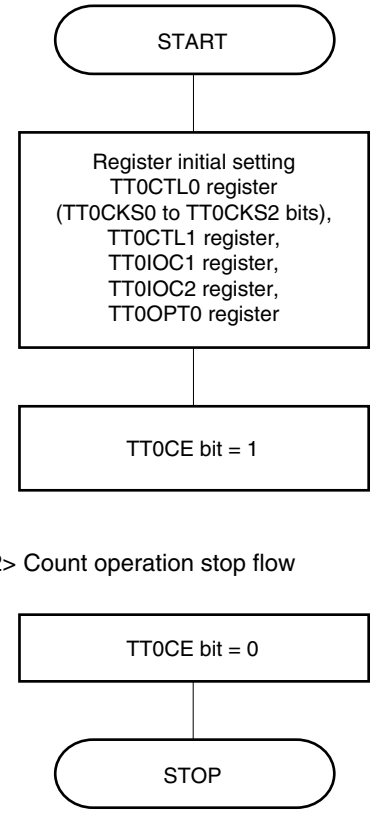


**(1) Operation flow in pulse width measurement mode**

**Figure 9-42. Software Processing Flow in Pulse Width Measurement Mode**




<1> Count operation start flow




Initial setting of these registers is performed before setting the TT0CE bit to 1.

The TT0CKS0 to TT0CKS2 bits can be set at the same time as when counting starts (TT0CE bit = 1).

<2> Count operation stop flow



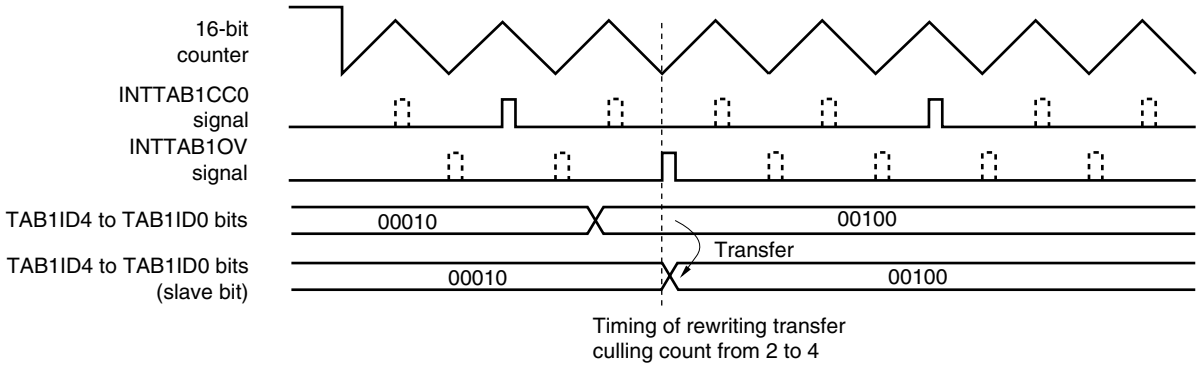

The counter is initialized and counting is stopped by clearing the TT0CE bit to 0.

**(2) To alternately output crest interrupt (INTTAB1CC0) and valley interrupt (INTTAB1OV)**

To alternately output the crest and valley interrupts, set both the TAB1OPT1.TAB1ICE and TAB1OPT1.TAB1IOE bits to 1.

**Figure 11-18. Crest/Valley Interrupt Output**

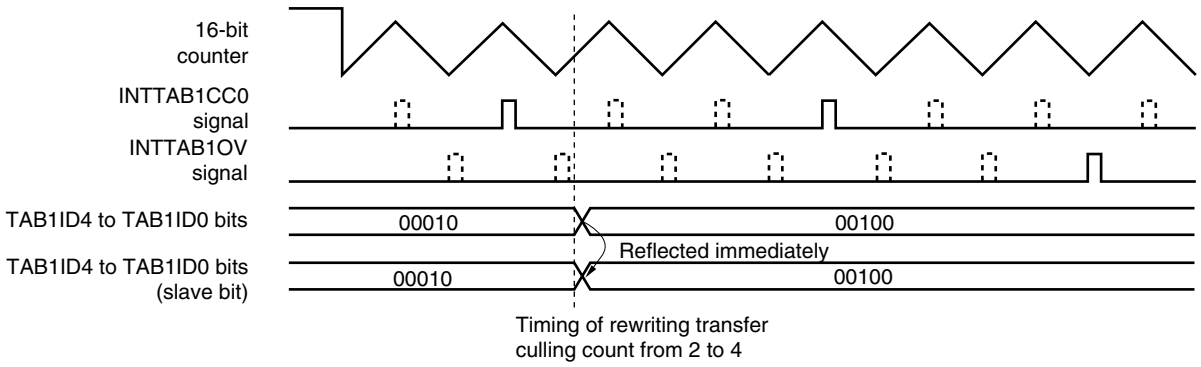
**(a) TAB1OPT0.TAB1CMS bit = 0, TAB1OPT2.TAB1RDE bit = 1 (with transfer culling control)**




**Remarks 1.** Transfer is performed at the culled interrupt output timing. The other transfer timing is ignored.

**2.** : Culled interrupt

**(b) TAB1CMS bit = 1, TAB1RDE bit = 0 or 1 (without transfer control)**




**Remarks 1.** Rewriting is reflected immediately. The transfer timing is ignored.

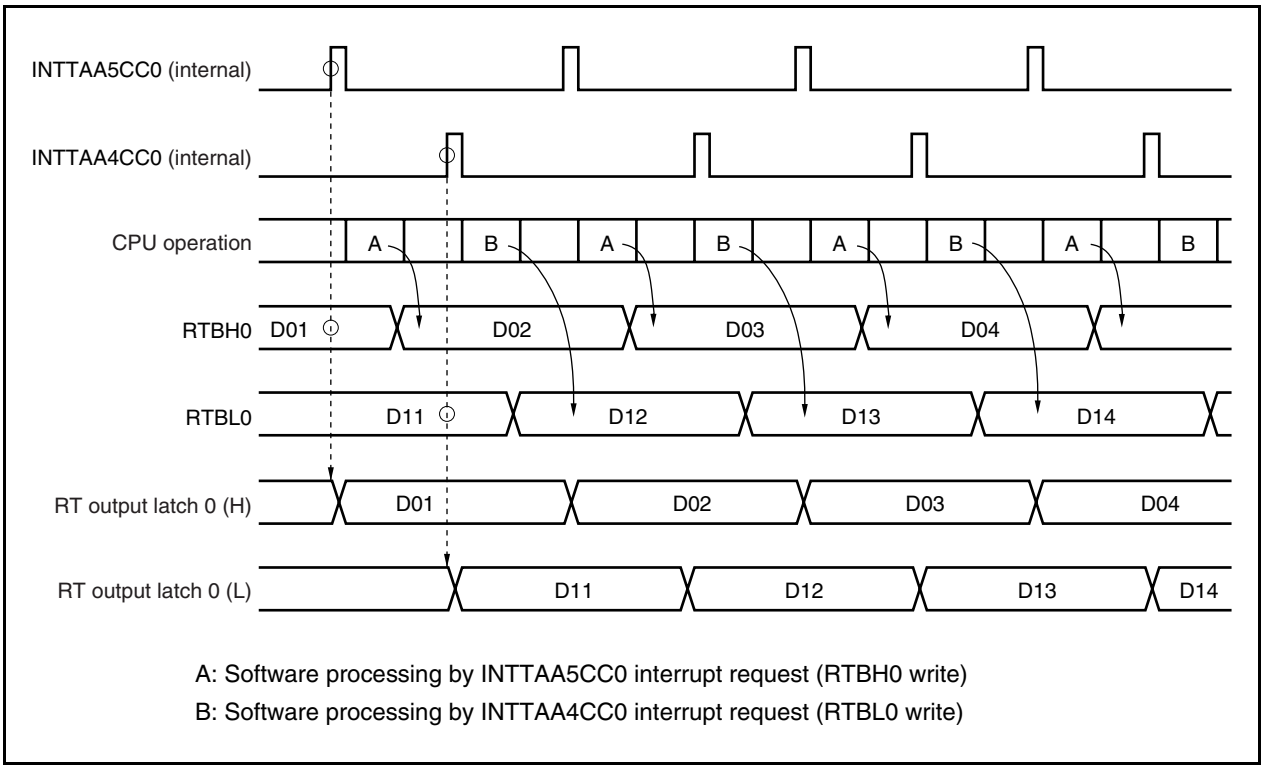
**2.** : Culled interrupt

## 14.4 Operation

If the real-time output operation is enabled by setting the RTPC0.RTPOE0 bit to 1, the data of the RTBH0 and RTBL0 registers is transferred to the real-time output latch in synchronization with the generation of the selected transfer trigger (set by the RTPC0.EXTR0 and RTPC0.BYTE0 bits). Of the transferred data, only the data of the bits for which real-time output is enabled by the RTPM0 register is output from the RTP00 to RTP07 bits. The bits for which real-time output is disabled by the RTPM0 register output 0.

If the real-time output operation is disabled by clearing the RTPOE0 bit to 0, the RTP00 to RTP07 signals output 0 regardless of the setting of the RTPM0 register.

**Figure 14-2. Example of Operation Timing of RTO0 (When EXTR0 Bit = 0, BYTE0 Bit = 0)**




**Remark** For the operation during standby, see **CHAPTER 27 STANDBY FUNCTION**.

**(2) Reception end interrupt request signal (INTUBnTIR)**

**(a) Single mode**

When reception is enabled, a reception end interrupt request signal is generated if data is shifted into the receive shift register and stored in the UBnRX register (if the receive data can be read).
When reception is disabled, no reception end interrupt request signal is generated.

**(b) FIFO mode**

When reception is enabled, a reception end interrupt request signal is generated if data is shifted into the receive shift register and receive data of the number set as the trigger by the UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits is transferred to receive FIFO (if receive data of the specified number can be read).
When reception is disabled, no reception end interrupt request signal is generated.

**(3) Transmission enable interrupt request signal (INTUBnTIT)**

**(a) Single mode**

The transmission enable interrupt request signal is generated if transmit data of one frame, including 7 or 8 bits of characters, is shifted out from the transmit shift register and the UBnTX register becomes empty (if transmit data can be written).

**(b) FIFO mode**

The transmission enable interrupt request signal is generated if transmit data of the number set as the trigger by the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits is transferred to the transmit shift register from transmit FIFO (if transmit data of the specified number can be written).

**(4) FIFO transmission end interrupt request signal (INTUBnTIF)**

**(a) Single mode**

Cannot be used.

**(b) FIFO mode**

The FIFO transmission end interrupt request signal is generated when no more data is in transmit FIFO and the transmit shift register (when the FIFO and register become empty). After the FIFO transmission end interrupt request signal has occurred, clear the interrupt request signal (INTUBnTIT) held pending in the pending mode (UBnFIC0.UBnITM bit = 0) by clearing the FIFO (UBnFIC0.UBnTFC bit = 1).

**Caution If the FIFO transmission end interrupt request signal is generated (all transmit data are not transmitted) because writing the next transmit data to transmit FIFO is delayed, do not clear the FIFO.**

### 19.3.4 Mode switching between CSIF3 and UARTB1

In the V850ES/JH3-E and V850ES/JJ3-E, CSIF3 and UARTB1 share the same pin and therefore cannot be used simultaneously. Set CSIF3 and UARTB1 in advance, using the PMC9, PFC9, and PFCE9 registers, before use.

**Caution The transmit/receive operation of CSIF3 and UARTB1 is not guaranteed if these functions are switched during transmission or reception. Be sure to disable the one that is not used.**

**Figure 19-5. CSIF3 and UARTB1 Mode Switch Settings**

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| PMC9 (PMC9H) | PMC915 | PMC914 | PMC913 | PMC912 | PMC911 | PMC910 | PMC99 | PMC98 |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| (PMC9L) | PMC97 | PMC96 | PMC95 | PMC94 | PMC93 | PMC92 | PMC91 | PMC90 |

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| PFC9 (PFC9H) | PFC915 | PFC914 | PFC913 | PFC912 | PFC911 | PFC910 | PFC99 | PFC98 |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| (PFC9L) | PFC97 | PFC96 | PFC95 | PFC94 | PFC93 | PFC92 | PFC91 | PFC90 |

After reset: 0000H R/W Address: PFCE9 FFFFF712H,
PFCE9L FFFFF712H, PFCE9H FFFFF713H

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| PFCE9 (PFCE9H) | PFCE915 | PFCE914 | PFCE913 | 0 | PFCE911 | PFCE910 | PFCE99 | PFCE98 |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| (PFCE9L) | PFCE97 | PFCE96 | PFCE95 | PFCE94 | PFCE93 | PFCE92 | PFCE91 | PFCE90 |

| PMC915 | PFCE915 | PFC915 | Operation mode |
|---|---|---|---|
| 0 | × | × | Port I/O mode |
| 1 | 0 | 0 | $\overline{\text{SCKF3}}$ (CSIF3) |

| PMC914 | PFCE914 | PFC914 | Operation mode |
|---|---|---|---|
| 0 | × | × | Port I/O mode |
| 1 | 0 | 0 | SOF3 (CSIF3) |
| 1 | 0 | 1 | RXDB1 (UARTB1) |

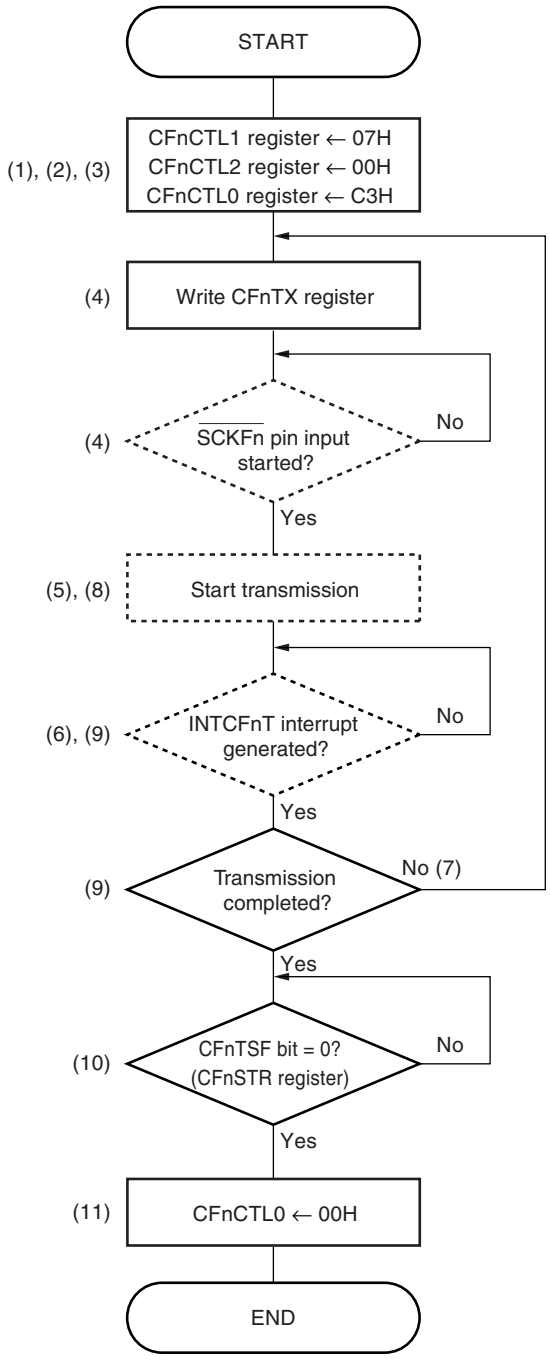
| PMC913 | PFCE913 | PFC913 | Operation mode |
|---|---|---|---|
| 0 | × | × | Port I/O mode |
| 1 | 0 | 0 | SIF3 (CSIF3) |
| 1 | 0 | 1 | TXDB1 (UARTB1) |

**Remark** × = don't care

### 19.6.10 Continuous transfer mode (slave mode, transmission mode)

MSB first (CFnCTL0.CFnDIR bit = 0), communication type 1 (CFnCTL1.CFnCKP and CFnCTL1.CFnDAP bits = 00), communication clock ($f_{CCLK}$) = external clock ($\overline{SCKFn}$) (CFnCTL1.CFnCKS2 to CFnCTL1.CFnCKS0 bits = 111), transfer data length = 8 bits (CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits = 0000)

#### (1) Operation flow




**Remarks 1.** The broken lines indicate the hardware processing.

**2.** The numbers in this figure correspond to the processing numbers in **(2) Operation timing**.

**3.** n = 0 to 4 (V850ES/JH3-E)
n = 0 to 6 (V850ES/JJ3-E)

**(7) IIC division clock select registers 0 to 2 (OCKS0 to OCKS2)**

The OCKSm registers control the I²C0n division clock.

These registers control the I²C00 division clock via the OCKS0 register, the I²C01 and I²C02 division clocks via the OCKS1 register, and the I²C03 and I²C04 division clocks via the OCKS2 register.

These registers can be read or written in 8-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: OCKS0 FFFFF340H, OCKS1 FFFFF344H, OCKS2 FFFFF348H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| OCKSm | 0 | 0 | 0 | OCKSENm | OCKSTHm | 0 | OCKSm1 | OCKSm0 |

(m = 0 to 2)

| OCKSENm | Operation setting of I²Cn division clock |
|---|---|
| 0 | Stops I²Cn division clock operation |
| 1 | Enables I²Cn division clock operation |

| OCKSTHm | OCKSm1 | OCKSm0 | Selection of I²Cn division clock |
|---|---|---|---|
| 0 | 0 | 0 | $f_{XX}$/4 |
| 0 | 0 | 1 | $f_{XX}$/6 |
| 0 | 1 | 0 | $f_{XX}$/8 |
| 0 | 1 | 1 | $f_{XX}$/10 |
| 1 | 0 | 0 | $f_{XX}$/2 |

**Remark** n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

**(8) IIC shift registers n (IICn)**

The IICn registers are used for serial transmission/reception (shift operations) synchronized with the serial clock. These registers can be read or written in 8-bit units, but data should not be written to the IICn registers during a data transfer.

Access (read/write) the IICn registers only during the wait period. Accessing these registers in communication states other than the wait period is prohibited. However, for the master device, the IICn registers can be written once only after the transmission trigger bit (IICCn.STTn bit) has been set to 1.

A wait state is released by writing the IICn registers during the wait period, and data transfer is started.

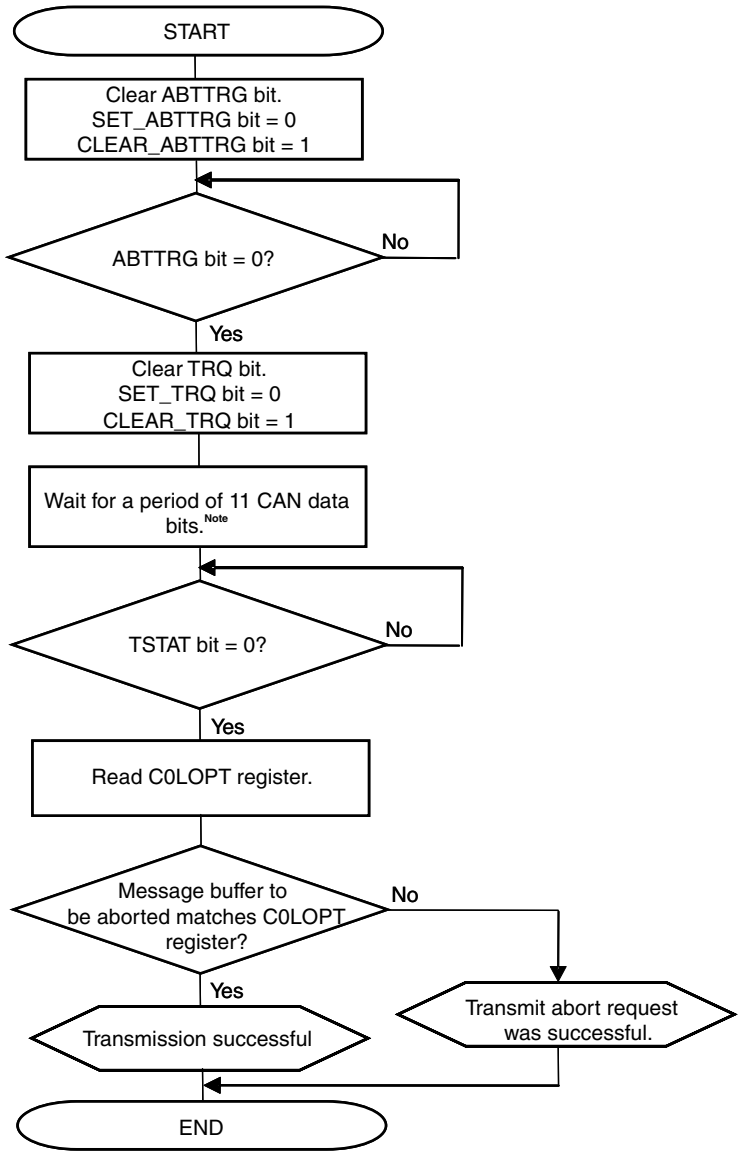
Reset sets these registers to 00H.

After reset: 00H R/W Address: IIC0 FFFFFD80H, IIC1 FFFFFD90H, IIC2 FFFFFDA0H, IIC3 FFFFFDB0H, IIC4 FFFFFBC0H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| IICn | | | | | | | | |

**Remark** n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

**Figure 21-47. Transmission Abort Processing Except for ABT Transmission (Normal Operation Mode with ABT)**




**Note** During a period of a total of 11 bits, 3 bits of interframe space and 8 bits of suspend transmission, the transmission request may have already been acknowledged by the protocol layer. Consequently, transmission may not be aborted but started even if the TRQ bit is cleared.

**Cautions 1. Execute transmission abort processing by clearing the TRQ bit, not the RDY bit.**

**2. Before making a sleep mode transition request, confirm that there is no transmission request left using this processing.**

**3. The TSTAT bit can be periodically checked by a user application or can be checked after the transmit completion interrupt.**

**4. Do not execute a new transmission request including in the other message buffers while transmission abort processing is in progress.**

**5. If data of the same message buffer are successively transmitted or if only one message buffer is used, judgments whether transmission has been successfully executed or failed may contradict. In such a case, make a judgment by using the history information of the C0TGPT register.**

**(g) SET_CONFIGURATION() request**

If any of wValue, wIndex, or wLength is other than the values shown in Table 22-3, a STALL response is made in the status stage.

- Default state: The CONF bit of the UF0 mode status register (UF0MODS) and the UF0 configuration register (UF0CNF) are set to 1 if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the CONF bit of the UF0MODS register and UF0CNF register are cleared to 0. In other words, the device skips the Addressed state and moves to the Configured state in which it responds to the Default address.
- Addressed state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device enters the Configured state if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the device remains in the Addressed state.
- Configured state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device returns to the Addressed state if the specified configuration value is 0 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 1, the device remains in the Configured state.

If the SET_CONFIGURATION() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) is set to 1, and an interrupt is issued. All Halt Features are cleared after the SET_CONFIGURATION() request has been completed even if the specified configuration value is the same as the current configuration value. If the SET_CONFIGURATION() request has been correctly processed, the data toggle of all endpoints is always initialized to DATA0 again (it is defined that the default status, Alternative Setting 0, is set from when the SET_CONFIGURATION request is received to when the SET_INTERFACE request is received).

**(h) SET_FEATURE() request**

A STALL response is made in the status stage if the SET_FEATURE() request is for a Feature that cannot be set or does not exist, or if the target is an interface or an endpoint that does not exist. A STALL response is also made if the wLength value is other than 0.

- Default state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Addressed state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Configured state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or an endpoint that exists; otherwise a STALL response is made in the status stage.

When the SET_FEATURE() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) and the EnHALT bit of the UF0 EPn status register L (UF0EnSL) are set to 1, and an interrupt is issued (n = 0 to 4, 7).

### (3) IPGT: Back-to-back IPG register

Access This register can be read and written in 32-bit units.

Address 002E 0008H

Default value 0000 0013H. This register is cleared to its default value by all types of resets.

**Caution Be sure to set bits 31 to 7 to "0".**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R | R | R | R | R | R |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R | R | R | R | R | R |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R | R | R | R | R | R | R | R |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | IPGT | | | | | | |
| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Name | Description |
|---|---|---|
| 6 to 0 | IPGT | IPG in back-to-back transmission:<br>These bits set the gap between packets (or an inter-packet gap (IPG)) in back-to-back transmission. The expression used to calculate IPG is as follows.<br>• IPG = (5 + IPGT) x time required to transmit 4 bits<br>(Time required to transmit 1 bit = 100 ns when the data rate is 10 Mbps or 10 ns when the data rate is 100 Mbps)<br>Set IPG to the time required to transmit at least 96 bits to satisfy the specification of IEEE802.3 (refer to **23.5.2 (5) Inter-packet gap (IPG)**). |

**(24) TBYT: Transmit byte counter**

Access This register can be read and written in 32-bit units.

Address 002E 01C0H

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| TBYT31 | TBYT30 | TBYT29 | TBYT28 | TBYT27 | TBYT26 | TBYT25 | TBYT24 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBYT23 | TBYT22 | TBYT21 | TBYT20 | TBYT19 | TBYT18 | TBYT17 | TBYT16 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBYT15 | TBYT14 | TBYT13 | TBYT12 | TBYT11 | TBYT10 | TBYT9 | TBYT8 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBYT7 | TBYT6 | TBYT5 | TBYT4 | TBYT3 | TBYT2 | TBYT1 | TBYT0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Name | Description |
|---|---|---|
| 31 to 0 | TBYT[31:0] | This counter indicates the number of bytes in a transmit packet. When a collision occurs before transmission is completed or aborted, the byte at which the collision occurred is also counted. The preamble and SFD are not included in the byte count indication. |

### 33.4.6 Pin connection

When performing on-board writing, mount a connector on the target system to connect to the dedicated flash programmer. Also, incorporate a function on-board to switch from the normal operation mode to the flash memory programming mode.

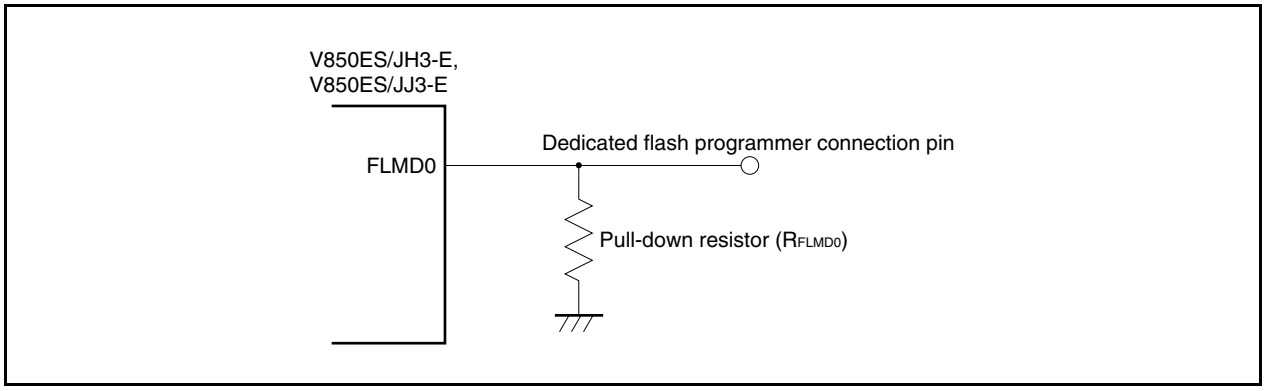
In the flash memory programming mode, all the pins not used for flash memory programming become the same status as that immediately after reset. Therefore, pin handling is required when the external device does not acknowledge the status immediately after a reset.

**(1) FLMD0 pin**

In the normal operation mode, input a voltage of $V_{SS}$ level to the FLMD0 pin. In the flash memory programming mode, supply a write voltage of $V_{DD}$ level to the FLMD0 pin.

Because the FLMD0 pin serves as a write protection pin in the self programming mode, a voltage of $V_{DD}$ level must be supplied to the FLMD0 pin via port control, etc., before writing to the flash memory. For details, see **33.5.5 (1) FLMD0 pin**.

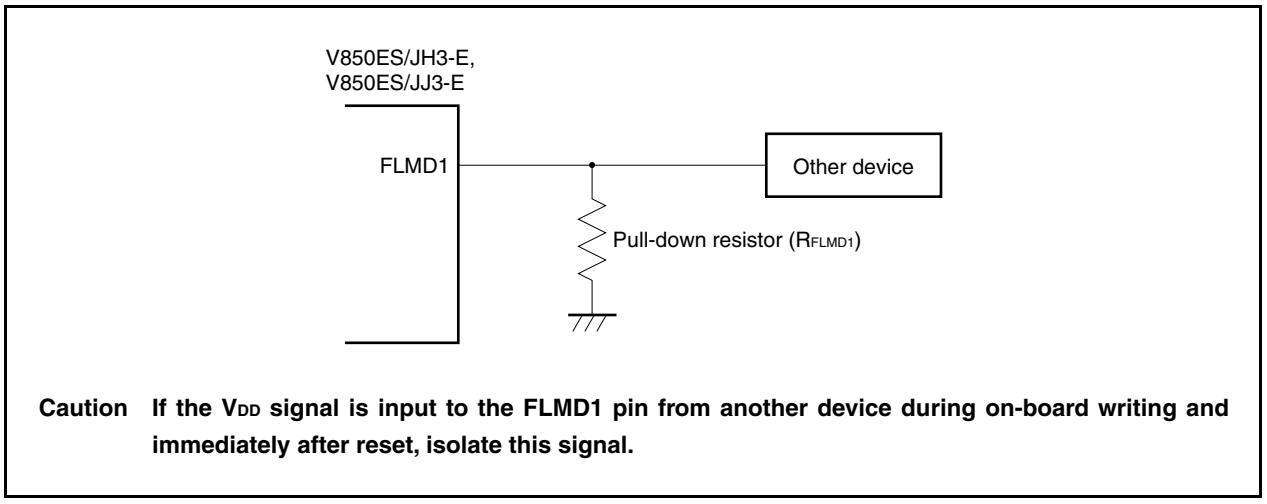
**Figure 33-11. FLMD0 Pin Connection Example**




**(2) FLMD1 pin**

When 0 V is input to the FLMD0 pin, the FLMD1 pin does not function. When $V_{DD}$ is supplied to the FLMD0 pin, the flash memory programming mode is entered, so 0 V must be input to the FLMD1 pin. The following shows an example of the connection of the FLMD1 pin.

**Figure 33-12. FLMD1 Pin Connection Example**




**Caution If the $V_{DD}$ signal is input to the FLMD1 pin from another device during on-board writing and immediately after reset, isolate this signal.**

### 34.2.3 Securement of user resources

The user must prepare the following to perform communication between MINICUBE2 and the target device and implement each debug function. These items need to be set in the user program or using the compiler options.

**(1) Securement of memory space**

The shaded portions in Figure 34-4 are the areas reserved for placing the debug monitor program, so user programs and data cannot be allocated in these spaces. These spaces must be secured so as not to be used by the user program.

**(2) Security ID setting**

The ID code must be embedded in the area between 0000070H and 0000079H in Figure 34-4, to prevent the memory from being read by an unauthorized person. For details, refer to **34.3 ROM Security Function**.

**(5) Securement of communication serial interface**

UARTC0, CSIF0, or CSIF3 is used for communication between MINICUBE2 and the target system. The settings related to the serial interface modes are performed by the debug monitor program, but if the setting is changed by the user program, a communication error may occur.

To prevent such a problem from occurring, communication serial interface must be secured in the user program.

[How to secure communication serial interface]

- On-chip debug mode register (OCDM)

  For the on-chip debug function using the UARTC0, CSIF0, or CSIF3, set the OCDM register functions to normal mode. Be sure to set as follows.

  - Input low level to the P56/INTP05/$\overline{\text{DRST}}$ pin.
  - Set the OCDM0 bit as shown below.

    <1> Clear the OCDM0 bit to 0.

    <2> Fix the P56/INTP05/$\overline{\text{DRST}}$ pin input to low level until the processing of <1> is complete.

- Serial interface registers

  Do not set the registers related to CSIF0, CSIF3, or UARTC0 in the user program.

- Interrupt mask register

  When CSIF0 is used, do not mask the transfer end interrupt (INTCF0R). When CSIF3 is used, do not mask the transfer end interrupt (INTCF3R). When UARTC0 is used, do not mask the reception completion interrupt (INTUC0R).

**(a) When CSIF0 is used**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CF0RIC | × | 0 | × | × | × | × | × | × |

**(b) When CSIF3 is used**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CF3RIC | × | 0 | × | × | × | × | × | × |

**(C) When UARTC0 is used**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| UC0RIC | × | 0 | × | × | × | × | × | × |

**Remark** ×: don't care