Renesas Electronics America Inc - UPD70F3779GF-GAT-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	76K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3779gf-gat-ax

(3) Port 9 mode control register (PMC9)

(1/2)

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H)	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	$\overline{\text{SCKF3}}$ I/O/TIAA51 input/TOAA51 output/A15 output

PMC914	Specification of P914 pin operation mode
0	I/O port
1	SOF3 output/RXDB1 input/INTP20 input/A14 output

PMC913	Specification of P913 pin operation mode
0	I/O port
1	SIF3 input/TXDB1 output/INTP19 input/A13 output

PMC912	Specification of P912 pin operation mode
0	I/O port
1	TOAB1OFF input/INTP18 input/A12 output

PMC911	Specification of P911 pin operation mode
0	I/O port
1	$\overline{\text{SCKE1}}$ I/O/TIAA50 input/TOAA50 output/A11 output

PMC910	Specification of P910 pin operation mode
0	I/O port
1	SOE1 output/RXDC5 input/SCL03 I/O/A10 output

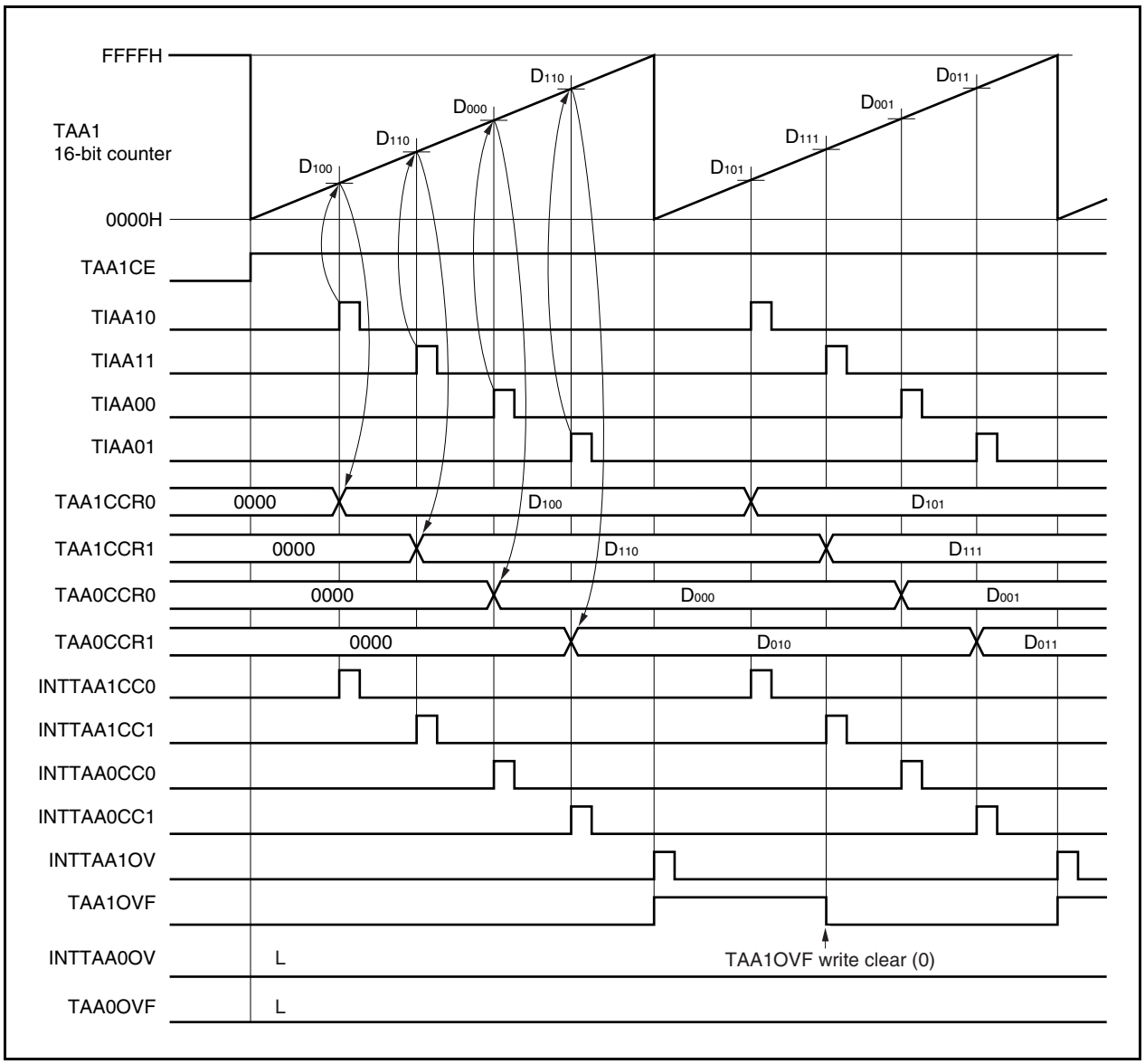
PMC99	Specification of P99 pin operation mode
0	I/O port
1	SIE1 input/TXDC5 output/SDA03 I/O/A9 output

PMC98	Specification of P98 pin operation mode
0	I/O port
1	TENC01 input/INTP17 input/A8 output

Remarks 1. The PMC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMC9 register as the PMC9H register and the lower 8 bits as the PMC9L register, they can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMC9H register.

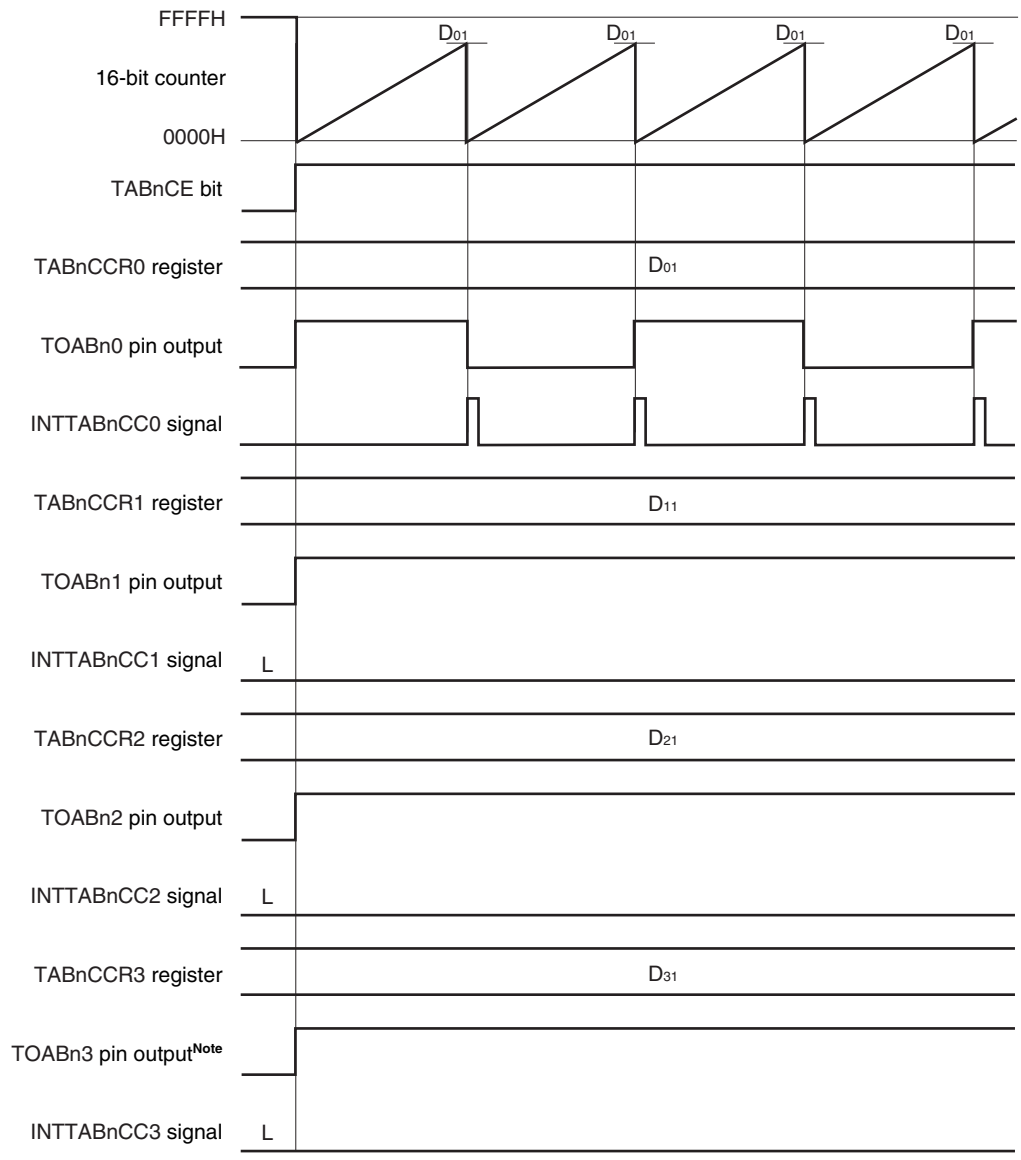
Figure 7-45. Example of Timing in Free-Running Mode (Capture Function)



If the set value of the TABnCCRk register is greater than the set value of the TABnCCR0 register, the count value of the 16-bit counter does not match the value of the TABnCCRk register. Consequently, the INTTABnCCk signal is not generated, nor is the output of the TOABnk pin changed.

Remark k = 1 to 3,
n = 0, 1

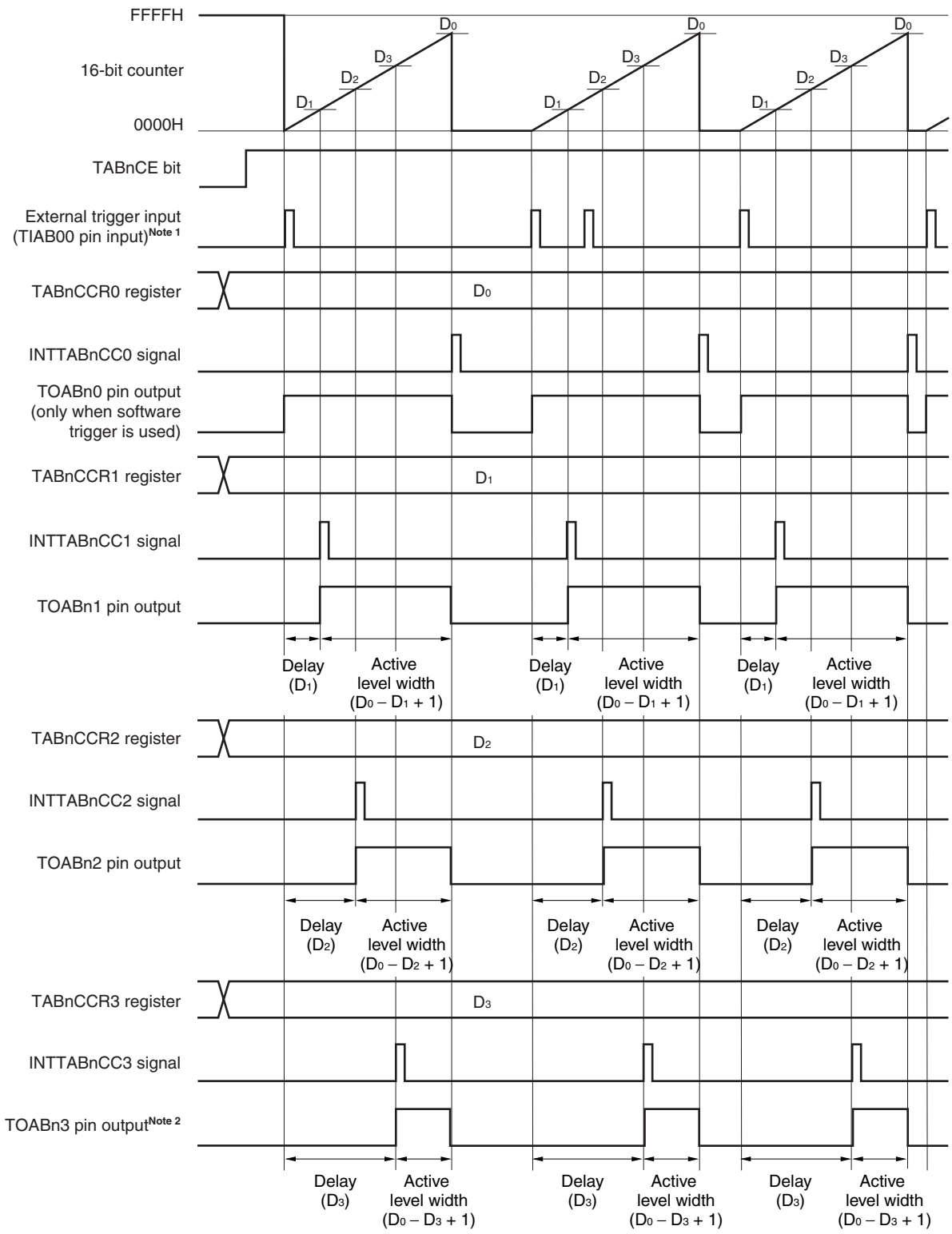
Figure 8-8. Timing Chart When $D_{01} < D_{k1}$



Note The V850ES/JH3-E only includes the TOAB13 pin; it is not provided with the TOAB03 pin.

Remark n = 0, 1

Figure 8-21. Basic Timing in One-Shot Pulse Output Mode



Notes 1. TAB1: TRGAB1 pin

2. The V850ES/JH3-E only includes the TOAB13 pin; it is not provided with the TOAB03 pin.

Remark n = 0, 1

(1) TAB1 dead-time compare register (TAB1DTC)

The TAB1DTC register is a 10-bit compare register that specifies the dead-time value.

Rewriting this register is prohibited when the TAB1CTL0.TAB1CE bit = 1.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution When generating a dead-time period, set the TAB1DTC register to 1 or higher.
Note, when the operation is stopped (TAB1CTL0.TAB1CE bit = 0), a dead-time period is not generated, so the output levels of the TOAB1T1 to TOAB1T3 and TOAB1B1 to TOAB1B3 pins are in their default states. Therefore, for the protection of the system, take measures such as making the TOAB1T1 to TOAB1T3 and TOAB1B1 to TOAB1B3 pins go into a high-impedance state before stopping operation, or setting the output levels of the pins before switching port modes.
When a dead-time period is not needed, set the TAB1DTC register to 0.

After reset: 0000H R/W Address: FFFFF584H

	15	10	9	0
TAB1DTC	000000		TAB1DTC9 to TAB1DTC0	

(2) Dead-time counters 1 to 3

The dead-time counters are 10-bit counters that count dead time.

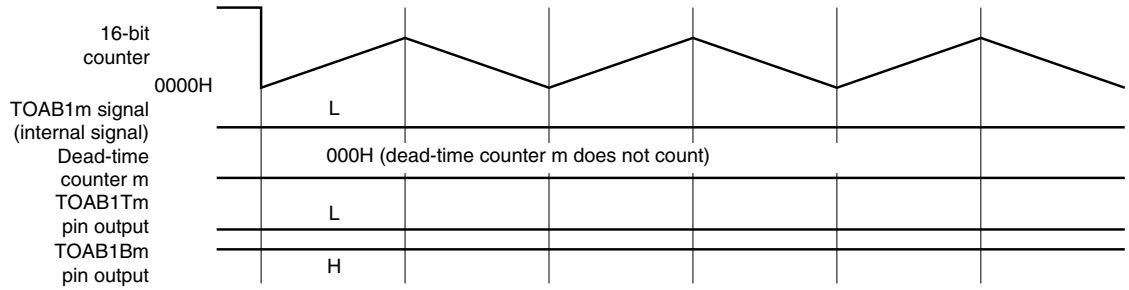
These counters are cleared or count up at the rising or falling edge of the TOAB1m output signal of TAB1, and are cleared or stopped when their count value matches the value of the TAB1DTC register. The count clock of these counters is the same as that set by the TAB1CTL0.TAB1CKS2 to TAB1CTL0.TAB1CKS0 bits of TAB1.

Remarks 1. The operation differs when the TAB1OPT2.TAB1DTM bit = 1. For details, see **11.4.2 (4) Automatic dead-time width narrowing function (TAB1OPT2.TAB1DTM bit = 1)**.

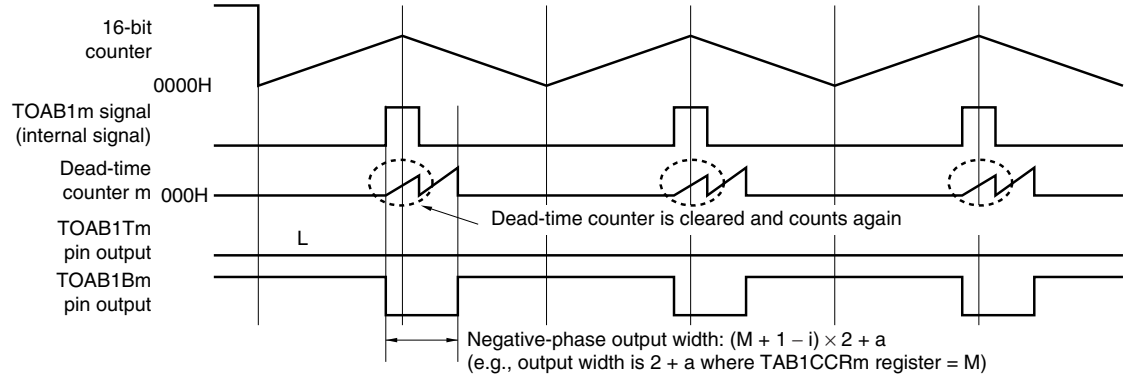
2. m = 1 to 3

Figure 11-12. PWM Output Waveform with Dead Time (2)

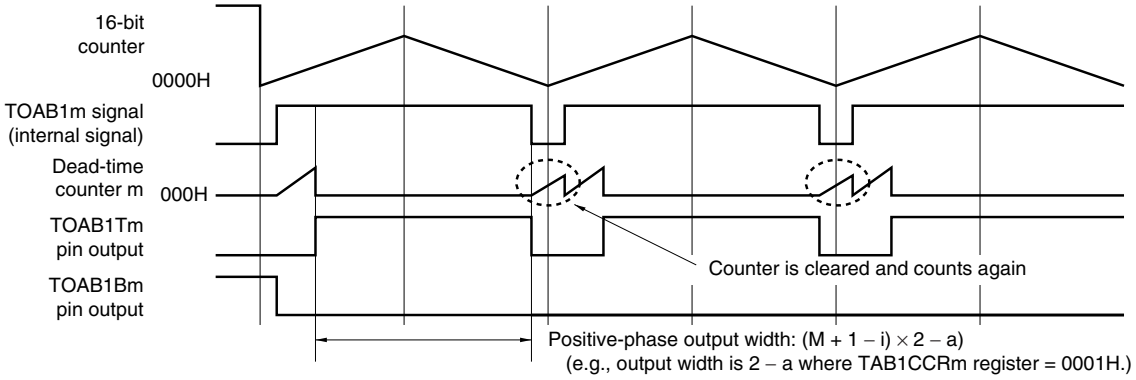
(a) 0% output (TAB1CCRm register = M + 1, TAB1CCR0 register = M, TAB1DTC register = a)



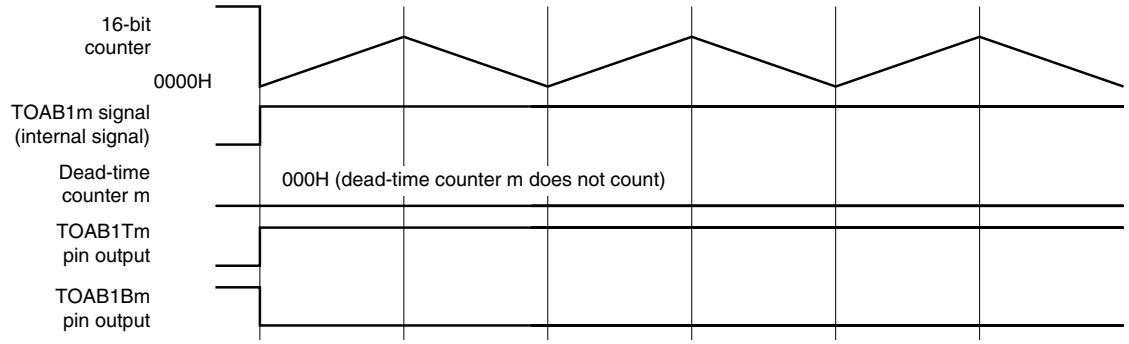
(b) In vicinity of 0% output (TAB1CCRm register = i ≥ M + 1 – a/2, TAB1CCR0 register = M, TAB1DTC register = a)



(c) In vicinity of 100% output (TAB1CCRm register = i ≤ a/2, TAB1CCR0 register = M, TAB1DTC register = a)



(d) 100% output (TAB1CCRm register = 0000H, TAB1CCR0 register = M, TAB1DTC register = a)



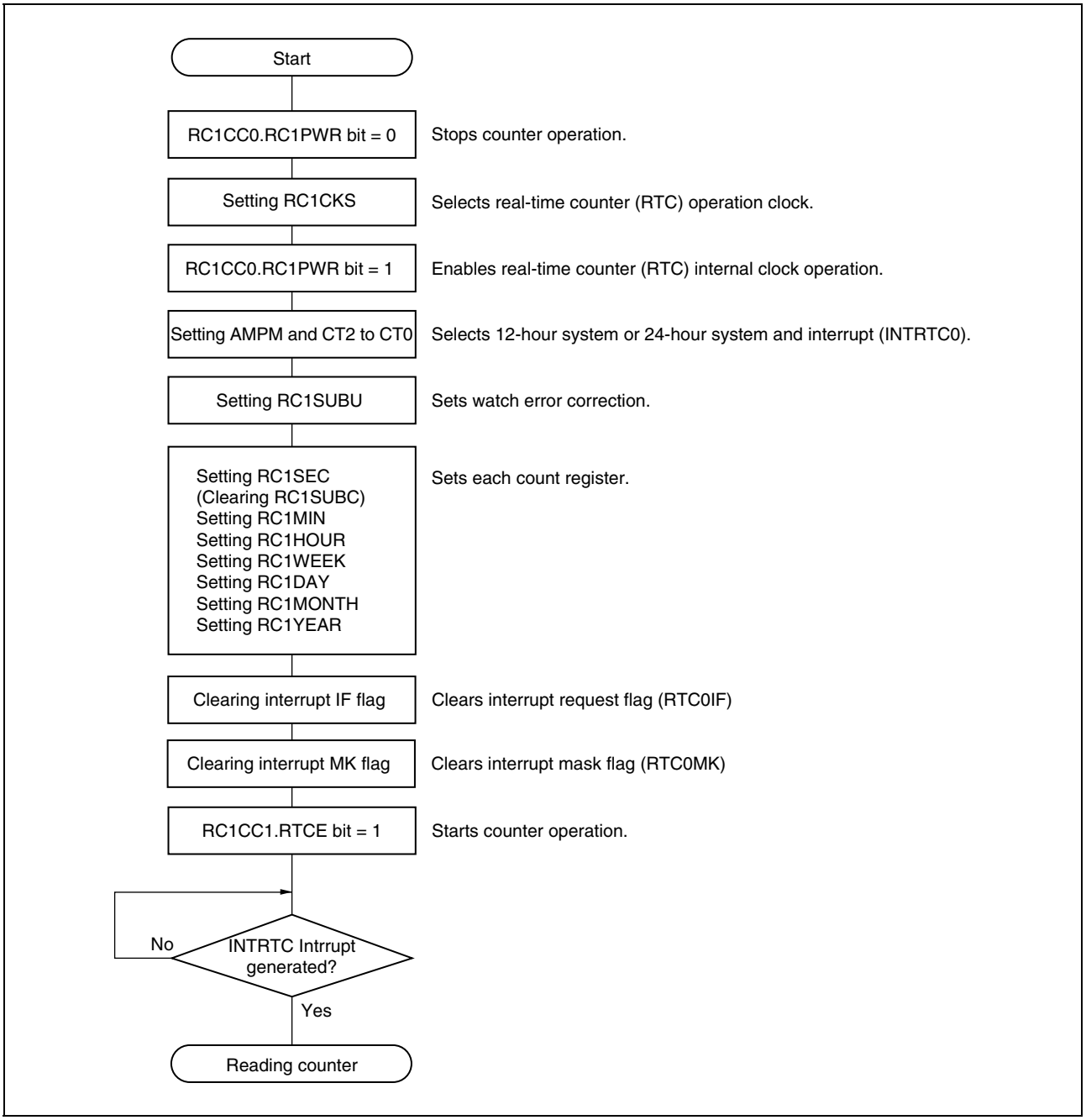
Remark m = 1 to 3

12.4 Operation

12.4.1 Initial settings

The initial settings are set when operating the watch function and performing a fixed-cycle interrupt operation.

Figure 12-2. Initial Setting Procedure



16.7.5 Reception error

In the single mode (UBnFIC0.UBnMOD bit = 0), the three types of errors that can occur during a receive operation are a parity error, framing error, and overrun error. In the FIFO mode (UBnFIC0.UBnMOD bit = 1), the three types of errors that can occur during a receive operation are a parity error, framing error, and overflow error.

As a result of data reception, the UBnSTR.UBnPE, UBnSTR.UBnFE, or UBnSTR.UBnOVE bit is set to 1 if a parity error, framing error, or overrun error occurs in the single mode. The UBnSTR.UBnOVF bit is set to 1 if an overflow error occurs in the FIFO mode. The UBnRXAP.UBnPEF or UBnRXAP.UBnFEF bit is set to 1 if a parity error or framing error occurs in the FIFO mode. At the same time, a reception error interrupt request signal (INTUBnTIRE) occurs. The contents of the error can be detected by reading the contents of the UBnSTR or UBnRXAP register.

The contents of the UBnSTR register are reset when 0 is written to the UBnOVF, UBnPE, UBnFE, or UBnOVE bit, or the UBnCTL0.UBnPWR or UBnCTL0.UBnRXE bit. The contents of the UBnRXAP register are reset when 0 is written to the UBnCTL0.UBnPWR bit.

Table 16-5. Reception Error Causes

Error Flag	Valid Operation Mode	Error Flag	Reception Error	Cause
UBnPE	Single mode	UBnPE	Parity error	The parity specification during transmission does not match the parity of the receive data
UBnFE		UBnFE	Framing error	No stop bit detected
UBnOVE		UBnOVE	Overrun error	The reception of the next data is ended before data is read from the UBnRX register
UBnOVF	FIFO mode	UBnOVF	Overflow error	The reception of the next data is ended while receive FIFO is full and before data is read.
UBnPEF		UBnPEF	Parity error	The parity specification during transmission does not match the parity of the data to be received.
UBnFEF		UBnFEF	Framing error	The stop bit is not detected when the target data is loaded.

Remark n = 0, 1

Figure 19-6. CSIF4 and UARTB0 Mode Switch Settings

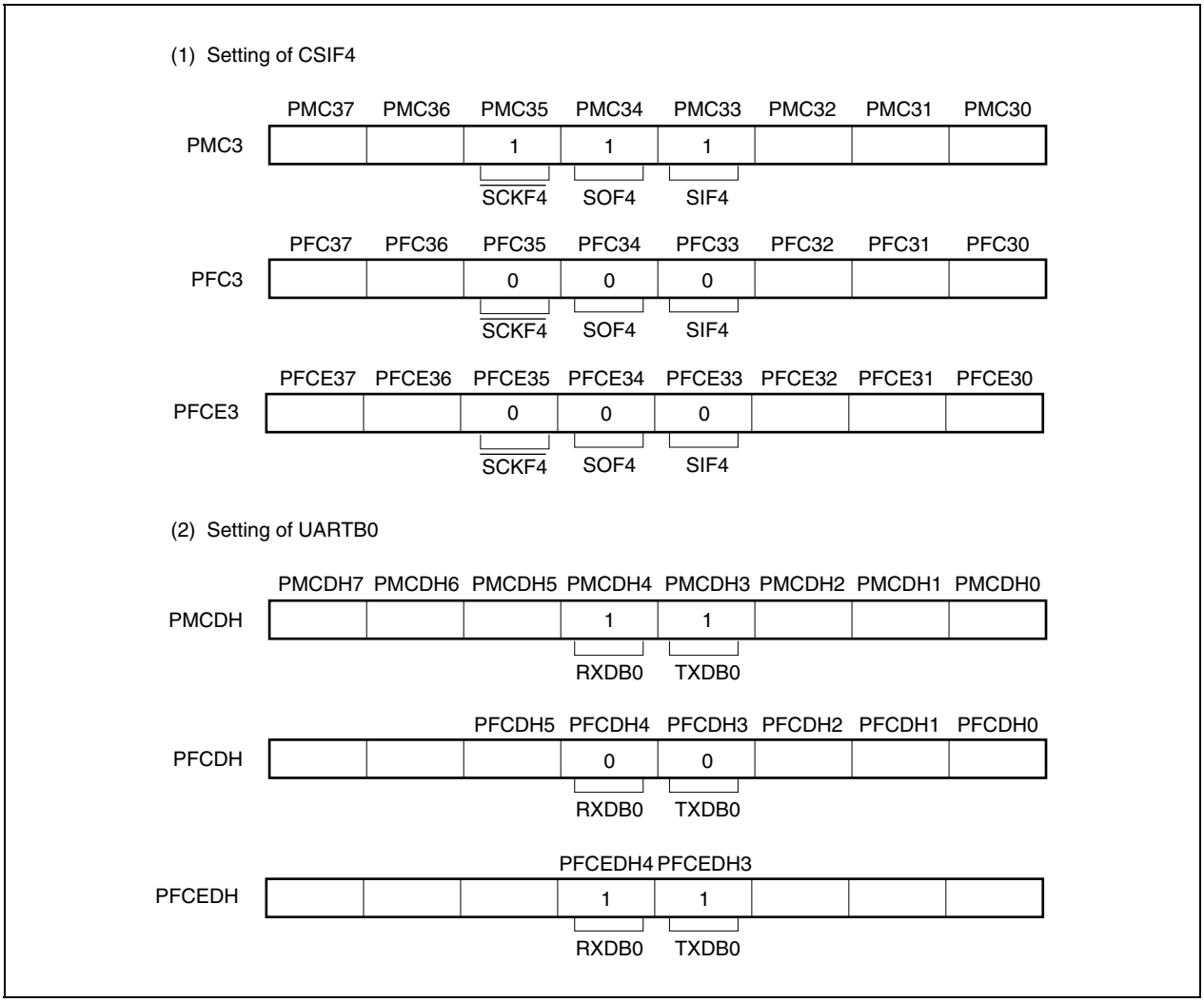


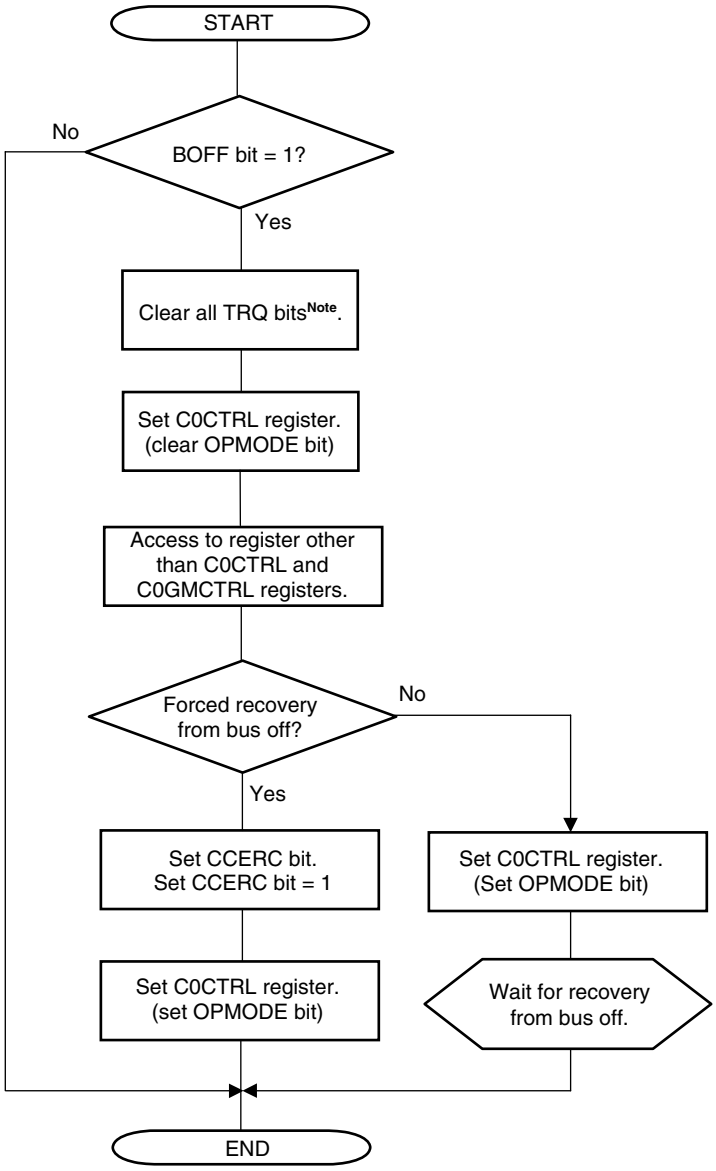
Table 20-2. Clock Settings

IICXn	IICCLn			Selection Clock	Transfer Clock	Settable Main Clock Frequency (fxx) Range	Transfer Speed	Operating Mode
CLXn	SMCn	CLn1	CLn0					
0	0	0	0	fxx/6 (OCKS0 = 11H)	fxx/264	24.00 MHz ≤ fxx ≤ 25.14 MHz	90.91 kHz to 95.23 kHz	Standard mode (SMCn = 0)
				fxx/8 (OCKS0 = 12H)	fxx/352	24.00 MHz ≤ fxx ≤ 33.52 MHz	68.18 kHz to 95.23 kHz	
				fxx/10 (OCKS0 = 13H)	fxx/440	30.00 MHz ≤ fxx ≤ 41.90 MHz	68.18 kHz to 95.23 kHz	
				fxx/2 (OCKS0 = 18H)	fxx/88	4.00 MHz ≤ fxx ≤ 6.25 MHz	45.45 kHz to 71.02 kHz	
0	0	0	1	fxx/4 (OCKSm = 10H)	fxx/344	24.00 MHz ≤ fxx ≤ 33.52 MHz	69.77 kHz to 97.44 kHz	
				fxx/6 (OCKSm = 11H)	fxx/516	25.14 MHz ≤ fxx ≤ 50.00 MHz	48.72 kHz to 96.90 kHz	
				fxx/8 (OCKSm = 12H)	fxx/688	33.52 MHz ≤ fxx ≤ 50.00 MHz	48.72 kHz to 72.67 kHz	
				fxx/10 (OCKSm = 13H)	fxx/860	41.90 MHz ≤ fxx ≤ 50.00 MHz	48.72 kHz to 58.14 kHz	
0	0	1	1	fxx/4 (OCKSm = 10H)	fxx/264	25.60 MHz	96.97 kHz	
				fxx/6 (OCKSm = 11H)	fxx/396	38.40 MHz	96.97 kHz	
0	1	0	X	fxx/4 (OCKSm = 10H)	fxx/96	24.00 MHz ≤ fxx ≤ 33.52 MHz	250.00 kHz to 349.17 kHz	High-speed mode (SMCn = 1)
				fxx/6 (OCKSm = 11H)	fxx/144	24.00 MHz ≤ fxx ≤ 50.00 MHz	166.67 kHz to 347.22 kHz	
				fxx/8 (OCKSm = 12H)	fxx/192	32.00 MHz ≤ fxx ≤ 50.00 MHz	166.67 kHz to 260.42 kHz	
				fxx/10 (OCKSm = 13H)	fxx/240	40.00 MHz ≤ fxx ≤ 50.00 MHz	166.67 kHz to 208.33 kHz	
0	1	1	1	fxx/4 (OCKSm = 10H)	fxx/72	25.60 MHz	355.56 kHz	
				fxx/6 (OCKSm = 11H)	fxx/108	38.40 MHz	355.56 kHz	
1	1	0	X	fxx/6 (OCKSm = 11H)	fxx/72	24.00 MHz ≤ fxx ≤ 25.14 MHz	333.33 kHz to 349.17 kHz	
				fxx/8 (OCKSm = 12H)	fxx/96	32.00 MHz ≤ fxx ≤ 33.52 MHz	333.33 kHz to 349.17 kHz	
				fxx/10 (OCKSm = 13H)	fxx/120	40.00 MHz ≤ fxx ≤ 41.90 MHz	333.33 kHz to 349.17 kHz	
Other than above				Setting prohibited	–	–	–	–

Remarks 1. n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)
m = 0 to 2

2. ×: don't care

Figure 21-54. Bus-off Recovery (Other Than in Normal Operation Mode with ABT)



Note To initialize the message buffer by clearing the RDY bit before starting the bus-off recovery sequence, clear all the TRQ bits.

Caution If a request to change the mode from the initialization mode to any operation mode is made to execute the bus-off recovery sequence again during a bus-off recovery sequence, the receive error counter (C0ERC.REC0 to REC6 bits) is cleared. It is therefore necessary to detect 11 contiguous recessive bits 128 times on the bus again.

Remark OPMODE: Normal operation mode, normal operation mode with ABT, receive-only mode, single-shot mode, self-test mode

22.4 Cautions

(1) Clock accuracy

To operate the USB function controller, the internal clock (6 MHz external clock × internal clock multiplied by 8 = 48 MHz internal clock) or external clock (external clock input to EXCLK pin (f_{USB} = 48 MHz)) must be used as the USB clock. When the internal clock is used as the USB clock, use a resonator with an accuracy of 6 MHz ±500 ppm (max.). When the external clock is used, apply a clock with an accuracy of 48 MHz ±500 ppm (max.) to the EXCLK pin. If the USB clock accuracy drops, the transmission data cannot satisfy the USB rating.

(2) Stopping the USB clock

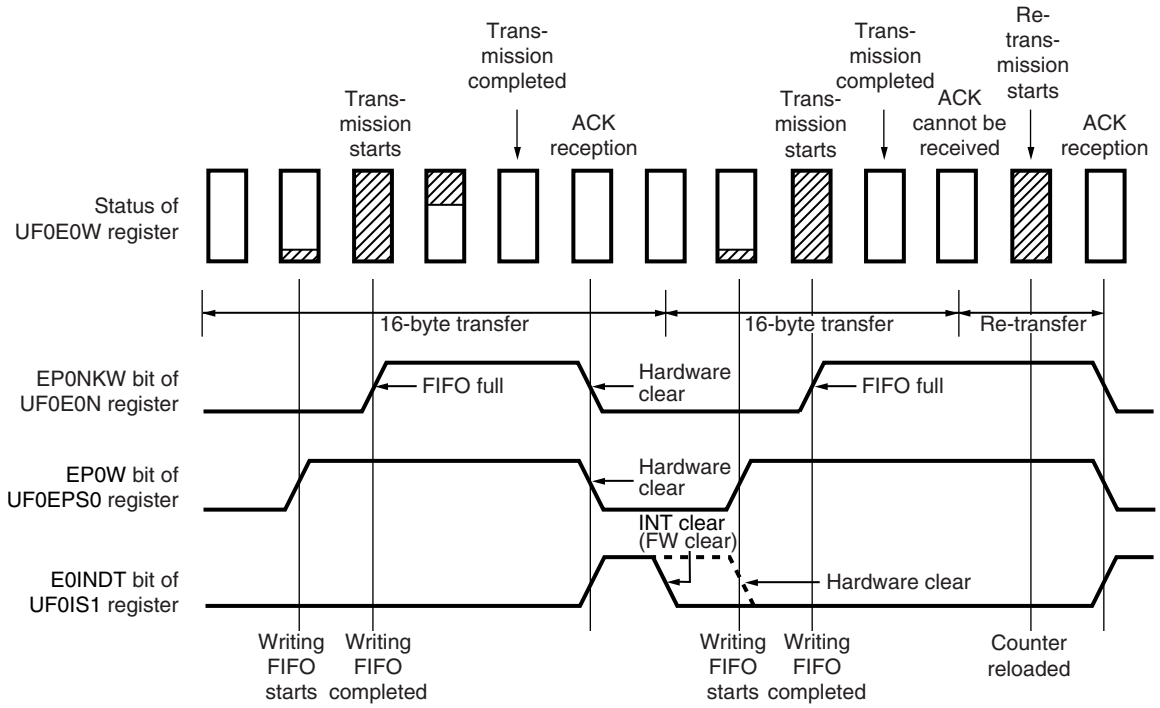
When the main clock (f_{XX}) has been selected as the USB function controller clock and it is necessary to stop the USB function controller, be sure to stop the USB function controller (by setting bits 1 and 0 of the UFCKMSK register to 1) first before stopping the main clock (f_{XX}).

If the main clock (f_{XX}) is stopped without first stopping the USB function controller, a malfunction might occur due to noise in the clock pulse when the main clock (f_{XX}) is restarted.

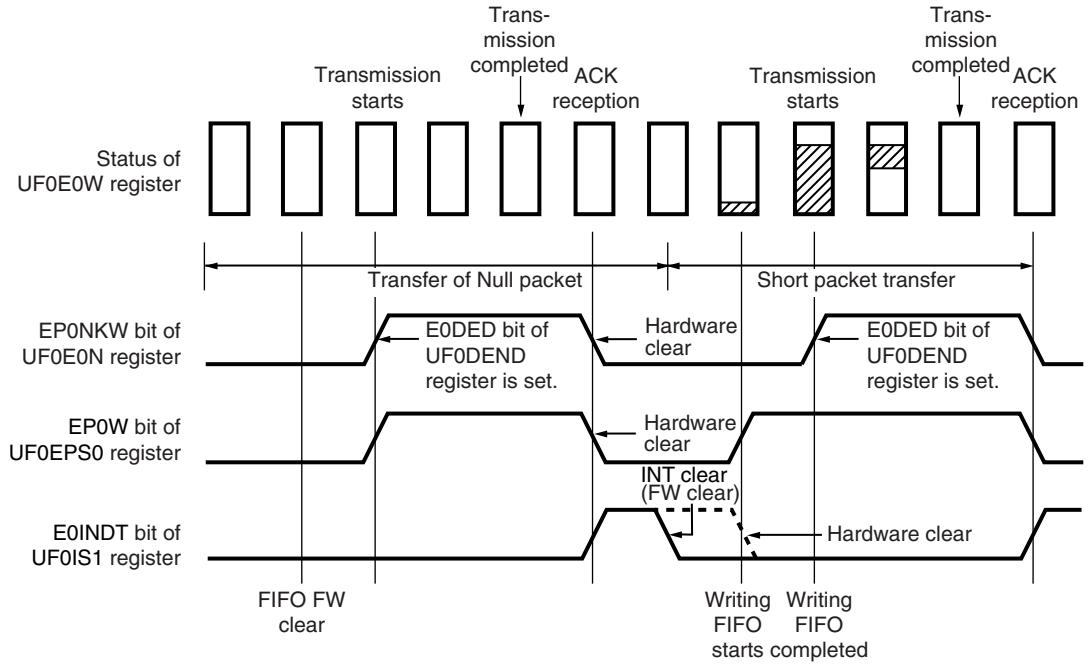
Similarly, when an external clock whose signal is input from the EXCLK pin is selected as the USB function controller clock, measures must be taken to prevent noise from being generated in the clock pulse by the external circuit. If this is not feasible, then the USB function controller must be stopped first before stopping the main clock (f_{XX}).

Figure 22-6. Operation of UF0E0W Register

(a) 16-byte transmission



(b) When Null packet or short packet is transmitted



(3) UF0 EP1 status register L (UF0E1SL)

This register stores the value that is to be returned in response to the GET_STATUS Endpoint1 request.

This register can be read or written in 8-bit units. Note, however, that data can be written to this register only when the EP0NKA bit is set to 1.

If an error occurs in Endpoint1, the E1HALT bit is set to 1. A write access to this register is ignored while a USB-side access to Endpoint1 is being received.

The hardware automatically transmits the contents of this register to the host when it has received the GET_STATUS Endpoint1 request. If Endpoint1 has stalled, the UF0BI1 register is cleared and the BKI1NK bit is cleared to 0.

Because writing this register is always masked when transfer to Endpoint1, rather than control transfer, is executed, be sure to check this register to see if data has been correctly written to it.

Caution To rewrite this register, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E1SL	0	0	0	0	0	0	0	E1HALT	00200150H	00H

Bit position	Bit name	Function
0	E1HALT	This bit indicates the status of Endpoint1. 1: Stalled 0: Not stalled This bit is set to 1 by hardware when the SET_FEATURE Endpoint1 request has been received. It is cleared to 0 by hardware when the CLEAR_FEATURE Endpoint1 request, SET_CONFIGURATION request, or the SET_INTERFACE request for the Interface to which Endpoint1 is linked has correctly been received. DATA PID is initialized to DATA0.

(16) RJBR: Receive jabber counter

Access This register can be read and written in 32-bit units.

Address 002E 017CH

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

31	30	29	28	27	26	25	24
RJBR31	RJBR30	RJBR29	RJBR28	RJBR27	RJBR26	RJBR25	RJBR24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
RJBR23	RJBR22	RJBR21	RJBR20	RJBR19	RJBR18	RJBR17	RJBR16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
RJBR15	RJBR14	RJBR13	RJBR12	RJBR11	RJBR10	RJBR9	RJBR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
RJBR7	RJBR6	RJBR5	RJBR4	RJBR3	RJBR2	RJBR1	RJBR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
31 to 0	RJBR[31:0]	This counter is incremented if the receive packet length exceeds 1,518 bytes (1,522 bytes when a VLAN frame is received) and the packet contains a CRC error or an alignment error. If a packet exceeding the length set to the LMAX register is received when the MACC1.HUGEN bit is set to 0, a CRC check is executed as soon as the set value of the LMAX register has been reached. Consequently, a CRC error may be detected at that point and this counter may not be incremented.

(30) TXPF: Transmit pause control frame counter

Access This register can be read and written in 32-bit units.

Address 002E 01D8H

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

31	30	29	28	27	26	25	24
TXPF31	TXPF30	TXPF29	TXPF28	TXPF27	TXPF26	TXPF25	TXPF24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
TXPF23	TXPF22	TXPF21	TXPF20	TXPF19	TXPF18	TXPF17	TXPF16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
TXPF15	TXPF14	TXPF13	TXPF12	TXPF11	TXPF10	TXPF9	TXPF8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TXPF7	TXPF6	TXPF5	TXPF4	TXPF3	TXPF2	TXPF1	TXPF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
31 to 0	TXPF[31:0]	This counter is incremented each time a pause control frame has been transmitted when the maximum amount of data has been stored in the receive FIFO.

27.5 IDLE2 Mode

27.5.1 Setting and operation status

The IDLE2 mode is set by setting the PSMR.PSM1 and PSMR.PSM0 bits to 10 and setting the PSC.STP bit to 1 in the normal operation mode.

In the IDLE2 mode, the clock oscillator continues operation but clock supply to the CPU, PLL, flash memory, and other on-chip peripheral functions stops.

As a result, program execution stops and the contents of the internal RAM before the IDLE2 mode was set are retained. The CPU, PLL, and other on-chip peripheral functions stop operating. However, the on-chip peripheral functions that can operate with the subclock or an external clock continue operating.

Table 27-7 shows the operating status in the IDLE2 mode.

The IDLE2 mode can reduce the power consumption more than the IDLE1 mode because it stops the operations of the on-chip peripheral functions, PLL, and flash memory. However, because the PLL and flash memory are stopped, a setup time for the PLL and flash memory is required when IDLE2 mode is released.

Cautions 1. Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the IDLE2 mode.

2. If the IDLE2 mode is set while an unmasked interrupt request signal is being held pending, the IDLE2 mode is released immediately by the pending interrupt request.

CHAPTER 33 FLASH MEMORY

The V850ES/JH3-E and V850ES/JJ3-E incorporate a flash memory.

- μPD70F3778: 256 KB flash memory
- μPD70F3779, 70F3781: 384 KB flash memory
- μPD70F3780, 70F3782, 70F3783, 70F3784, 70F3785, 70F3786: 512 KB flash memory

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/JH3-E and V850ES/JJ3-E are soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

33.1 Features

- 4-byte/1-clock access (when instruction is fetched)
- Capacity: 256/384/512 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
  - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Flash memory rewrite prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

Table 33-6. Wiring of V850ES/JH3-E Flash Writing Adapters (FA-128GF-GAT-B) (1/2)

Flash Programmer (FG-FP5) Connection Pin			Name of FA Board Pin	CSIF0 + HS Used		CSIF0 Used		UARTC0 Used	
Signal Name	I/O	Pin Function		Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SI	P41/SOF0	4	P41/SOF0	4	P30/TXDC0	25
SO/TxD	Output	Transmit signal	SO	P40/SIF0	3	P40/SIF0	3	P31/RXDC0	26
SCK	Output	Transfer clock	SCK	P42/$\overline{\text{SCKF0}}$	5	P42/$\overline{\text{SCKF0}}$	5	Not needed	–
CLK	Output	Clock to V850ES/JH3-E	X1	Not needed	–	Not needed	–	Not needed	–
			X2	Not needed	–	Not needed	–	Not needed	–
/RESET	Output	Reset signal	/RESET	$\overline{\text{RESET}}$	18	$\overline{\text{RESET}}$	18	$\overline{\text{RESET}}$	18
FLMD0	Output	Write voltage	FLMD0	FLMD0	12	FLMD0	12	FLMD0	12
FLMD1	Output	Write voltage	FLMD1	PDL5/AD5/ FLMD1	92	PDL5/AD5/ FLMD1	92	PDL5/AD5/ FLMD1	92
HS	Input	Handshake signal for CSI0 + HS communication	RESERVE/ HS	P20	38	Not needed	–	Not needed	–
VDD	–	VDD voltage generation/ voltage monitor	VDD	V_{DD}	13, 82	V_{DD}	13, 82	V_{DD}	13, 82
				EV_{DD}	35, 61, 85, 102, 118	EV_{DD}	35, 61, 85, 102, 118	EV_{DD}	35, 61, 85, 102, 118
				UV_{DD}	11	UV_{DD}	11	UV_{DD}	11
				AV_{REF0}	1	AV_{REF0}	1	AV_{REF0}	1
GND	–	Ground	GND	V_{SS}	15, 34, 60, 84, 101, 117	V_{SS}	15, 34, 60, 84, 101, 117	V_{SS}	15, 34, 60, 84, 101, 117
				AV_{SS}	2	AV_{SS}	2	AV_{SS}	2

Cautions 1. Be sure to connect the REGC pin to GND via 4.7 μF (recommend value) capacitor.

2. Clock cannot be supplied from the CLK pin of the flash programmer.
Create an oscillator on the board and supply clock.

CHAPTER 37 RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/index.html)

Remark Evaluation of the soldering conditions for the (A) standard products is incomplete because these products are under development.

Table 37-1. Surface Mounting Type Soldering Conditions

μPD70F3778GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3779GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3780GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3781GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3782GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3783GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. Products with –AX at the end of the part number are lead-free products.

2. For soldering methods and conditions other than those recommended, please contact a Renesas Electronics sales representative.