Renesas Electronics America Inc - UPD70F3780GF-GAT-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	76K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3780gf-gat-ax

Conventions	Data significance:	Higher digits on the left and lower digits on the right
	Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
	Memory map address:	Higher addresses on the top and lower addresses on the bottom
	Note:	Footnote for item marked with **Note** in the text
	Caution:	Information requiring particular attention
	Remark:	Supplementary information
	Numeric representation:	Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH
	Prefix indicating power of 2 (address space, memory capacity):	K (kilo): $2^{10} = 1,024$ M (mega): $2^{20} = 1,024^2$ G (giga): $2^{30} = 1,024^3$

2.4 Cautions

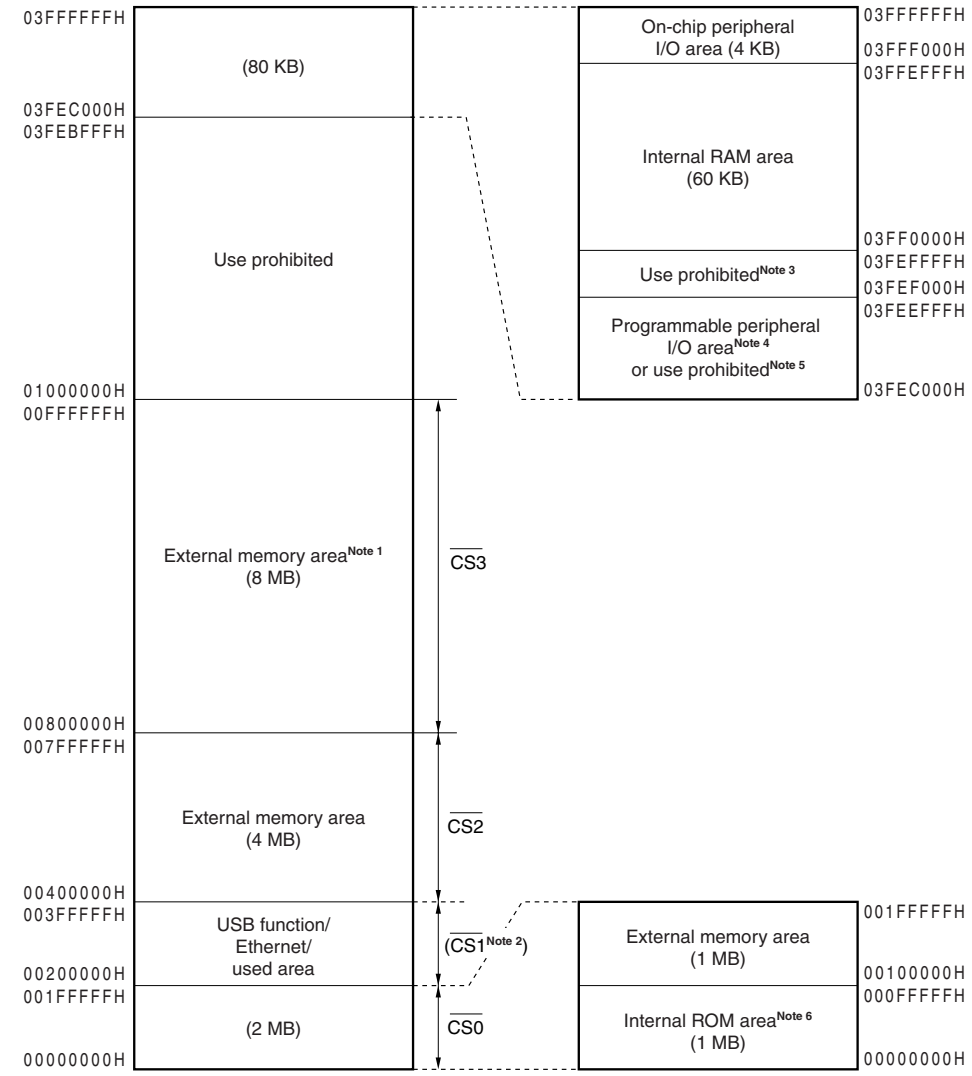
When the power is turned on, the following pins may output an undefined level temporarily even during reset.

- P51/INTP08/DDO pin

5.3 Memory Block Function

The 16 MB external memory space is divided into memory blocks of 2 MB, 4 MB, and 8 MB from the lowest of the memory space. The programmable wait function and bus cycle operation mode for each of these blocks can be independently controlled in one-block units.

Figure 5-1. Data Memory Map: Physical Address



Notes 1. Use of this area is allowed only when using the V850ES/JJ3-E. When using the V850ES/JH3-E, this area cannot be used.

2. $\overline{CS1}$ is not provided as an external signal of the V850ES/Jx3-E; it is used internally as a chip select signal for the USB and Ethernet.

3. Use of addresses 03FEF000H to 03FEFFFFH is prohibited because these addresses are in the same area as the on-chip peripheral I/O area.

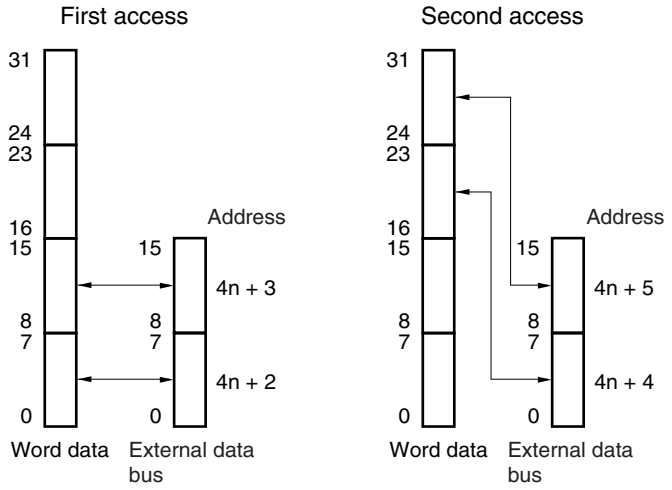
4. Only the programmable peripheral I/O area is seen as images of 256 MB each in the 4 GB address space.

5. In the CAN controller version, addresses 03FEC000H to 03FEEFFFH are assigned as a programmable peripheral I/O area in addresses 03FEC000H to 03FECBFFH. Use of these addresses in a version without a CAN controller is prohibited.

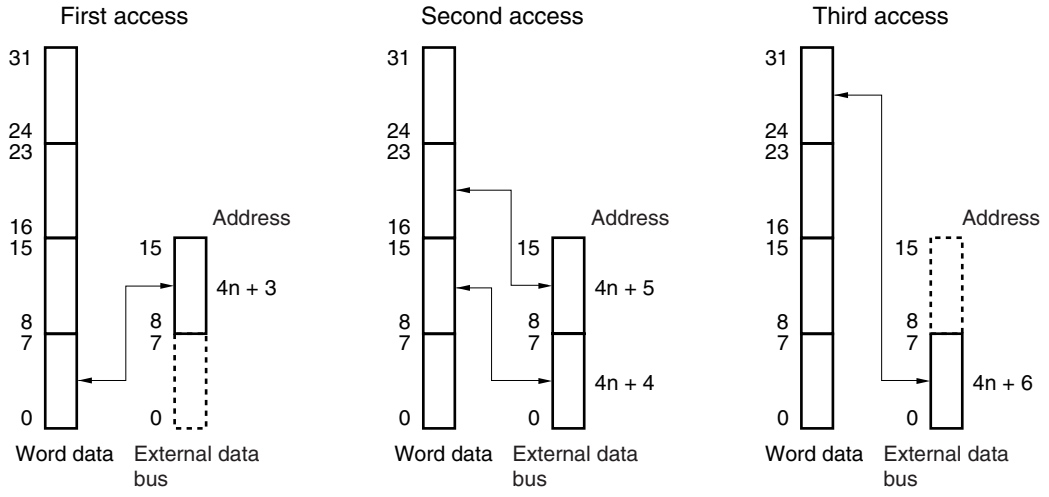
6. This area is used as an external memory area when data write access to this area is executed.

(a) 16-bit data bus width (2/2)

<3> Access to address (4n + 2)



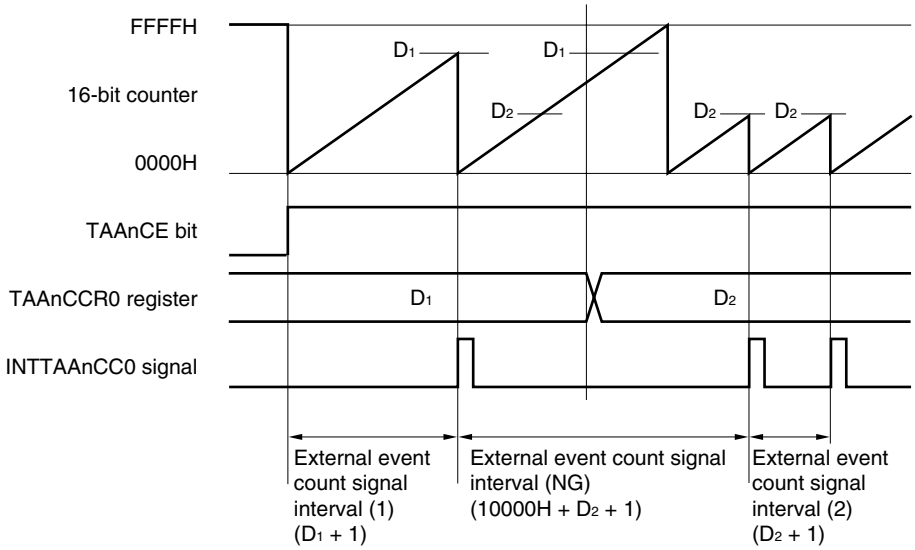
<4> Access to address (4n + 3)



(b) Notes on rewriting the TAAnCCR0 register

To change the value of the TAAnCCR0 register to a smaller value, stop counting once and then change the set value.

If the value of the TAAnCCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



Remark n = 0 to 5

If the value of the TAAnCCR0 register is changed from D_1 to D_2 while the count value is greater than D_2 but less than D_1, the count value is transferred to the CCR0 buffer register as soon as the TAAnCCR0 register has been rewritten. Consequently, the value that is compared with the 16-bit counter is D_2.

Because the count value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the count value matches D_2, the INTTAAnCC0 signal is generated.

Therefore, the INTTAAnCC0 signal may not be generated at the valid edge count of "(D_1 + 1) times" or "(D_2 + 1) times" as originally expected, but may be generated at the valid edge count of "(10000H + D_2 + 1) times".

Table 7-8 show the timer modes that can be used in the tuned-operation mode and Table 7-9 shows the differences of the timer output functions between individual operation and tuned operation (√: Settable, ×: Not settable).

Table 7-8. Timer Modes Usable in Tuned-Operation Mode

Master Timer	Slave Timer	Free-Running Timer Mode	PWM Mode
TAA1	TAA0	√	√
TAA3	TAA2	√	√
TAB0	TAA5	√	√
TAB1	TAA4	√	√

Table 7-9. Timer Output Functions

Tuned Channel	Timer	Pin	Free-Running Timer Mode		PWM Mode	
			Individual Operation	Tuned Operation	Individual Operation	Tuned Operation
Ch0	TAA1 (master)	TOAA10	PPG	←	Toggle	←
		TOAA11	PPG	←	PWM	←
	TAA0 (slave)	TOAA00	PGP	←	Toggle	PWM
		TOAA01	PPG	←	PWM	←
Ch1	TAA3 (master)	TOAA30	PPG	←	Toggle	←
		TOAA31	PPG	←	PWM	←
	TAA2 (slave)	TOAA20	PPG	←	Toggle	PWM
		TOAA21	PPG	←	PWM	←
Ch2	TAB0 (master)	TOAB00	PPG	←	Toggle	←
		TOAB01 to TOAB03	PPG	←	PWM	←
	TAA5 (slave)	TOAA50	PPG	←	Toggle	PWM
		TOAA51	PPG	←	PWM	←
Ch3	TAB1 (master)	TOAB10	PPG	←	Toggle	←
		TOAB11 to TOAB13	PPG	←	PWM	←
	TAA4 (slave)	TOAA40	PPG	←	Toggle	PWM
		TOAA41	PPG	←	PWM	←

Remark The timing of transmitting data from the compare register of the buffer register is as follows.

- PPG: CPU write timing
- Toggle, PWM, triangular wave PWM: Timing at which timer counter and compare register match TOAAn0 and TOABm0

(6) TABn I/O control register 4 (TABnIOC4)

The TABnIOC4 register is an 8-bit register that controls the timer output.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H. This register is not reset by stopping the timer operation (TABnCTL0.TABnCE = 0).

Cautions 1. Accessing the TABnIOC4 register is prohibited in the following statuses. For details, see 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and the main clock oscillation is stopped**
- **When the CPU operates on the internal oscillation clock**

2. The TABnIOC4 register can be set only in the interval timer mode and free-running timer mode. Be sure to set the TABnIOC4 register to 00H in all other modes (for details of the mode setting, see 8.4 (2) TABn control register 1 (TABnCTL1)). Even in free-running timer mode, if the TABnCCR0 to TABnCCR3 registers are set to the capture function, the setting of the TABnIOC4 register becomes invalid.

After reset: 00H R/W Address: TAB0IOC4 FFFFF550H, TAB1IOC4 FFFFF570H

TABnIOC4 (n = 0, 1)

7	6	5	4	3	2	1	0
TABnOS3Note	TABnOR3Note	TABnOS2	TABnOR2	TABnOS1	TABnOR1	TABnOS0	TABnOR0

TABnOSm	TABnORm	Toggle control of TOABnm pin (m = 0 to 3)
0	0	No request. Normal toggle operation.
0	1	Reset request Fix to inactive level upon next match between value of 16-bit counter and value of TAAnCCRm register.
1	0	Set request Fix to active level upon next match between value of 16-bit counter and value of TAAnCCRm register.
1	1	Keep request Keep the current output level.

Note The TOAB03 pin is not provided in the V850ES/JH3-E. Set the TAB0OS3 and TAB0OR3 bits to 0.

When the TABnCE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H in synchronization with the count clock, and the counter starts counting. At this time, the output of the TOABn0 pin is inverted. Additionally, the set value of the TABnCCR0 register is transferred to the CCR0 buffer register.

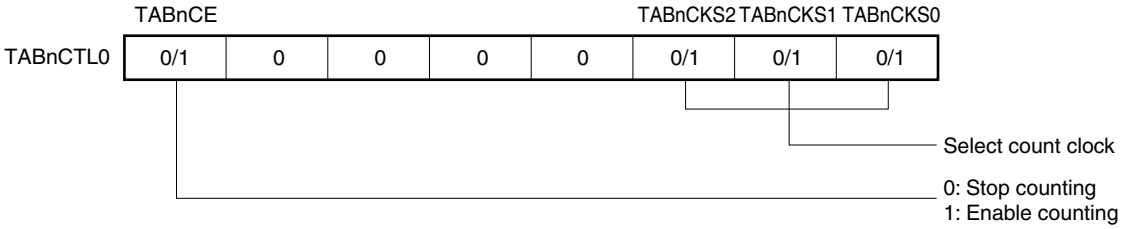
When the count value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, the output of the TOABn0 pin is inverted, and a compare match interrupt request signal (INTTABnCC0) is generated.

The interval can be calculated by the following expression.

Interval = (Set value of TABnCCR0 register + 1) × Count clock cycle

Figure 8-4. Register Setting for Interval Timer Mode Operation (1/2)

(a) TABn control register 0 (TABnCTL0)



(b) TABn control register 1 (TABnCTL1)

Note This bit can be set to 1 only when the interrupt request signals (INTTABnCC0 and INTTABnCCk) are masked by the interrupt mask flags (TABnCCMK0 to TABnCCMKk) and the timer output (TOABnk) is performed at the same time. However, the TABnCCR0 and TABnCCRk registers must be set to the same value (see **8.5.1 (2) (d) Operation of TABnCCR1 to TABnCCR3 registers**) (k = 1 to 3).

Remark n = 0, 1

(b) When using capture/compare register as capture register

Figure 9-38. Software Processing Flow in Free-Running Timer Mode (Capture Function) (1/2)

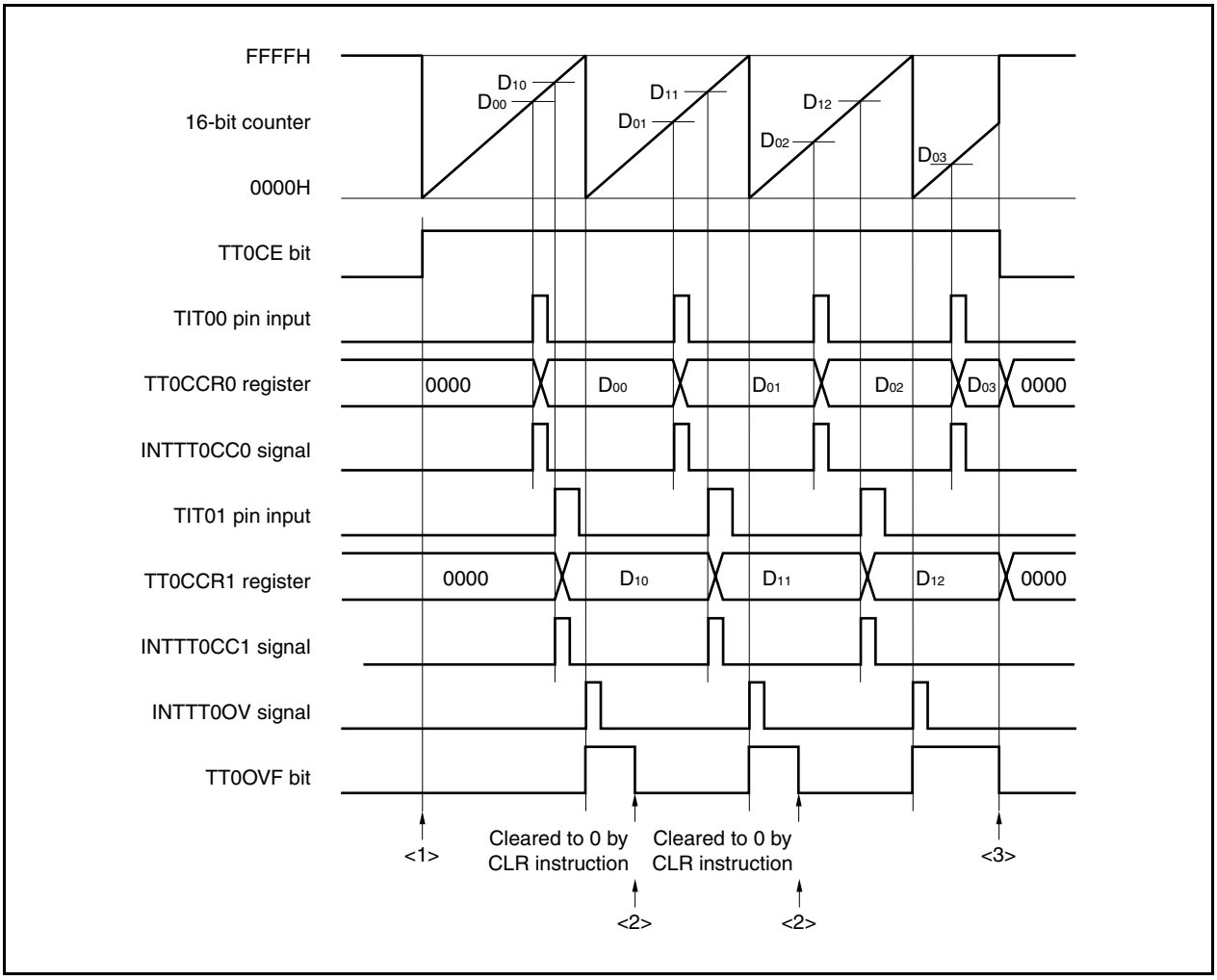
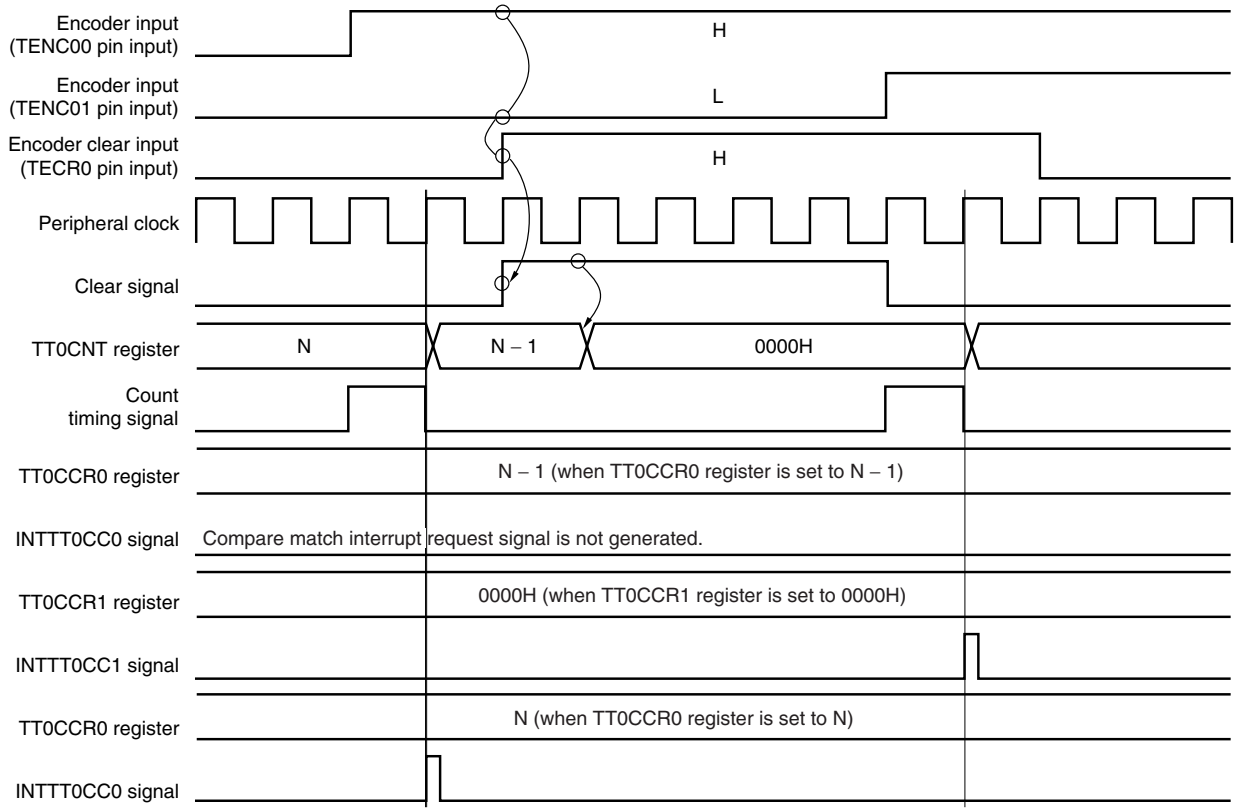


Figure 9-54. Operation Example (When TT0SCE Bit = 1, TT0ZCL Bit = 1, TT0BCL Bit = 0, TT0ACL Bit = 1, TT0UDS1 and TT0UDS0 Bits = 11, TECR0 = High Level, TENC01 = Low Level, and TENC00 = High Level) (3/3)

(iv) If the high level is input to the TECR0 pin later than the low level is input to the TENC01 pin while the counter is counting up, the counter is cleared after it counts up.



If the counter is cleared in this way, a miscount does not occur even if inputting the signal to the TECR0 pin is late, because the clear level condition of the TECR0, TENC01, and TENC00 pins is set and the 16-bit counter is cleared to 0000H when the clear level condition is detected.

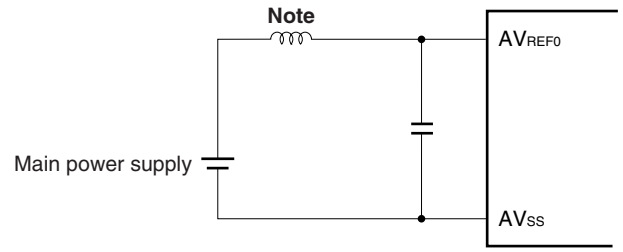
(7) AV_{REF0} pin

(a) The AV_{REF0} pin is used as the power supply pin of the A/D converter and also supplies power to the alternate-function ports. In an application where a backup power supply is used, be sure to supply the same potential as V_{DD} to the AV_{REF0} pin as shown in Figure 15-15.

(b) The AV_{REF0} pin is also used as the reference voltage pin of the A/D converter. If the source supplying power to the AV_{REF0} pin has a high impedance or if the power supply has a low current supply capability, the reference voltage may fluctuate due to the current that flows during conversion (especially, immediately after the conversion operation enable bit ADA0CE has been set to 1). As a result, the conversion accuracy may drop. To avoid this, it is recommended to connect a capacitor across the AV_{REF0} and AV_{SS} pins to suppress the reference voltage fluctuation as shown in Figure 15-15.

(c) If the source supplying power to the AV_{REF0} pin has a high DC resistance (for example, because of insertion of a diode), the voltage when conversion is enabled may be lower than the voltage when conversion is stopped, because of a voltage drop caused by the A/D conversion current.

Figure 15-15. AV_{REF0} Pin Processing Example



Note Parasitic inductance

(8) Reading ADA0CRn register

When the ADA0M0 to ADA0M2, ADA0S, ADA0PFM, or ADA0PFT register is written, the contents of the ADA0CRn register may be undefined. Read the conversion result after completion of conversion and before writing to the ADA0M0 to ADA0M2, ADA0S, ADA0PFM, or ADA0PFT register. Also, when an external/timer trigger is acknowledged, the contents of the ADA0CRn register may be undefined. Read the conversion result after completion of conversion and before the next external/timer trigger is acknowledged. The correct conversion result may not be read at a timing different from the above.

(9) External trigger mode

When using the external trigger mode, the input trigger during A/D conversion will not be acknowledged.

(3) IIC flag registers n (IICFn)

The IICFn registers set the I²C0n operation mode and indicate the I²C bus status.

These registers can be read or written in 8-bit or 1-bit units. However, the STCFn and IICBSYn bits are read-only.

IICRSVn enables/disables the communication reservation function (see **20.14 Communication Reservation**).

The initial value of the IICBSYn bit is set by using the STCENn bit (see **20.15 Cautions**).

The IICRSVn and STCENn bits can be written only when operation of I²C0n is disabled (IICCn.IICEn bit = 0). After operation is enabled, IICFn can be read.

Reset sets these registers to 00H.

Remark n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

21.10 Message Transmission

21.10.1 Message transmission

In all the operation modes, if the C0MCTRLm.TRQ bit is set to 1 in a message buffer that satisfies the following conditions, the message buffer that is to transmit a message is searched.

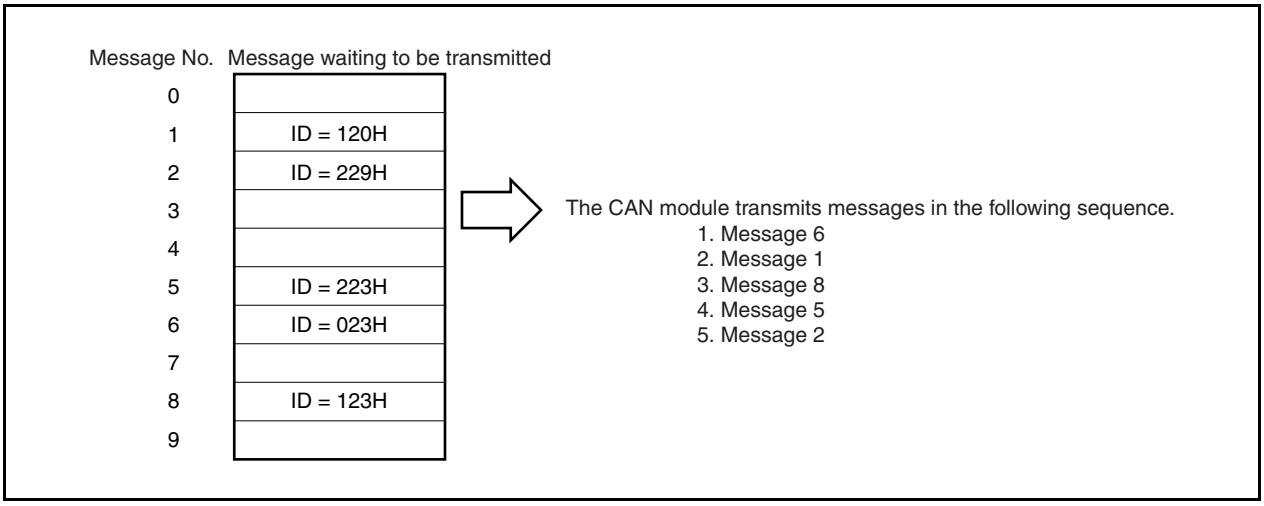
- Used as a message buffer
  (C0MCONFm.MA0 bit set to 1.)
- Set as a transmit message buffer
  (C0MCONFm.MT2 to C0MCONFm.MT0 bits set to 000B.)
- Ready for transmission
  (C0MCTRLm.RDY bit is set to 1.)

Remark m = 00 to 31

The CAN system is a multi-master communication system. In a system like this, the priority of message transmission is determined based on message identifiers (IDs). To facilitate transmission processing by software when there are several messages awaiting transmission, the CAN module uses hardware to check the ID of the message with the highest priority and automatically identifies that message. This eliminates the need for software-based priority control.

Transmission priority is controlled by the identifier (ID).

Figure 21-31. Message Processing Example

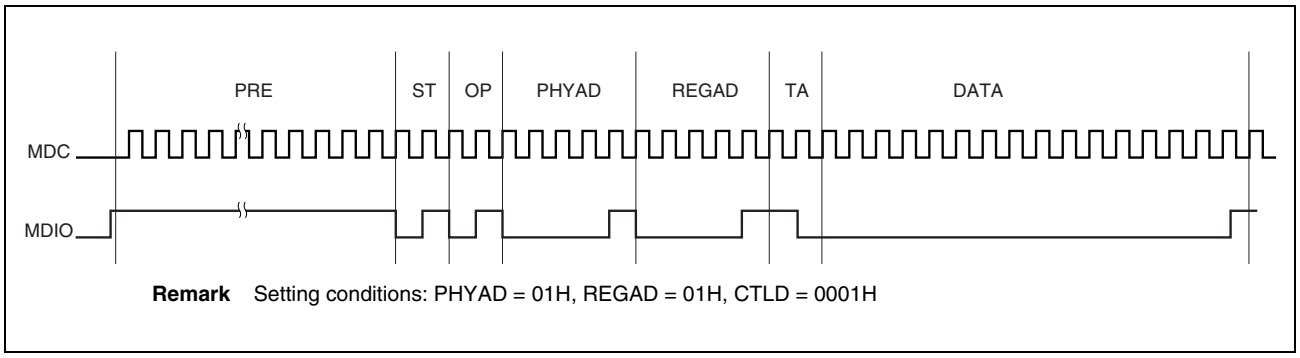


A 32-bit preamble, 2-bit start bit field, and 2-bit opcode, which indicates whether a register in the PHY device is read or written, are automatically appended to the serial management frame. PHYAD and REGAD indicate the address of the externally connected PHY device and the address of a register in that PHY device respectively. The values set to the MADR.FIAD and RGAD bits are appended to PHYAD and REGAD, respectively.

The Ethernet controller serially outputs data from the preamble to REGAD, and after a 2-bit turnaround, the data set to the CTLD bits of the MWTD register is output for a write access. For a read access, serial data is input by the MDI signal and written to the MRDD.PRSD bit.

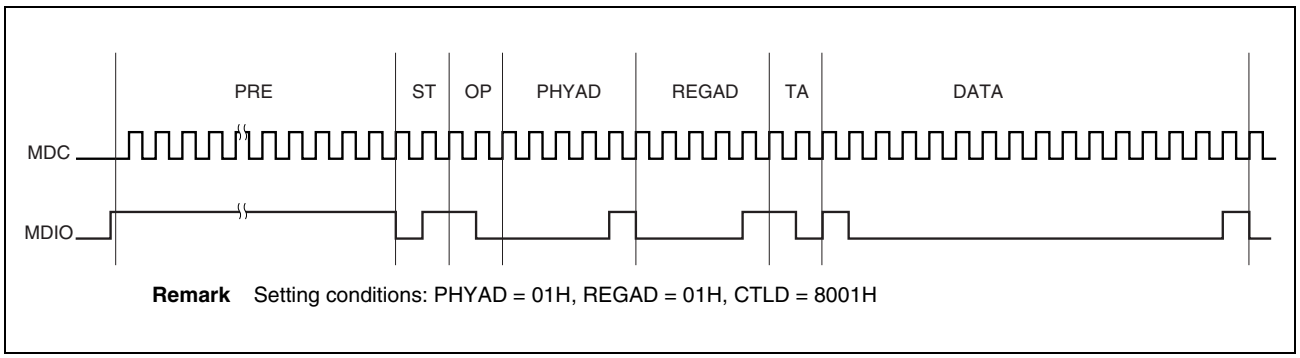
While the MDO signal is being output, the MDOEN signal is asserted to 1.

Figure 23-13. Timing of MII Management Interface Signal (Write Access)



Remark Setting conditions: PHYAD = 01H, REGAD = 01H, CTLD = 0001H

Figure 23-14. Timing of MII Management Interface Signal (Read Access)



Remark Setting conditions: PHYAD = 01H, REGAD = 01H, CTLD = 8001H

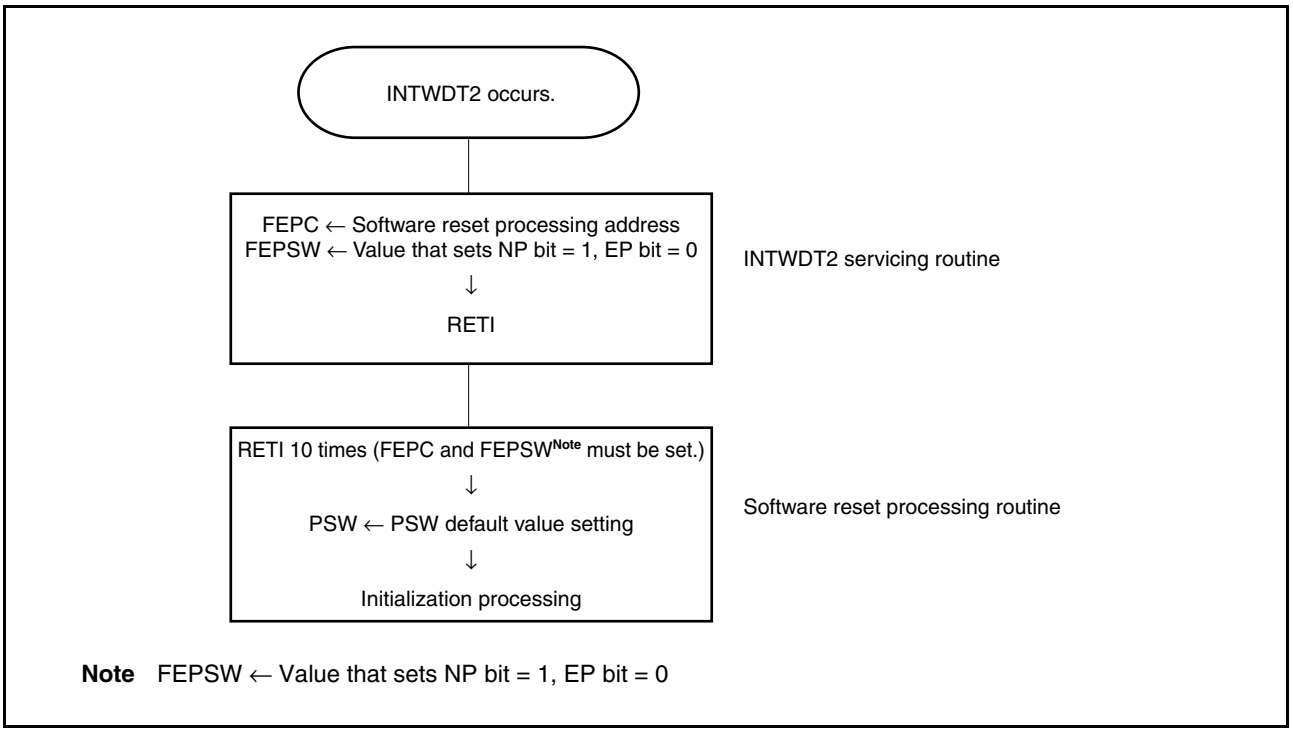
(c) SCAN command

The Ethernet controller has a SCAN command to successively read a specific PHY register. When the MCMD.SCANC bit is set to 1, read accesses are generated one after another. By reading the MRDD.PRSD bit, the specific PHY register can be polled.

(2) From INTWDT2 signal

Restoring from non-maskable interrupt servicing executed by the non-maskable interrupt request (INTWDT2) by using the RETI instruction is disabled. Execute the following software reset processing.

Figure 25-4. Software Reset Processing



Note FEPSW ← Value that sets NP bit = 1, EP bit = 0

25.2.3 NP flag

The NP flag is a status flag that indicates that non-maskable interrupt servicing is under execution.

This flag is set when a non-maskable interrupt request signal has been acknowledged, and masks non-maskable interrupt requests to prohibit multiple interrupts from being acknowledged.

After reset: 00000020H

	31 to 8	7	6	5	4	3	2	1	0
PSW	0	**NP**	EP	ID	SAT	CY	OV	S	Z

NP	NMI interrupt servicing status
0	No NMI interrupt servicing
1	NMI interrupt currently being serviced

25.3.5 Interrupt mask registers 0 to 7 (IMR0 to IMR7)

The IMR0 to IMR5 registers set the interrupt mask state for the maskable interrupts. The xxMKn bit of the IMR0 to IMR7 registers is equivalent to the xxICn.xxMKn bit.

The IMRm register can be read or written in 16-bit units.

If the higher 8 bits of the IMRm register are used as an IMRmH register and the lower 8 bits as an IMRmL register, these registers can be read or written in 8-bit or 1-bit units (m = 0 to 7).

Reset sets these registers to FFFFH.

Caution The device file defines the xxICn.xxMKn bit as a reserved word. If a bit is manipulated using the name of xxMKn, the contents of the xxICn register, instead of the IMRm register, are rewritten (as a result, the contents of the IMRm register are also rewritten).

(1/2)

After reset: 1FH R/W Address: FFFFF10EH

	7	6	5	4	3	2	1	0
IMR7L	0	0	0	1	1	1	TRXMK0 Note 1	RECMK0 Note 1

After reset: FFFFH R/W Address: IMR6 FFFFF10CH, IMR6L FFFFF10CH, IMR6H FFFFF10DH

	15	14	13	12	11	10	9	8
IMR6 (IMR6H Note 2)	WUPMK0 Note 1	ERRMK0 Note 1	ETPHYMK	ETBERMK	ETMOVMK	ETMRSMK	ETMTSMK	ETMFSMK

	7	6	5	4	3	2	1	0
IMR6L	ETMRQMK	ETMTXMK	ETMRXMK	UFMK1	UFMK0	RTC2MK	RTC1MK	RTC0MK

After reset: FFFFH R/W Address: IMR5 FFFFF10AH, IMR5L FFFFF10AH, IMR5H FFFFF10BH

	15	14	13	12	11	10	9	8
IMR5 (IMR5H Note 2)	KRMK	DMAMK3	DMAMK2	DMAMK1	DMAMK0	ADMK	IICMK4 Note 3	UC2TMK

	7	6	5	4	3	2	1	0
IMR5L	UC2RMK/ IICMK2	CF6TMK/ UC7TMK Note 3	CF6RMK/ UC7RMK Note 3	CF5TMK/ UC6TMK Note 3	CF5RMK/ UC6RMK Note 3	UB0TITOMK	UB0TIREMK	UB0TIFMK

After reset: FFFFH R/W Address: IMR4 FFFFF108H, IMR4L FFFFF108H, IMR4H FFFFF109H

	15	14	13	12	11	10	9	8
IMR4 (IMR4H Note 2)	CF4TMK/ UB0TITMK	CF4RMK/ UB0TIRMK	UB1TITOMK	UB1TIREMK	UB1TIFMK	CF3TMK/ UB1TITMK	CF3RMK/ UB1TIRMK	CF2TMK/ UC0TMK

	7	6	5	4	3	2	1	0
IMR4L	CF2RMK/ UC0RMK	CF1TMK/ UC1TMK	CF1RMK/ UC1RMK/ IICMK0	CF0TMK/ UC3TMK	CF0RMK/ UC3RMK/ IICMK1	CE1TI0FMK/ UC5TMK	CE1TMK/ UC5RMK/ IICMK3	CE0TI0FMK/ UC4TMK

Notes 1. μPD70F3783, 70F3786 only

2. To read bits 8 to 15 of the IMR6 to IMR4 registers in 8-bit or 1-bit units, specify them as bits 0 to 7 of IMR6H to IMR4H registers.

3. V850ES/JJ3-E only

Cautions 1. Set bits 7 to 5 of the IMR7 register to "0" and bits 4 to 2 to "1". If the setting of these bits is changed, the operation is not guaranteed.

2. Do not read or write the IMR7 register in 16-bit units.

Remark xx: Identification name of each peripheral unit (see **Table 25-4 Interrupt Control Register (xxICn)**).

n: Peripheral unit number (see **Table 25-4 Interrupt Control Register (xxICn)**)

(T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	P02, P03, P20 to P27, P30 to P37 P40 to P48, P50 to P59, P90 to P915	Per pin	4	mA
			Total of all pins	50	mA
		PCM0 to PCM3, PCS0, PCS2, PCS3 PCT0, PCT1, PCT4, PCT6 PDL0 to PDL15, PDH0 to PDH7	Per pin	4	mA
			Total of all pins	50	mA
		UDMF, UDPF	Per pin	4	mA
			Total of all pins	8	mA
		P70 to P711	Per pin	4	mA
			Total of all pins	20	mA
Output current, high	I_{OH}	P02, P03, P20 to P27, P30 to P37 P40 to P48, P50 to P59, P90 to P915	Per pin	–4	mA
			Total of all pins	–50	mA
		PCM0 to PCM3, PCS0, PCS2, PCS3 PCT0, PCT1, PCT4, PCT6 PDL0 to PDL15, PDH0 to PDH7	Per pin	–4	
			Total of all pins	–8	
		UDMF, UDPF	Per pin	–4	mA
			Total of all pins	–8	mA
		P70 to P711	Per pin	–4	mA
			Total of all pins	–20	mA
Operating ambient temperature	T_A	In normal operation		–40 to +85	°C
		In flash memory programming		–40 to +85	°C
Storage temperature	T_{stg}			–40 to +125	°C

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage. Therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

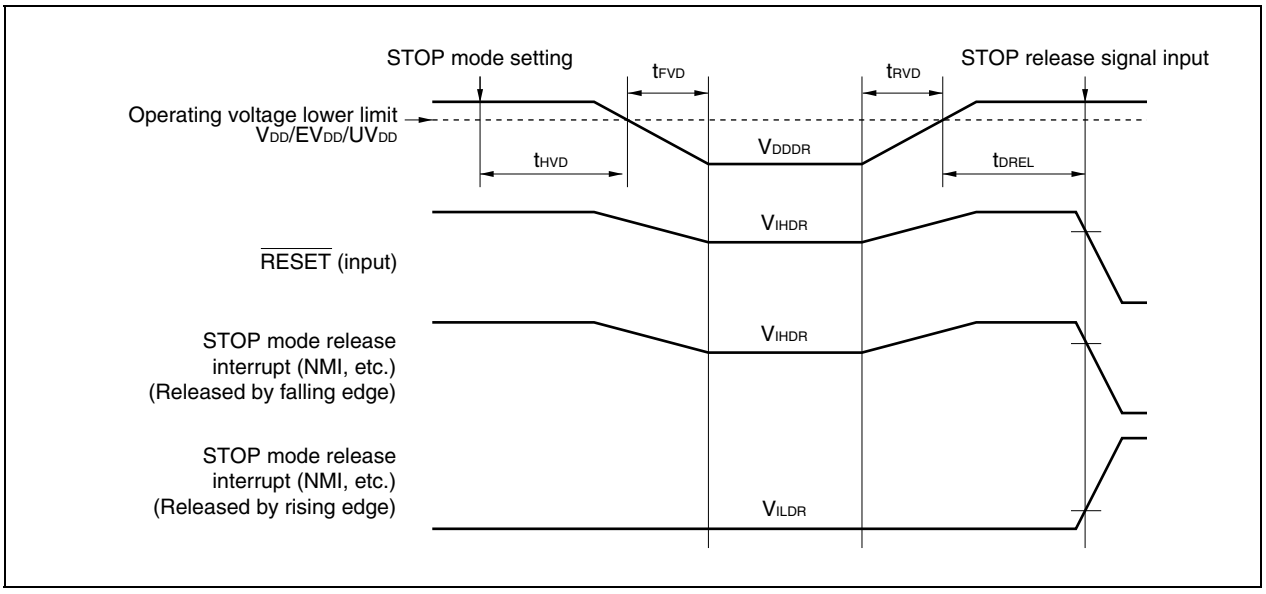
35.6 Data Retention Characteristics

(1) In STOP mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0}, V_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode (all functions stopped)	1.9		3.6	V
Data retention current	I_{DDDR}	STOP mode (all functions stopped), V_{DDDR} = 2.0 V		10	135	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage retention time	t_{HVD}	After STOP mode setting	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches 2.85 V (MIN.)	0			ms
Data retention input voltage, high	V_{IHDR}	V_{DD} = EV_{DD} = UV_{DD} = V_{DDDR}	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	V_{DD} = EV_{DD} = UV_{DD} = V_{DDDR}	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.



APPENDIX B MAJOR DIFFERENCES BETWEEN V850ES/Jx3-E AND V850ES/Jx3-H

Table B-1. Major Differences Between V850ES/Jx3-E and V850ES/Jx3-H

Major Difference	V850ES/Jx3-E	V850ES/Jx3-H
Minimum instruction execution time	20 ns (50 MHz operation)	20.8 ns (48 MHz operation)
Maximum RAM size	60 KB + 64 KB[Note]	48 KB + 8 KB[Note]
D/A controller	None	Available
Ethernet controller	Available	None
Asynchronous serial interface	UARTC: 6/8 ch	UARTC: 5 ch
	UARTB(UART with FIFO function): 2 ch	None
Clocked serial interface	CSIE (CSI with FIFO function): 2 ch	None
I^2C	4/5 ch	3 ch
Package	128-pin LQFP 144-pin LQFP	100-pin LQFP 128-pin LQFP

Note Data-only RAM

(6/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	00000000010RRRRR	adr←(PC+2) + (GR [reg1] logically shift left by 1) PC←(PC+2) + (sign-extend (Load-memory (adr,Halfword)) logically shift left by 1	5	5	5					
SXB	reg1	00000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0))	1	1	1					
SXH	reg1	00000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	0000011111iiiii 0000000100000000	EIPC ←PC+4 (Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR dddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit (adr,bit#3))	3 Note3	3 Note3	3 Note3				×	
	reg2, [reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not (Load-memory-bit (adr,reg2))	3 Note3	3 Note3	3 Note3				×	
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	00000000100RRRRR	GR[reg1]←zero-extend (GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	00000000110RRRRR	GR[reg1]←zero-extend (GR[reg1] (15 : 0))	1	1	1					

Notes 1. ddddddddd: Higher 8 bits of disp9.

2. 3 if there is an instruction that rewrites the contents of the PSW immediately before.

3. If there is no wait state (3 + the number of read access wait states).

4. n is the total number of list12 load registers. (According to the number of wait states. Also, if there are no wait states, n is the total number of list12 registers. If n = 0, same operation as when n = 1)

5. RRRRR: other than 00000.

6. The lower halfword data only are valid.

7. ddddddddddddddddddddd: The higher 21 bits of disp22.

8. ddddddddddddddd: The higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states).

10. b: bit 0 of disp16.

11. According to the number of wait states (2 if there are no wait states).