Renesas Electronics America Inc - UPD70F3781GF-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	124K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3781gf-gat-ax

(3) Port 9 mode control register (PMC9)

(1/2)

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H)	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	$\overline{\text{SCKF3}}$ I/O/TIAA51 input/TOAA51 output/A15 output

PMC914	Specification of P914 pin operation mode
0	I/O port
1	SOF3 output/RXDB1 input/INTP20 input/A14 output

PMC913	Specification of P913 pin operation mode
0	I/O port
1	SIF3 input/TXDB1 output/INTP19 input/A13 output

PMC912	Specification of P912 pin operation mode
0	I/O port
1	TOAB1OFF input/INTP18 input/A12 output

PMC911	Specification of P911 pin operation mode
0	I/O port
1	$\overline{\text{SCKE1}}$ I/O/TIAA50 input/TOAA50 output/A11 output

PMC910	Specification of P910 pin operation mode
0	I/O port
1	SOE1 output/RXDC5 input/SCL03 I/O/A10 output

PMC99	Specification of P99 pin operation mode
0	I/O port
1	SIE1 input/TXDC5 output/SDA03 I/O/A9 output

PMC98	Specification of P98 pin operation mode
0	I/O port
1	TENC01 input/INTP17 input/A8 output

Remarks 1. The PMC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMC9 register as the PMC9H register and the lower 8 bits as the PMC9L register, they can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMC9H register.

(8) TMT0 option register 0 (TT0OPT0)

The TT0OPT0 register is an 8-bit register that sets the capture/compare operation and detects overflows.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF607H

	7	6	5	4	3	2	1	<0>
TT0OPT0	0	0	TT0CCS1	TT0CCS0	0	0	0	TT0OVF

TT0CCS1	TT0CCR1 register capture/compare selection
0	Selected as compare register
1	Selected as capture register (cleared by the TT0CTL0.TT0CE bit = 0)
The TT0CCS1 bit setting is valid only in the free-running timer mode.	

TT0CCS0	TT0CCR0 register capture/compare selection
0	Selected as compare register
1	Selected as capture register (cleared by the TT0CTL0.TT0CE bit = 0)
The TT0CCS0 bit setting is valid only in the free-running timer mode.	

TT0OVF	TMT0 overflow detection flag
Set (1)	Overflow occurred
Reset (0)	0 written to TT0OVF bit or TT0CTL0.TT0CE bit = 0

- The TT0OVF bit is set to 1 when the 16-bit counter value overflows from FFFFH to 0000H in the free-running timer mode or the pulse width measurement mode.
- An overflow interrupt request signal (INTTT0OV) is generated when the TT0OVF bit is set to 1. The INTTT0OV signal is not generated in modes other than the free-running timer mode and the pulse width measurement mode.
- The TT0OVF bit is not cleared to 0 even when the TT0OVF bit or the TT0OPT0 register are read when the TT0OVF bit = 1.
- Before clearing the TT0OVF bit to 0 after generation of the INTTT0OV signal, be sure to confirm (by reading) that the TT0OVF bit is set to 1.
- The TT0OVF bit can be both read and written, but the TT0OVF bit cannot be set to 1 by software. Writing 1 has no effect on the operation of TMT0.

Cautions 1. Rewrite the TT0CCS1 and TT0CCS0 bits when the TT0CE bit = 0. (The same value can be written when the TT0CE bit = 1.) If rewriting was mistakenly performed, clear the TT0CE bit to 0 and then set these bits again.

2. Be sure to set bits 1 to 3, 6, and 7 to "0".

(e) Set the TAA4CE bit to 1 and set the TAB1CE bit to 1 immediately after that to start the 6-phase PWM output operation

Rewriting the TAB1CTL0, TAB1CTL1, TAB1IOC1, TAB1IOC2, TAA4CTL0, and TAA4CTL1 registers is prohibited during operation. The operation and the PWM output waveform are not guaranteed if any of these registers is rewritten during operation. However, rewriting the TAB1CTL0.TAB1CE bit to clear it is permitted. Manipulating (reading/writing) the other TAB1, TAA4, and TAB1 option registers is prohibited until the TAA4CTL0.TAA4CE bit is set to 1 and then the TAB1CE bit is set to 1.

(2) Tuning operation clearing procedure

To clear the tuning operation and exit the 6-phase PWM output mode, set the TAA4 and TAB1 registers using the following procedure.

<1> Clear the TAB1CTL0.TAB1CE bit to 0 and stop the timer operation.
<2> Clear the TAA4CTL0.TAA4CE bit to 0 so that TAA4 can be separated.
<3> Stop the timer output by using the TAB1IOC0 register.
<4> Clear the TAA4CTL1.TAA4SYE bit to 0 to clear the tuning operation.

Caution Manipulating (reading/writing) the other TAB1, TAA4, and TAB1 option registers is prohibited until the TAB1CE bit is set to 1 and then the TAA4CE bit is set to 1.

(3) When not tuning TAA4

When the match interrupt signal of TAA4 is not necessary as the conversion trigger source that starts the A/D converter, TAA4 can be used independently as a separate timer without being tuned. In this case, the match interrupt signal of TAA4 cannot be used as a trigger source to start A/D conversion in the 6-phase PWM output mode. Therefore, fix the TAB1OPT2.TAB1AT0 to TAB1OPT2.TAB1AT3 bits to 0.

The other control bits can be used in the same manner as when TAA4 is tuned.

If TAA4 is not tuned, the compare registers (TAA4CCR0 and TAA4CCR1) of TAA4 are not affected by the setting of the TAB1OPT0.TAB1CMS and TAB1OPT2.TAB1RDE bit. For the initialization procedure when TAA4 is not tuned, see (b) to (e) in **11.4.5 (1) Tuning operation starting procedure**. (a) is not necessary because it is a step used to set TAA4 for the tuning operation.

(4) Basic operation of TAA4 during tuning operation

The 16-bit counter of TAA4 only counts up. The 16-bit counter is cleared by the set cycle value of the TAB1CCR0 register and starts counting from 0000H again. The count value of this counter is the same as the value of the 16-bit counter of TAB1 when it counts up. However, it is not the same when the 16-bit counter of TAA4 counts down.

- When TAB1 counts up (same value)
  16-bit counter of TAB1: 0000H → M (counting up)
  16-bit counter of TAA4: 0000H → M (counting up)
- When TAB1 counts down (not same value)
  16-bit counter of TAB1: M + 1 → 0001H (counting down)
  16-bit counter of TAA4: 0000H → M (counting up)

(2) Pending mode/pointer mode

The pending mode or pointer mode can be selected by using the UBnFIC0.UBnITM and UBnFIC0.UBnIRM bits in the FIFO mode (UBnFIC0.UBnMOD bit = 1).

If transmission is started by writing data of more than double the amount set as the trigger by the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits to transmit FIFO, the transmission enable interrupt request signal (INTUBnTIT) may occur more than once. The reception end interrupt request signal (INTUBnTIR) may also occur more than once if the number of receive data set as the trigger by the UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits is 8 bytes or less in receive FIFO. In the pending or pointer mode, it can be specified how an interrupt is handled after it has been held pending.

(a) Pending mode

(i) During transmission (writing to transmit FIFO)

- If the data of the first transmission enable interrupt request signal (INTUBnTIT) is not written to transmit FIFO after the interrupt has occurred, the second INTUBnTIT signal does not occur (is held pending) even if the generation condition of the second INTUBnTIT signal is satisfied (when transmit data of the number set as the trigger by the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits is transferred from transmit FIFO to the transmit shift register).

  When data for the first INTUBnTIT signal is later written to transmit FIFO, the pending INTUBnTIT signal is generated[Note].

  Note The number of pending interrupts is as follows.

  When trigger is set to 1 byte (UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits = 0000): 15 times max.
  When trigger is set to 2 bytes (UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits = 0001): 7 times max.
  :
  When trigger is set to 6 bytes (UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits = 0101): 1 time max.
  When trigger is set to 7 bytes (UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits = 0110): 1 time max.
  When trigger is set to 8 bytes (UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits = 0111): 1 time max.

- In the pending mode, transmit data of the number set as the trigger by the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits is always written to transmit FIFO when the transmission enable interrupt request signal (INTUBnTIT) occurs. Writing data to transmit FIFO is prohibited if the data is more or less than the specified number. If data more or less than the specified number is written, the operation is not guaranteed.
- Fix the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits to 0000 (set number of transmit data: 1 byte) to write transmit data to transmit FIFO by DMA. If any other setting is made, the operation is not guaranteed.

Remark n = 0, 1

17.3.5 Mode switching between UARTC4 and CSIE0

In the V850ES/JH3-E and V850ES/JJ3-E, UARTC4 and CSIE0 share of the same pin and therefore cannot be used simultaneously. Set UARTC4 in advance, using the PMC4, PFC4, and PFCE4 registers, before use.

Caution The transmit/receive operation of UARTC4 and CSIE0 is not guaranteed if these functions are switched during transmission or reception. Be sure to disable the one that is not used.

Figure 17-6. UARTC4 and CSIE0 Mode Switch Settings

After reset: 0000H R/W Address: PMC4 FFFFF448H,
PMC4L FFFFF448H, PMC4H FFFFF449H

	15	14	13	12	11	10	9	8
PMC4	0Note	0Note	0Note	0Note	0Note	0Note	0Note	PMC48Note

7	6	5	4	3	2	1	0
PMC47Note	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40

After reset: 0000H R/W Address: PFC4 FFFFF468H,
PFC4L FFFFF468H, PFC4H FFFFF469H

	15	14	13	12	11	10	9	8
PFC4	0Note	0Note	0Note	0Note	0Note	0Note	0Note	PFC48Note

7	6	5	4	3	2	1	0
PFC47Note	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40

After reset: 00H R/W Address: FFFFF708H

	7	6	5	4	3	2	1	0
PFCE4	PFCE47Note	PFCE46Note	PFCE45	PFCE44	PFCE43	PFCE42	PFCE41	PFCE40

PMC45	PFCE45	PFC45	Operation mode
0	×	×	Port I/O mode
1	0	0	$\overline{\text{SCKE0}}$ (CSIE0)

PMC44	PFCE44	PFC44	Operation mode
0	×	×	Port I/O mode
1	0	0	SOE0 (CSIE0)
1	0	1	RXDC4 (UARTC4)

PMC43	PFCE43	PFC43	Operation mode
0	×	×	Port I/O mode
1	0	0	SIE0 (CSIE0)
1	0	1	TXDC4 (UARTC4)

Note V850ES/JJ3-E only

Remark × = don't care

Therefore, the maximum baud rate that can be received by the destination is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} \text{ Brate}$$

Similarly, obtaining the following maximum allowable transfer rate yields the following.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k + 2}{2 \times k} \times FL = \frac{21k - 2}{2 \times k} FL$$

$$FLmax = \frac{21k - 2}{20\ k} FL \times 11$$

Therefore, the minimum baud rate that can be received by the destination is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 2} \text{ Brate}$$

Obtaining the allowable baud rate error for UARTCn and the destination from the above-described equations for obtaining the minimum and maximum baud rate values yields the following.

Table 17-5. Maximum/Minimum Allowable Baud Rate Error

Division Ratio (k)	Maximum Allowable Baud Rate Error	Minimum Allowable Baud Rate Error
4	+2.32%	–2.43%
8	+3.52%	–3.61%
20	+4.26%	–4.30%
50	+4.56%	–4.58%
100	+4.66%	–4.67%
255	+4.72%	–4.72%

Remarks 1. The reception accuracy depends on the bit count in 1 frame, the input clock frequency, and the division ratio (k). The higher the input clock frequency and the larger the division ratio (k), the higher the accuracy.

2. k: Set value of UCnCTL2.UCnBRS7 to UCnCTL2.UCnBRS0 bits

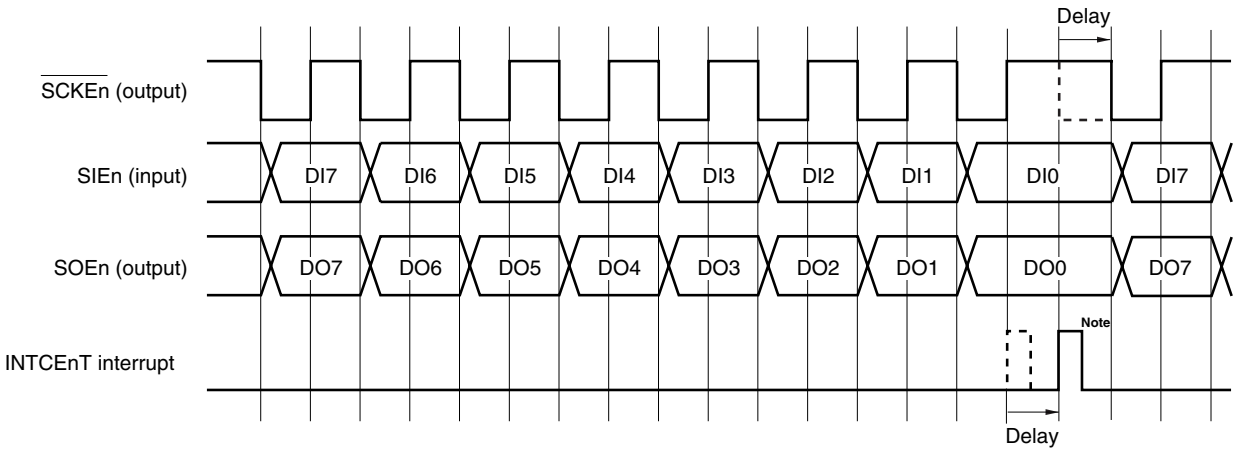
3. n = 0 to 5 (V850ES/JH3-E)
n = 0 to 7 (V850ES/JJ3-E)

(14) Delay control of transmission/reception completion interrupt (INTCEnT)

In the master mode (CEnCTL1.CEnCKS2 to CEnCTL1.CEnCKS0 bits = other than 111), occurrence of the transmission/reception completion interrupt (INTCEnT) can be delayed by half a clock (1/2 serial clock), depending on the setting (1) of the CEnCTL0.CEnTMS bit. The CEnSIT bit is valid only in the master mode. In the slave mode (CEnCTL1.CEnCKS2 to CEnCTL1.CEnCKS0 bits = 111), setting the CEnSIT bit to 1 is prohibited (even if set, the INTCEnT interrupt is not affected).

Caution If the CEnCTL0.CEnTMS bit is set to 1 in the continuous mode (CEnCTL0.CEnTMS bit = 1), the INTCEnT interrupt is not output at the end of data other than the last data set by the CEnCTL3.CEnSFN3 to CEnCTL3.CEnSFN0 bits, but a delay of half a clock (1/2 serial clock) can be inserted between each data transfer.

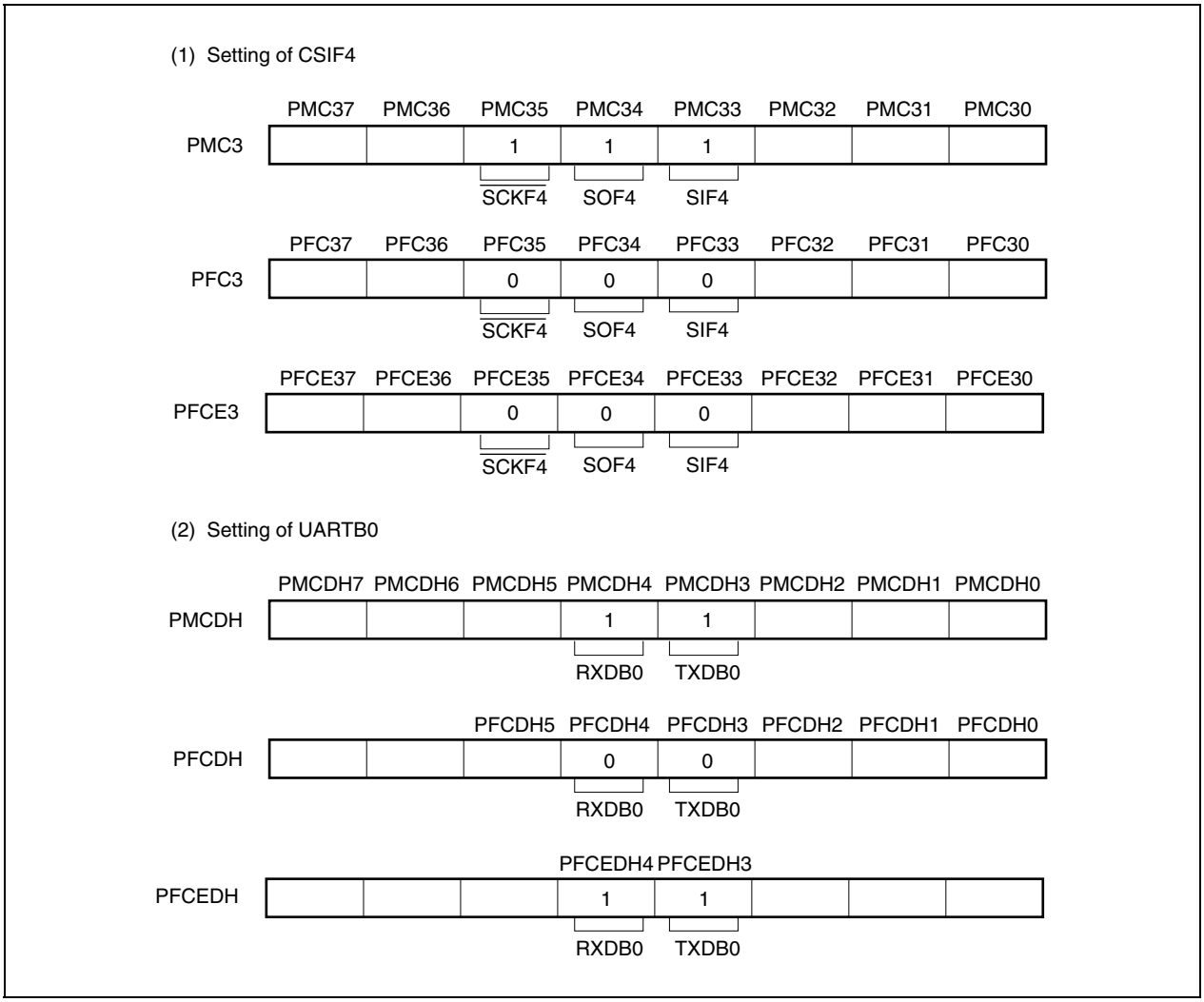
Figure 18-12. Delay Control of Transmission/Reception Completion Interrupt (INTCEnT): CEnCTL0.CEnSIT Bit = 1, CEnCKP, CEnDAP Bits = 00, CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 Bits = 1000 (Transfer Data Length: 8 Bits)



Note If the CEnCTL0.CEnTMS bit is set to 1 in the continuous mode (CEnCTL0.CEnTMS bits = 1), the INTCEnT interrupt is not output at the end of data other than the last data set by the CEnCTL3.CEnSFN3 to CEnCTL3.CEnSFN0 bits, but a delay of half a clock (1/2 serial clock) can be inserted between each data transfer.

Remark n = 0, 1

Figure 19-6. CSIF4 and UARTB0 Mode Switch Settings

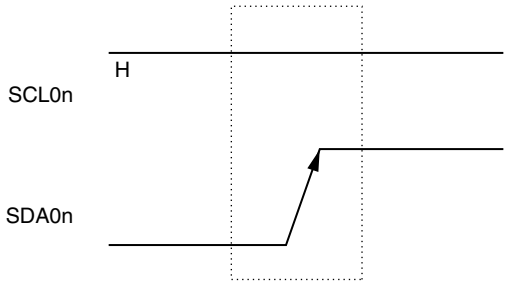


20.6.5 Stop condition

When the SCL0n pin is high level, changing the SDA0n pin from low level to high level generates a stop condition.

A stop condition is generated when serial transfer from the master device to the slave device has been completed. When the V850ES/JH3-E or V850ES/JJ3-E is used as the slave device, it can detect the stop condition.

Figure 20-13. Stop Condition



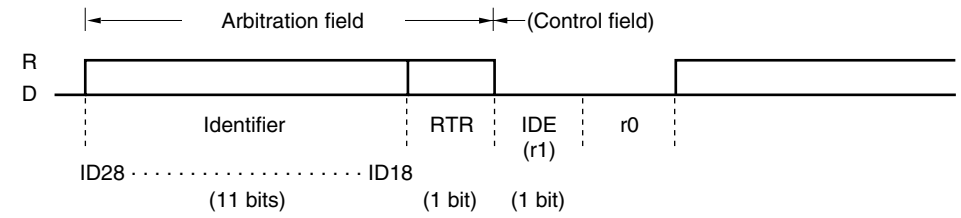
Remark n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

A stop condition is generated when the IICCn.SPTn bit is set to 1. When the stop condition is detected, the IICSn.SPDn bit is set to 1 and the interrupt request signal (INTIICn) is generated when the IICCn.SPIEn bit is set to 1.

<2> Arbitration field

The arbitration field is used to set the priority, data frame/remote frame, and frame format.

Figure 21-6. Arbitration Field (in Standard Format Mode)



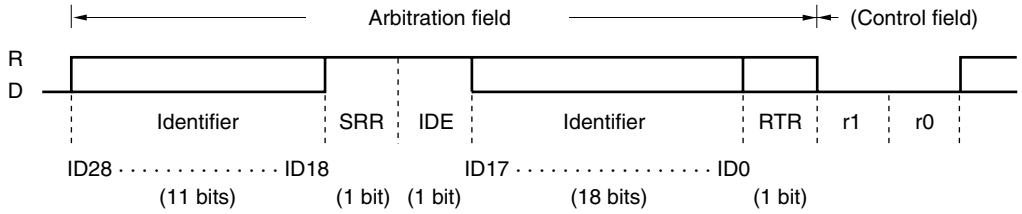
Cautions 1. ID28 to ID18 are identifiers.

2. An identifier is transmitted MSB first.

Remark D: Dominant = 0

R: Recessive = 1

Figure 21-7. Arbitration Field (in Extended Format Mode)



Cautions 1. ID28 to ID18 are identifiers.

2. An identifier is transmitted MSB first.

Remark D: Dominant = 0

R: Recessive = 1

Table 21-3. RTR Frame Settings

Frame Type	RTR Bit
Data frame	0 (D)
Remote frame	1 (R)

Table 21-4. Frame Format Setting (IDE Bit) and Number of Identifier (ID) Bits

Frame Format	SRR Bit	IDE Bit	Number of Bits
Standard format mode	None	0 (D)	11 bits
Extended format mode	1 (R)	1 (R)	29 bits

(4/4)

Set PSMODE0	Clear PSMODE0	Setting of PSMODE0 bit
0	1	PSMODE0 bit is cleared to 0.
1	0	PSMODE bit is set to 1.
Other than above		PSMODE0 bit is not changed.

Set PSMODE1	Clear PSMODE1	Setting of PSMODE1 bit
0	1	PSMODE1 bit is cleared to 0.
1	0	PSMODE1 bit is set to 1.
Other than above		PSMODE1 bit is not changed.

Set OPMODE0	Clear OPMODE0	Setting of OPMODE0 bit
0	1	OPMODE0 bit is cleared to 0.
1	0	OPMODE0 bit is set to 1.
Other than above		OPMODE0 bit is not changed.

Set OPMODE1	Clear OPMODE1	Setting of OPMODE1 bit
0	1	OPMODE1 bit is cleared to 0.
1	0	OPMODE1 bit is set to 1.
Other than above		OPMODE1 bit is not changed.

Set OPMODE2	Clear OPMODE2	Setting of OPMODE2 bit
0	1	OPMODE2 bit is cleared to 0.
1	0	OPMODE2 bit is set to 1.
Other than above		OPMODE2 bit is not changed.

22.2.2 USB memory map

The USB function controller seen from the CPU is assigned to the CS1 space in the microcontroller. The memory space is divided for use as follows.

Table 22-1. Division of CPU Memory Space

Address	Area	
00200000H to 00200092H	EPC control register area	
00200100H to 00200114H	EPC data hold register area	
00200144H to 002003C4H	EPC request data register area	
00200400H to 00200408H	Bridge register area	
00200500H to 0020050EH	DMA register area	
00201000H	Bulk-in register area	EP1 (Bulk-IN1)
00202000H		EP3 (Bulk-IN2)
00210000H	Bulk-out register area	EP2 (Bulk-Out1)
00220000H		EP4 (Bulk-Out2)
00240000H	Peripheral control register area	

(5) UF0 bulk-out 1 register (UF0BO1)

The UF0BO1 register is a 64-byte × 2 FIFO that stores data for Endpoint2. This register consists of two banks of 64-byte FIFOs each of which performs a toggle operation and repeatedly connects the buses on the SIE and CPU sides. The toggle operation takes place when data is in the FIFO on the SIE side and when no data is in the FIFO on the CPU side (counter value = 0).

This register is read-only, in 8-bit units. A write access to this register is ignored.

When the hardware receives data for Endpoint2 from the host, it automatically transfers the data to the UF0BO1 register. When the register correctly receives the data, a FIFO toggle operation occurs. As a result, the BKO1DT bit of the UF0IS3 register is set to 1, the quantity of the received data is held by the UF0BO1L register, and an interrupt request or DMA request is issued to the CPU. Whether the interrupt request or DMA request is issued can be selected by using the DQBO1MS bit of the UF0IDR register.

Read the data held by the UF0BO1 register by FW, up to the value of the amount of data read by the UF0BO1L register. When the correct received data is held by the FIFO connected to the SIE side and the value of the UF0BO1L register reaches 0, the toggle operation of the FIFO occurs, and the BKO1NK bit of the UF0EN register is automatically cleared to 0. If data greater than the value of the UF0BO1L register is read and if the FIFO toggle condition is satisfied, the toggle operation of the FIFO occurs. As a result, the next packet may be read by mistake. Note that, if the toggle condition is not satisfied, the first data is repeatedly read.

If overrun data is received while data is held by the FIFO connected to the CPU side, Endpoint2 stalls, and the FIFO on the CPU side is cleared.

When the UF0BO1 register is read while no data is in it, an undefined value is read.

Caution Be sure to read all the data stored in this register.

	7	6	5	4	3	2	1	0	Address	After reset
UF0BO1	BKO17	BKO16	BKO15	BKO14	BKO13	BKO12	BKO11	BKO10	00200108H	Undefined

Bit position	Bit name	Function
7 to 0	BKO17 to BKO10	These bits store data for Endpoint2.

The operation of the UF0BO1 register is illustrated below.

(12) UF0 descriptor length register (UF0DSCL)

This register stores the length of the value that is to be returned in response to the GET_DESCRIPTOR Configuration request. The value of this register is the number of bytes of all the descriptors set by the UF0CIEn register minus 1 (n = 0 to 255). The total descriptor length that is to be returned in response to the GET_DESCRIPTOR Configuration request is determined according to the value of this register.

This register can be read or written in 8-bit units. However, data can be written to this register only when the EP0NKA bit is set to 1.

Processing of wLength is automatically controlled. If this register is set to 00H, it means that the descriptor to be returned is 1 byte long. If the register is set to FFH, a descriptor length of 256 bytes is returned. When a descriptor exceeding 256 bytes in length is used, set the CDCGDST bit of the UF0MODC register to 1 and process the GET_DESCRIPTOR request by FW (at this time, the CDCGD bit of the UF0MODS register is also set to 1).

Caution To rewrite this register, set the EP0NKA bit to 1 before reading the register contents, and rewrite the register contents after confirming that the bit has been set, in order to prevent conflict between a read access and a write access.

	7	6	5	4	3	2	1	0	Address	After reset
UF0DSCL	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0	002001A0H	00H

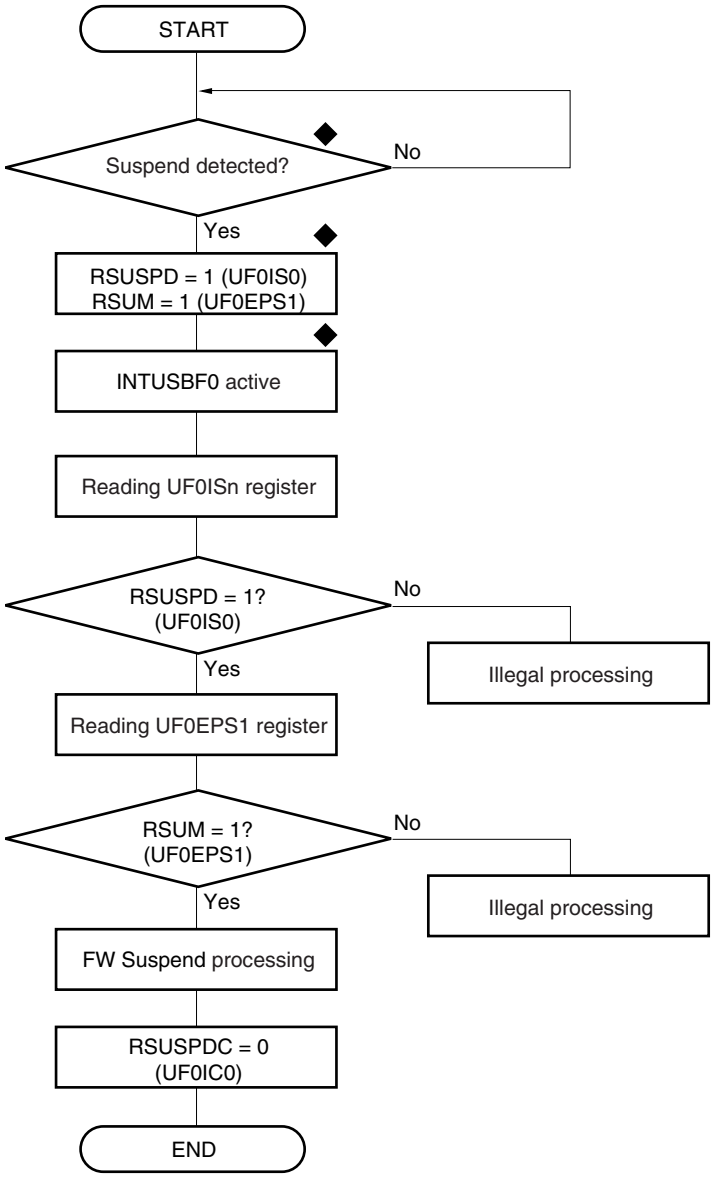
Bit position	Bit name	Function
7 to 0	DPL7 to DPL0	These bits set the value of the number of bytes of all the descriptors to be returned in response to the GET_DESCRIPTOR Configuration request minus 1.

22.9.4 Suspend/Resume processing

How Suspend/Resume processing is performed differs depending on the configuration of the system. One example is given below.

Figure 22-30. Example of Suspend/Resume Processing (1/3)

(a) Example of Suspend processing



Remarks 1. n = 0, 1

2. ♦: Processing by hardware

(11) Read values of DSAn and DDAn registers

Values in the middle of updating may be read from the DSAn and DDAn registers during DMA transfer (n = 0 to 3). For example, if the DSAnH register and then the DSAnL register are read when the DMA transfer source address (DSAn register) is 0000FFFFH and the count direction is incremental (DADCn.SAD1 and DADCn.SAD0 bits = 00), the value of the DSAn register differs as follows, depending on whether DMA transfer is executed immediately after the DSAnH register is read.

(a) If DMA transfer does not occur while DSAn register is read

<1> Read value of DSAnH register: DSAnH = 0000H

<2> Read value of DSAnL register: DSAnL = FFFFH

(b) If DMA transfer occurs while DSAn register is read

<1> Read value of DSAnH register: DSAnH = 0000H

<2> Occurrence of DMA transfer

<3> Incrementing DSAn register: DSAn = 00100000H

<4> Read value of DSAnL register: DSAnL = 0000H

(2) Releasing HALT mode by reset

The same operation as the normal reset operation is performed.

Table 27-3. Operating Status in HALT Mode

Item \ Setting of HALT Mode		Operating Status	
		When Subclock Is Not Used	When Subclock Is Used
Main clock oscillator (f_X)		Oscillation enabled	
Subclock oscillator (f_{XT})		–	Oscillation enabled
Internal oscillator (f_R)		Oscillation enabled	
PLL		Operable	
CPU		Stops operation	
DMA controller		Operable	
Interrupt controller		Operable	
Timer	TAA0 to TAA5	Operable	
	TAB0, TAB1	Operable	
	TMM0 to TMM3	Operable when a clock other than f_{XT} is selected as the count clock	Operable
	TMT0	Operable	
Real-time counter (RTC)		Operable when f_X (divided BRG) is selected as the count clock	Operable
Watchdog timer (WDT2)		Operable when a clock other than f_{XT} is selected as the count clock	Operable
Serial interface	CSIFn	Operable (n = 0 to 4: V850ES/JH3-E, n = 0 to 6: V850ES/JJ3-E)	
	CSIE0, CSIE1	Operable	
	I^2C0m	Operable (m = 0 to 3: V850ES/JH3-E, m = 0 to 4: V850ES/JJ3-E)	
	UARTCx	Operable (x = 0 to 5: V850ES/JH3-E, x = 0 to 7: V850ES/JJ3-E)	
	UARTB0, UARTB1	Operable	
A/D converter		Operable	
Real-time output function (RTO)		Operable	
Key interrupt function (KR)		Operable	
CRC operation circuit		Operable (No data input to the CRCIN register because the CPU is stopped)	
External bus interface		See **CHAPTER 5 BUS CONTROL FUNCTION**.	
Port function		Retains status before HALT mode was set	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the HALT mode was set.	
CAN[Note]		Operable	
USB function		Operable	
Ethernet controller		Operable	

Note μPD70F3783, 70F3786 only

33.4.6 Pin connection

When performing on-board writing, mount a connector on the target system to connect to the dedicated flash programmer. Also, incorporate a function on-board to switch from the normal operation mode to the flash memory programming mode.

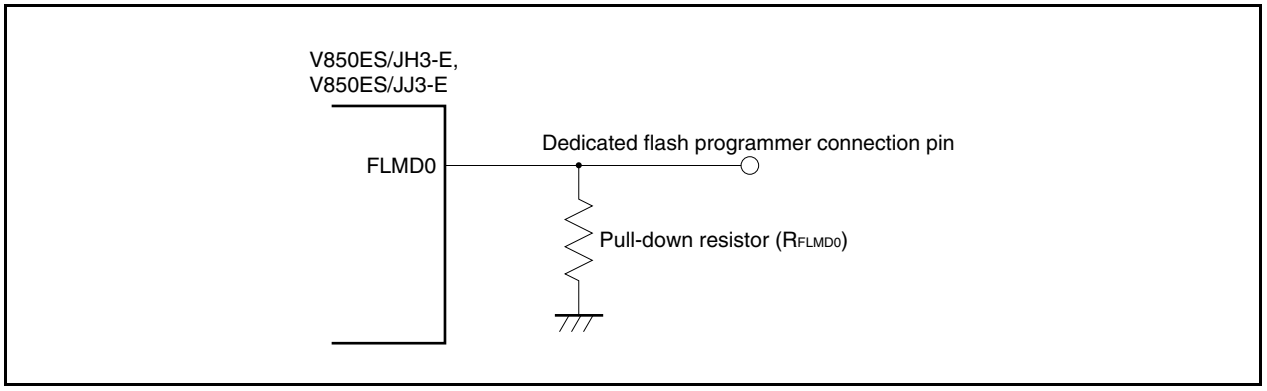
In the flash memory programming mode, all the pins not used for flash memory programming become the same status as that immediately after reset. Therefore, pin handling is required when the external device does not acknowledge the status immediately after a reset.

(1) FLMD0 pin

In the normal operation mode, input a voltage of V_{SS} level to the FLMD0 pin. In the flash memory programming mode, supply a write voltage of V_{DD} level to the FLMD0 pin.

Because the FLMD0 pin serves as a write protection pin in the self programming mode, a voltage of V_{DD} level must be supplied to the FLMD0 pin via port control, etc., before writing to the flash memory. For details, see **33.5.5 (1) FLMD0 pin**.

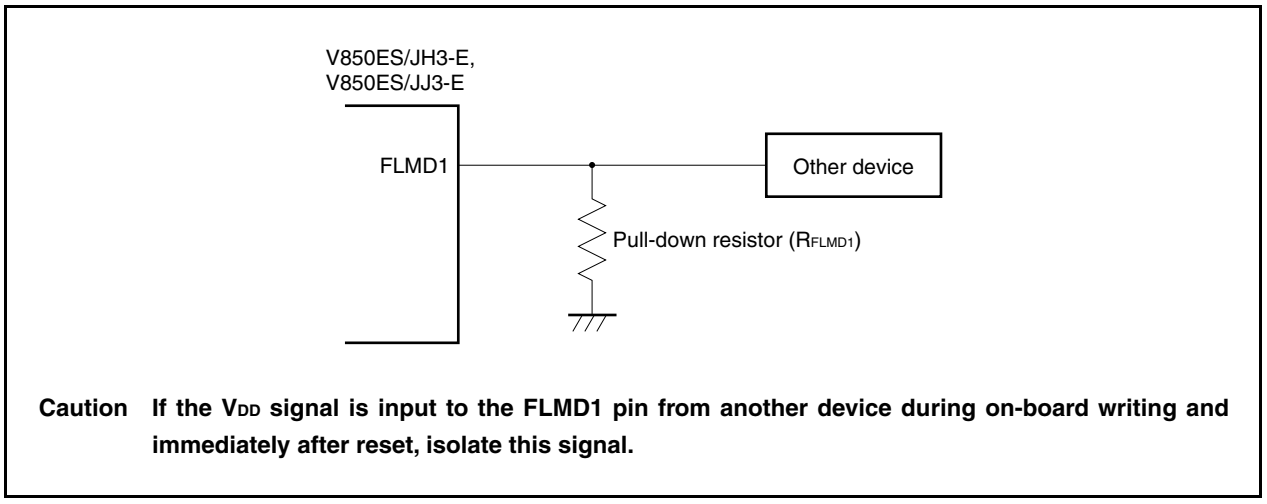
Figure 33-11. FLMD0 Pin Connection Example



(2) FLMD1 pin

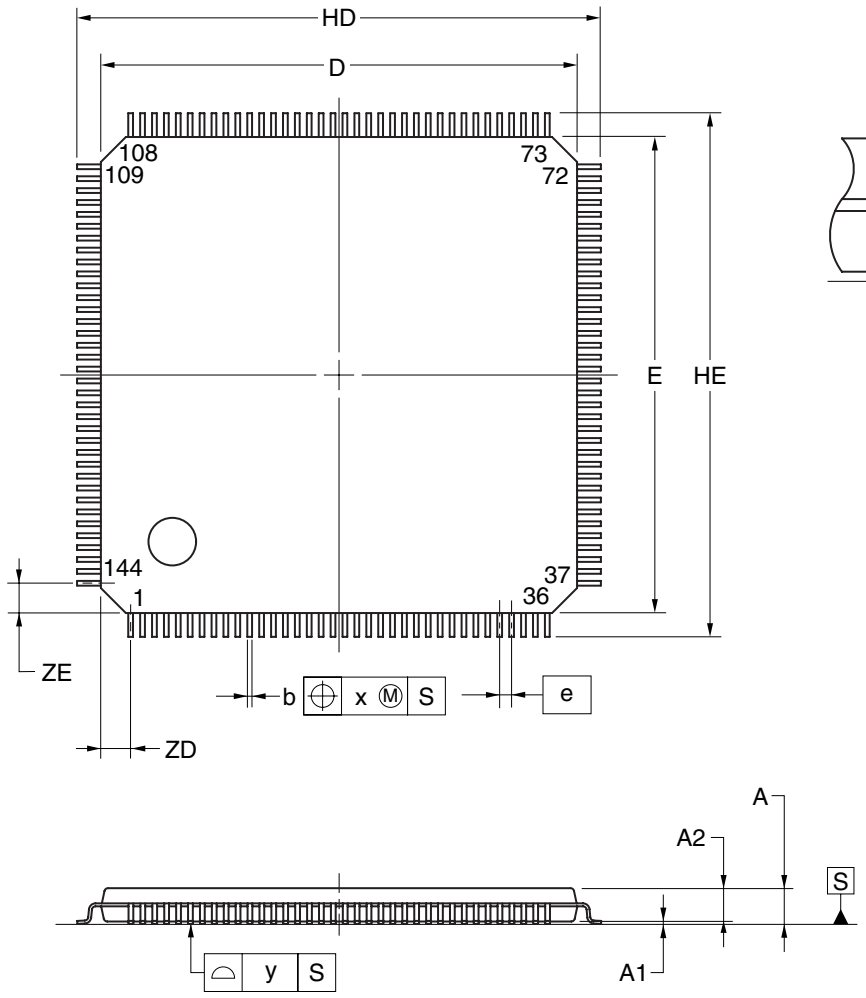
When 0 V is input to the FLMD0 pin, the FLMD1 pin does not function. When V_{DD} is supplied to the FLMD0 pin, the flash memory programming mode is entered, so 0 V must be input to the FLMD1 pin. The following shows an example of the connection of the FLMD1 pin.

Figure 33-12. FLMD1 Pin Connection Example

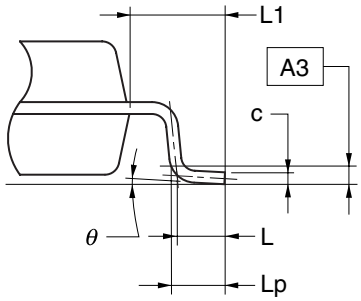


Caution If the V_{DD} signal is input to the FLMD1 pin from another device during on-board writing and immediately after reset, isolate this signal.

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	20.00±0.20
HD	22.00±0.20
HE	22.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P144GJ-50-GAE-2

Notes 12. In this instruction, for convenience of mnemonic description, the source register is made reg2, but the reg1 field is used in the opcode. Therefore, the meaning of register specification in the mnemonic description and in the opcode differs from other instructions.

rrrrr = regID specification

RRRRR = reg2 specification

13. iiiii: Lower 5 bits of imm9.

IIII: Higher 4 bits of imm9.

14. Do not specify the same register for general-purpose registers reg1 and reg3.

15. sp/imm: Specified by bits 19 and 20 of the sub-opcode.

16. ff = 00: Load sp in ep.

01: Load sign-expanded 16-bit immediate data (bits 47 to 32) in ep.

10: Load 16-bit logically-left-shifted 16-bit immediate data (bits 47 to 32) in ep.

11: Load 32-bit immediate data (bits 63 to 32) in ep.

17. If imm = imm32, n + 3 clocks.

18. rrrrr: Other than 00000.

19. ddddddd: Higher 7 bits of disp8.

20. dddd: Higher 4 bits of disp5.

21. dddddd: Higher 6 bits of disp8.