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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	124K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3782gf-gat-ax

(a) Function as compare register

The TABnCCR1 register can be rewritten even when the TABnCTL0.TABnCE bit = 1.

The set value of the TABnCCR1 register is transferred to the CCR1 buffer register. When the value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTABnCC1) is generated. If TOABn1 pin output is enabled at this time, the output of the TOABn1 pin is inverted.

(b) Function as capture register

When the TABnCCR1 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TABnCCR1 register if the valid edge of the capture trigger input pin (TIABn1 pin) is detected. In the pulse width measurement mode, the count value of the 16-bit counter is stored in the TABnCCR1 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIABn1 pin) is detected.

Even if the capture operation and reading the TABnCCR1 register conflict, the correct value of the TABnCCR1 register can be read.

Remark n = 0, 1

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 8-3. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	–
Triangular wave PWM mode	Compare register	Batch write

10.4.2 Cautions

(1) It takes the 16-bit counter up to the following time to start counting after the TMnCTL0.TMnCE bit is set to 1, depending on the count clock selected.

(n = 0)

Selected Count Clock	Maximum Time Before Counting Start
f_{XX}	$2/f_{XX}$
$f_{XX}/2$	$3/f_{XX}$
$f_{XX}/4$	$6/f_{XX}$
$f_{XX}/64$	$128/f_{XX}$
$f_{XX}/512$	$1024/f_{XX}$
$f_{XX}/1024$	$2048/f_{XX}$
$f_R/8$	$16/f_R$
f_{XT}	$2/f_{XT}$

(n = 1 to 3)

Selected Count Clock	Maximum Time Before Counting Start
$f_{XX}/2$	$4/f_{XX}$
$f_{XX}/4$	$6/f_{XX}$
$f_{XX}/8$	$12/f_{XX}$
$f_{XX}16$	$32/f_{XX}$
$f_{XX}/64$	$128/f_{XX}$
$f_{XX}/256$	$512/f_{XX}$
$f_{XX}/512$	$1024/f_{XX}$
$f_{XX}/1024$	$2048/f_{XX}$

(2) Rewriting the TMnCMP0 and TMnCTL0 registers is prohibited while TMMn is operating.
If these registers are rewritten while the TMnCE bit is 1, the operation cannot be guaranteed.
If they are rewritten by mistake, clear the TMnCTL0.TMnCE bit to 0, and re-set the registers.

Remark n = 0 to 3

11.2 Configuration

The motor control function consists of the following hardware.

Item	Configuration
Timer register	Dead-time counters
Compare register	TAB1 dead-time compare register (TAB1DTC register)
Control registers	TAB1 option register 1 (TAB1OPT1) TAB1 option register 2 (TAB1OPT2) TAB1 I/O control register 3 (TAB1IOC3) High-impedance output control register 0 (HZA0CTL0) High-impedance output control register 1 (HZA0CTL1)

- 6-phase PWM output can be produced with dead time by using the output of TAB1 (TOAB11, TOAB12, TOAB13).
- The output level of the 6-phase PWM output can be set individually.
- The 16-bit timer/counter of TAB1 counts up/down triangular waves. When the timer/counter underflows and when a cycle match occurs, an interrupt is generated. Interrupt generation, however, can be suppressed up to 31 times.
- TAA4 can execute counting at the same time as TAB1 (timer tuning operation function). TAA4 can be set in three ways as it can generate an A/D trigger source (TABTADT0) and two types of interrupts: a TAB1 underflow interrupt (INTTAB1OV) and a cycle match interrupt (INTTAB1CC0).

(4) Real-time counter control register 3 (RC1CC3)

The RC1CC3 register is an 8-bit register that controls the interval interrupt function and RTCDIV pin.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFAE0H

	7	6	5	4	3	2	1	0
RC1CC3	RINTE	CLOE2	CKDIV	0	0	ICT2	ICT1	ICT0

RINTE	Interval interrupt (INTRTC2) control
0	Does not generate interval interrupt.
1	Generates interval interrupt.

CLOE2	RTCDIV pin output control
0	Disables RTCDIV pin output.
1	Enables RTCDIV pin output.

CKDIV0	RTCDIV pin output frequency selection
1	Outputs 512 Hz (1.95 ms) from RTCDIV pin.
	Outputs 16.384 kHz (0.061 ms) from RTCDIV pin.

ICT2	ICT1	ICT0	Interval interrupt (INTRTC2) selection
0	0	0	$2^6/f_{XT}$ (1.953125 ms)
0	0	1	$2^7/f_{XT}$ (3.90625 ms)
0	1	0	$2^8/f_{XT}$ (7.8125 ms)
0	1	1	$2^9/f_{XT}$ (15.625 ms)
1	0	0	$2^{10}/f_{XT}$ (31.25 ms)
1	0	1	$2^{11}/f_{XT}$ (62.5 ms)
1	1	×	$2^{12}/f_{XT}$ (125 ms)

Cautions 1. See **12.4.7 Changing INTRTC2 interrupt setting during real-time counter operation** when rewriting the RINTE bit during real-time counter operation (RC1PWR bit = 1).

2. The RTCDIV output operates as follows when the CLOE2 bit setting is changed.

- When changed from 0 to 1: A pulse set by the CKDIV bit is output after two clocks or less (2 × 32.768kHz).
- When changed from 1 to 0: Output of the RTCDIV output is stopped after two clocks or less (fixed to low level, 2 × 32.768kHz)).

3. See **12.4.7 Changing INTRTC2 interrupt setting during real-time counter operation** when rewriting the ICT2 to ICT0 bits while the real-time counter operates (RC1PWR bit = 1).

(2/2)

UBnRT3	UBnRT2	UBnRT1	UBnRT0	Number of data of transmit FIFO set as trigger	Pointer mode	Pending mode
0	0	0	0	1 byte	Settable	Settable
0	0	0	1	2 bytes	Setting prohibited	
0	0	1	0	3 bytes		
0	0	1	1	4 bytes		
0	1	0	0	5 bytes		
0	1	0	1	6 bytes		
0	1	1	0	7 bytes		
0	1	1	1	8 bytes		
1	0	0	0	9 bytes		
1	0	0	1	10 bytes		
1	0	1	0	11 bytes		
1	0	1	1	12 bytes		
1	1	0	0	13 bytes		
1	1	0	1	14 bytes		
1	1	1	0	15 bytes		
1	1	1	1	16 bytes		

- Set the number of receive FIFO receive data to be the trigger.
- Each time data of the specified number has been stored from the receive shift register to receive FIFO, the INTUBnTIR interrupt is generated.
  In the pending mode (UBnFIC0.UBnIRM bit = 0), the INTUBnTIR signal is generated under the conditions of the pending mode.
- In the pointer mode (UBnFIC0.UBnIRM bit = 1), the number of receive data set as the trigger can be only 1 byte (UBnRT3 to UBnRT0 bits = 0000), and other settings are prohibited. If a setting of other than 1 byte is made, the operation is not guaranteed.

(5) CSIEn status register (CEnSTR)

These registers indicate the status of the CSIBUFn register or the transfer status.

These registers can be read or written in 8-bit or 1-bit units (however, bits 6 to 0 can only be read. They do not change even if they are written).

Reset sets this register to 20H.

In addition to reset input, the CEnSTR register can be initialized by clearing (0) the CEnCTL0.CEnPWR bit.

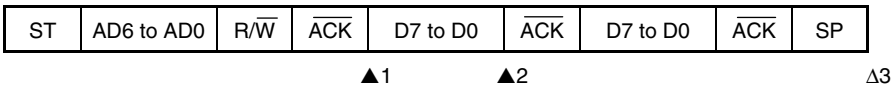
Cautions 1. Accessing the CEnSTR register is prohibited in the following statuses. For details, refer to 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates with the subclock and the main clock oscillation is stopped**
- **When the CPU operates with the internal oscillation clock**

2. Because the values of the CEnFLF, CEnEMP, CEnTSF, CEnSFP3 to CEnSFP0 bits may change at any time during transfer, their values during transfer may differ from the actual values. Especially, use the CEnTSF bit independently (do not use this bit in relation with the other bits). To detect the end of transfer by the CEnSTR register, check to see if the CEnEMF bit is 1 after the data to be transferred has been written to the CSIBUFn register.

(3) When arbitration loss occurs during data transfer

<1> When IICCn.WTIMn bit = 0



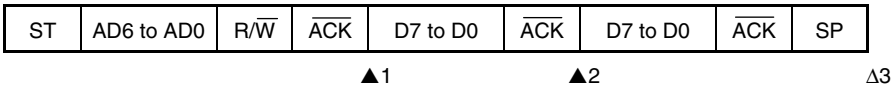
▲1: IICSn register = 10001110B

▲2: IICSn register = 01000000B (Example: When ALDn bit is read during interrupt servicing)

Δ 3: IICSn register = 00000001B

Remarks 1. ▲: Always generated
Δ: Generated only when SPIEn bit = 1
2. n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

<2> When WTIMn bit = 1



▲1: IICSn register = 10001110B

▲2: IICSn register = 01000100B (Example: When ALDn bit is read during interrupt servicing)

Δ 3: IICSn register = 00000001B

Remarks 1. ▲: Always generated
Δ: Generated only when SPIEn bit = 1
2. n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

20.14.2 When communication reservation function is disabled (IICFn.IICRSVn bit = 1)

When the IICCn.STTn bit is set when the bus is not being used for communication during bus communication, this request is rejected and a start condition is not generated. There are two modes in which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released when the IICCn.LRELn bit was set to 1) (n = 0 to 2)

To confirm whether the start condition was generated or the request was rejected, check the IICFn.STCFn flag. The time shown in Table 20-7 is required until the STCFn flag is set after setting the STTn bit to 1. Therefore, secure the time by software.

Table 20-7. Wait Periods

OCKSENm	OCKSm1	OCKSm0	CLn1	CLn0	Wait Period
1	0	0	0	×	20 clocks
1	0	1	0	×	30 clocks
1	1	0	0	×	40 clocks
1	1	1	0	×	50 clocks
0	0	0	1	0	10 clocks

Remarks **1.** ×: don't care

2. n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)
m = 0 to 2

(17) CAN0 module transmit history list register (C0TGPT)

The C0TGPT register is used to read the transmit history list.

(1/2)

After reset: xx02H R/W Address: 03FEC064H

(a) Read

	15	14	13	12	11	10	9	8
C0TGPT	TGPT7	TGPT6	TGPT5	TGPT4	TGPT3	TGPT2	TGPT1	TGPT0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	THPM	TOVF

(b) Write

	15	14	13	12	11	10	9	8
C0TGPT	0	0	0	0	0	0	0	0
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Clear TOVF

(a) Read

TGPT7 to TGPT0	Transmit history list read pointer
0 to 31	When the C0TGPT register is read, the contents of the element indexed by the read pointer (TGPT) of the transmit history list are read. These contents indicate the number of the message buffer to which a data frame or a remote frame was transmitted last.

THPM[Note 1]	Transmit history pointer match
0	The transmit history list has at least one message buffer number that has not been read.
1	The transmit history list has no message buffer numbers that have not been read.

TOVF[Note 2]	Transmit history list overflow bit
0	All the message buffer numbers that have not been read are preserved. All the numbers of the message buffers to which a new data frame or remote frame has been transmitted are recorded to the transmit history list (the transmit history list has a vacant element).
1	At least 7 entries have been stored since the host processor serviced the THL last time (i.e. read C0TGPT). The first 6 entries are sequentially stored whereas the last entry might have been overwritten by newly transmitted messages a number of times because all buffer numbers are stored at position LOPT-1 when TOVF bit is set to 1. As a consequence receptions cannot be completely recovered in the order that they were received.

Notes 1. The read value of the TGPT0 to TGPT7 bits is invalid when the THPM bit = 1.

2. If all the transmit history is read by the C0TGPT register while the TOVF bit is set (1), the THPM bit is not cleared (0) but kept set (1), even if transmission of new data has been completed.

Remark Transmission from message buffers 0 to 7 is not recorded to the transmit history list in the normal operation mode with ABT.

(11) UF0 INT status 0 register (UF0IS0)

This register indicates the interrupt source. If the contents of this register are changed, the EPCINT0B signal becomes active.

This register is read-only, in 8-bit units.

If an interrupt request (INTUSBF0) is generated from USBF, the FW must read this register to identify the interrupt source.

Each bit of this register is forcibly cleared to 0 when 0 is written to the corresponding bit of the UF0IC0 register.

Caution In the USBF, multiple interrupt sources, such as Bus Reset, Resume, and Short, are ORed internally and are issued as a single interrupt request (INTUSBF0). Therefore, in the case of the occurrence of multiple interrupt sources, they are ORed and issued as an INTUSBF0 interrupt request.

For example, if a Bus Reset interrupt source and Resume interrupt source occur, the two sources are ORed and an INTUSBF0 interrupt request is issued.

Under these conditions, if the Bus Reset interrupt source is cleared to 0 (UF0IC0.BUSRSTC = 0), the V850ES/JH3-E or V850ES/JJ3-E internal INTUSBF0 interrupt request may remain set to 1 since the Resume interrupt source will still remain. The new interrupt request flag (US0BIC.US0BIF), therefore, might not be set to 1.

In this case, after performing clear processing for each interrupt request with the INTUSBF0 interrupt servicing routine, confirm the flag status for the UF0IS0 and UF0IS1 registers again, and if there are any interrupt sources with flags set to 1, perform flag clearing (only the applicable bits need to be cleared (do not perform a batch clearing)).

	7	6	5	4	3	2	1	0	Address	After reset
UF0IS0	BUSRST	RSUSPD	0	SHORT	DMAED	SETRQ	CLRRQ	EPHALT	00200020H	00H

Bit position	Bit name	Function
7	BUSRST	This bit indicates that Bus Reset has occurred. 1: Bus Reset has occurred (interrupt request is generated). 0: Not Bus Reset status (default value)
6	RSUSPD	This bit indicates that the Resume or Suspend status has occurred. Reference bit 7 of the UF0EPS1 register by FW. 1: Resume or Suspend status has occurred (interrupt request is generated). 0: Resume or Suspend status has not occurred (default value).
4	SHORT	This bit indicates that data is read from the FIFO of either the UF0BO1 or UF0BO2 register and that the USBSPnB signal (n = 2, 4) is active. It is valid only when the FIFO is full in the DMA mode. 1: USBSPnB signal is active (interrupt request is generated). 0: USBSPnB signal is not active (default value). Identify on which endpoint the operation is performed, by using the UF0DMS1 register. This bit is not automatically cleared to 0 even when the UF0DMS1 register is read by FW.

(4) UF0 EP0 write register (UF0E0W)

The UF0E0W register is a 64-byte FIFO that stores the IN data (passes it to SIE) sent to the host in the data stage to Endpoint0.

This register is write-only, in 8-bit units. When this register is read, 00H is read.

The hardware transmits data to the USB bus in synchronization with an IN token only when the EP0NKW bit of the UF0E0N register is set to 1 (when NAK is not transmitted). When data is transmitted and when the host correctly receives the data, the EP0NKW bit of the UF0E0N register is automatically cleared to 0 by hardware. A short packet is transmitted when data is written to the UF0E0W register and the E0DED bit of the UF0DEND register is set to 1 (EP0W bit of the UF0EPS0 register = 1 (data exists)). A Null packet is transmitted when the UF0E0W register is cleared and the E0DED bit of the UF0DEND register is set to 1 (EP0W bit of the UF0EPS0 register = 1 (data exists)).

The UF0E0W register is cleared to 0 when the next SETUP token is received while transmission has not been completed yet. If the stage of control transfer (read) changes to the status stage while ACK has not been correctly received in the data stage, the UF0E0W register is automatically cleared to 0. At the same time, it is also cleared to 0 if the EP0NKW bit of the UF0E0N register is 1.

If the UF0E0W register is read while no data is in it, 00H is read.

	7	6	5	4	3	2	1	0	Address	After reset
UF0E0W	E0W7	E0W6	E0W5	E0W4	E0W3	E0W2	E0W1	E0W0	00200106H	Undefined

Bit position	Bit name	Function
7 to 0	E0W7 to E0W0	These bits store the IN data sent to the host in the data stage to Endpoint0.

The operation of the UF0E0W register is illustrated below.

(2) RPKT: Receive packet counter

Access This register can be read and written in 32-bit units.

Address 002E 0144H

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

31	30	29	28	27	26	25	24
RPKT31	RPKT30	RPKT29	RPKT28	RPKT27	RPKT26	RPKT25	RPKT24
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
RPKT23	RPKT22	RPKT21	RPKT20	RPKT19	RPKT18	RPKT1	RPKT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
RPKT15	RPKT14	RPKT13	RPKT12	RPKT11	RPKT10	RPKT9	RPKT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
RPKT7	RPKT6	RPKT5	RPKT4	RPKT3	RPKT2	RPKT1	RPKT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
31 to 0	RPKT[31:0]	This counter is incremented when any packet, including packets in which an error has occurred, all unicast packets, all multicast packets, and broadcast packets, is received.

(2) Procedure for transmitting or receiving a serial management frame

Serial management frames are transmitted or received as follows.

First, the MIND.SCANA bit is checked to see whether the SCAN command is under execution.

If not, the MIND.BUSY bit is checked to see whether the serial management frame is being accessed. If the BUSY bit is 1, the Ethernet controller waits until it is cleared to 0. On the other hand, while the SCAN command is being executed, the MCMD.SCANC bit is cleared to 0 and then the Ethernet controller waits until the BUSY bit is cleared to 0.

Next, the address of the external PHY device to which the frame is to be transmitted and the address of a register in the PHY device are set to the MADR.FIAD and RGAD bits, respectively.

When a write access is to be made, writing is started by writing data to the MWTD.CTLD bits.

The BUSY bit is set to 1 when data has been written to the MWDT register and cleared to 0 when writing is complete.

A read access is started by writing 1 to the MCMD.RSTAT bit. When the RSTAT bit is set to 1, the BUSY bit is set to 1. The BUSY bit is cleared to 0 after completion of reading. The host system can obtain the data of the PHY register by confirming that the BUSY bit is 0 and then reading the MRDD.PRSD bit.

To execute the SCAN command, set the MCMD.SCANC bit to 1. When this bit has been set to 1, reading is repeatedly executed. The MIND.SCANA bit is set to 1 while the SCAN command is being executed. The MIND.NVALID bit is set to 1 until the first read access is completed after the SCAN command has been executed. The MIND.BUSY bit is set to 1 when the SCAN command is executed. If the SCAN command is disabled (by clearing the MCMD.SCANC bit to 0), the MIND.BUSY bit is cleared to 0 after the current read access is completed.

How reception works is described below using an example of an actual descriptor chain.

After the RXS bit of the core function setting register (ETHMODE) is set to 1 by software, the first descriptor is read from the address indicated by the reception descriptor pointer (RXDP) (0028 0000H), and the reception descriptor is analyzed.

The first buffer address pointer (0028 1000H) is set as the DMA transfer start address and the reception data in the FIFO is transferred to buffer A.

When buffer A becomes full upon subsequent receptions, the next descriptor (0028 0008H) is read, the buffer address pointer (0028 1800H) is set as the DMA start address, and the reception data in the FIFO is transferred to buffer C.

In the final reception, the E and U bits of the descriptor are set to 1, and the number of data bytes transferred is written back to the descriptor's size field.

Once all the packet data has been transferred, the U and S bits of the first descriptor are set to 1, and the reception status information is written back to the status (A) field.

(7) External DMA request enable register (EXDRQEN)

The EXDRQEN register sets the DMA request to each DMA channel when connecting the external USB device by using the $\overline{\text{UDMARQm}}$/$\overline{\text{UDMAAKm}}$ pin (m = 0, 1).

This register can be read or written in 8-bit units.

Reset sets This register to 00H.

After reset: 00H R/W Address: FFFFFF60H

	7	6	5	4	3	2	1	0
EXDRQEN	RQ3EX1E	RQ2EX1E	RQ1EX1E	RQ0EX1E	RQ3EX0E	RQ2EX0E	RQ1EX0E	RQ0EX0E

RQnEX1E	Assignment of DMA channel n (n = 0 to 3)
0	Does not assign DMA channel n to $\overline{\text{UDMARQ1}}$/$\overline{\text{UDMAAK1}}$ pin
1	Assigns DMA channel n to $\overline{\text{UDMARQ1}}$/$\overline{\text{UDMAAK1}}$ pin

RQnEX0E	Assignment of DMA channel n (n = 0 to 3)
0	Does not assign DMA channel n to $\overline{\text{UDMARQ0}}$/$\overline{\text{UDMAAK0}}$ pin
1	Assigns DMA channel n to $\overline{\text{UDMARQ0}}$/$\overline{\text{UDMAAK0}}$ pin

Cautions 1. Assigning multiple DMA channels to the $\overline{\text{UDMARQ1}}$/$\overline{\text{UDMAAK1}}$ pin is prohibited (setting the RQ3EX1E, RQ2EX1E, RQ1EX1E, and RQ0EX1E bits to the $\overline{\text{UDMARQ1}}$/$\overline{\text{UDMAAK1}}$ pin at the same time is prohibited).

2. Assigning multiple DMA channels to the $\overline{\text{UDMARQ0}}$/$\overline{\text{UDMAAK0}}$ pin is prohibited (setting the RQ3EX0E, RQ2EX0E, RQ1EX0E, and RQ0EX0E bits to the $\overline{\text{UDMARQ0}}$/$\overline{\text{UDMAAK0}}$ pin at the same time is prohibited).

3. Assigning both the $\overline{\text{UDMARQ1}}$/$\overline{\text{UDMAAK1}}$ pin and the $\overline{\text{UDMARQ0}}$/$\overline{\text{UDMAAK0}}$ pin to the same DMA channel is prohibited (setting the RQ3EX1E and RQ3EX0E, RQ2EX1E and RQ2EX0E, RQ1EX1E and RQ1EX0E, and RQ0EX1E and RQ0EX0E bits respectively at the same time is prohibited).

4. When using a DMA request from an external source by setting the EXDRQEN register, set the DTFRn.IFCn5-IFCn0 bit to 000000 (to prohibit a DMA request via an interrupt).
For details, see 24.3 (6) DMA trigger factor registers 0 to 3 (DTFR0 to DTFR3).

(b) Repeatedly execute setting INITn bit until transfer is forcibly terminated correctly

<1> Suppress a request from the DMA request source of the channel to be forcibly terminated (stop operation of the on-chip peripheral I/O).
<2> Check that the DMA transfer request of the channel to be forcibly terminated is not held pending, by using the DTFRn.DFn bit. If a DMA transfer request is held pending, wait until execution of the pending request is completed.
<3> When it has been confirmed that the DMA request of the channel to be forcibly terminated is not held pending, clear the Enn bit to 0.
<4> Again, clear the Enn bit of the channel to be forcibly terminated.
If the target of transfer for the channel to be forcibly terminated (transfer source/destination) is the internal RAM, execute this operation once more.
<5> Copy the initial number of transfers of the channel to be forcibly terminated to a general-purpose register.
<6> Set the INITn bit of the channel to be forcibly terminated to 1.
<7> Read the value of the DBCn register of the channel to be forcibly terminated, and compare it with the value copied in <5>. If the two values do not match, repeat operations <6> and <7>.

Remarks 1. When the value of the DBCn register is read in <7>, the initial number of transfers is read if forced termination has been correctly completed. If not, the remaining number of transfers is read.
2. Note that method (b) may take a long time if the application frequently uses DMA transfer for a channel other than the DMA channel to be forcibly terminated.

(4) Procedure of temporarily stopping DMA transfer (clearing Enn bit)

Stop and resume the DMA transfer under execution using the following procedure.

<1> Suppress a transfer request from the DMA request source (stop the operation of the on-chip peripheral I/O).
<2> Check the DMA transfer request is not held pending, by using the DFn bit (check if the DFn bit = 0).
If a request is pending, wait until execution of the pending DMA transfer request is completed.
<3> If it has been confirmed that no DMA transfer request is held pending, clear the Enn bit to 0 (this operation stops DMA transfer).
<4> Set the Enn bit to 1 to resume DMA transfer.
<5> Resume the operation of the DMA request source that has been stopped (start the operation of the on-chip peripheral I/O).

(5) Memory boundary

The operation is not guaranteed if the address of the transfer source or destination exceeds the area of the DMA target (external memory, internal RAM, or on-chip peripheral I/O) during DMA transfer.

(6) Transferring misaligned data

DMA transfer of misaligned data with a 16-bit bus width is not supported.
If an odd address is specified as the transfer source or destination, the least significant bit of the address is forcibly assumed to be 0.

25.3.2 Restore

Recovery from maskable interrupt servicing is carried out by the RETI instruction.

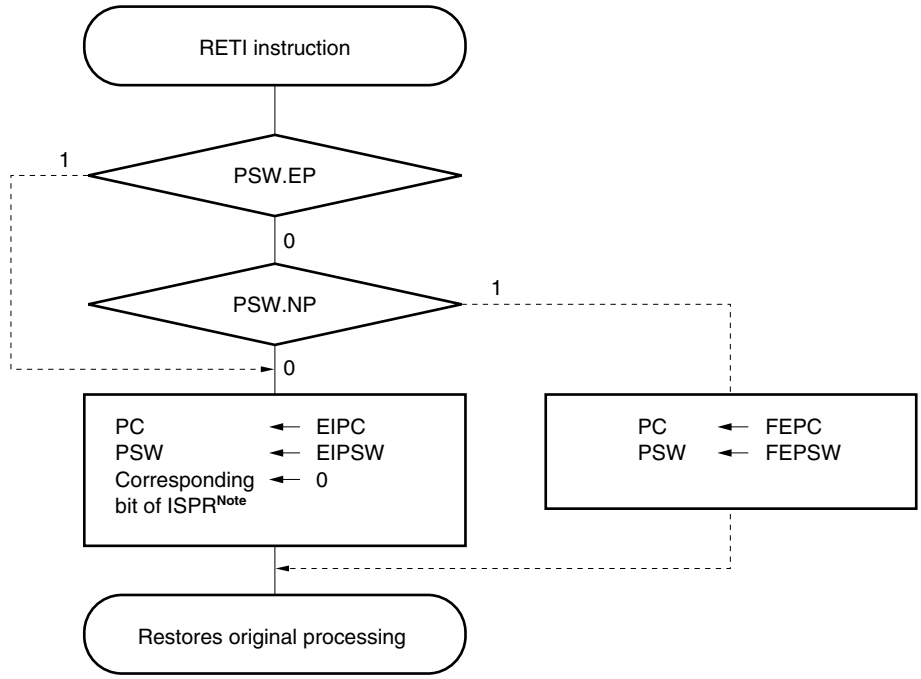
When the RETI instruction is executed, the CPU performs the following processing, and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from EIPC and EIPSW because the PSW.EP bit is 0 and the PSW.NP bit is 0.

<2> Transfers control back to the address of the restored PC and PSW.

The processing of the RETI instruction is shown below.

Figure 25-6. RETI Instruction Processing



Note For the ISPR register, see **25.3.6 In-service priority register (ISPR)**.

Caution When the EP and NP bits are changed by the LDSR instruction during maskable interrupt servicing, in order to restore the PC and PSW correctly during recovery by the RETI instruction, it is necessary to set the EP bit back to 0 and the NP bit back to 0 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

Table 27-9. Operating Status in STOP Mode

Setting of STOP Mode / Item		Operating Status	
		When Subclock Is Not Used	When Subclock Is Used
Main clock oscillator (f_X)		Stops oscillation	
Subclock oscillator (f_{XT})		–	Oscillation enabled
Internal oscillator (f_R)		Oscillation enabled	
PLL		Stops operation	
CPU		Stops operation	
DMA controller		Stops operation	
Interrupt controller		Stops operation	
Timer	TAA0 to TAA5	Stops operation	
	TAB0, TAB1	Stops operation	
	TMM0 to TMM3	Operable when f_R/8 is selected as the count clock	Operable when f_R/8 or f_{XT} is selected as the count clock
	TMT0	Stops operation	
Real-time counter (RTC)		Stops operation	Operable when f_{XT} is selected as the count clock
Watchdog timer (WDT2)		Operable when f_R is selected as the count clock	Operable when f_R or f_{XT} is selected as the count clock
Serial interface	CSIFn	Operable when the $\overline{\text{SCKFn}}$ input clock is selected as the count clock (n = 0 to 4: V850ES/JH3-E, n = 0 to 6: V850ES/JJ3-E)	
	CSIE0, CSIE1	Operable when the $\overline{\text{SCKE0}}$ or $\overline{\text{SCKE1}}$ input clock is selected as the count clock	
	I^2C0m	Stops operation (m = 0 to 3: V850ES/JH3-E, m = 0 to 4: V850ES/JJ3-E)	
	UARTCx	Stops operation (but UARTC0 is operable when the ASCKC0 input clock is selected) (x = 0 to 5: V850ES/JH3-E, x = 0 to 7: V850ES/JJ3-E)	
	UARTB0, UARTB1	Stops operation	
A/D converter		Stops operation (conversion result undefined)Notes 1, 2	
Real-time output function (RTO)		Stops operation (output held)	
Key interrupt function (KR)		Operable	
CRC operation circuit		Stops operation	
External bus interface		See **CHAPTER 5 BUS CONTROL FUNCTION**.	
Port function		Retains status before STOP mode was set	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the STOP mode was set.	
CANNote 5		Stops operation	
USB function		Stops operationNote 4	
Ethernet controller		Stops operationNote 4	

Notes 1. If the STOP mode is set while the A/D converter is operating, the A/D converter is automatically stopped and starts operating again after the STOP mode is released. However, in that case, the A/D conversion results after the STOP mode is released are invalid. All the A/D conversion results before the STOP mode is set are invalid.

2. Even if the STOP mode is set while the A/D converter is operating, the power consumption is reduced equivalently to when the A/D converter is stopped before the STOP mode is set.

3. μPD70F3783, 70F3786 only

4. To realize low power consumption, stop the USB function and Ethernet controller before shifting to the stop mode.

CHAPTER 37 RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/index.html)

Remark Evaluation of the soldering conditions for the (A) standard products is incomplete because these products are under development.

Table 37-1. Surface Mounting Type Soldering Conditions

μPD70F3778GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3779GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3780GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3781GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3782GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)
μPD70F3783GF-GAT-AX: 128-pin plastic LQFP (fine pitch) (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. Products with –AX at the end of the part number are lead-free products.

2. For soldering methods and conditions other than those recommended, please contact a Renesas Electronics sales representative.

Table A-1. System Configuration (When Using QB-V850ESJX3E[Note 1])

Target Device		V850ES/JH3-E 128-pin plastic LQFP	V850ES/JJ3-E 144-pin plastic LQFP
<5> In-circuit emulator		QB-V850ESJX3E[Note 1]	
<6> Check pin adapter	S type	QB-144-CA-01[Note 2] (optional)	
	T type		
<7> Extension probe (flexible type)	S type	QB-144-EP-02S (optional)	
	T type		
<8> Extension probe (coaxial type)	S type	QB-144-EP-01S (optional)	
	T type		
<9> Exchange adapter[Note 3]	S type	QB-128GF-EA-01S	QB-144GJ-EA-01S
	T type	QB-128GF-EA-02T	QB-144GJ-EA-01T
<10> Check pin adapter[Note 4]	S type	QB-128-CA-01S (optional)	QB-144-CA-01S (optional)
<11> Space adapter[Note 4]	S type	QB-144-SA-01S (optional)	QB-144-SA-01S (optional)
	T type	QB-128GF-YS-01T (optional)	QB-144GJ-01T (optional)
<12> YQ connector[Note 3]	T type	QB-128GF-YQ-01T	QB-144GJ-YQ-01T
<13> Mount adapter	S type	QB-128GF-MA-01S	QB-144GJ-MA-01S
	T type	QB-128GF-HQ-01T	QB-144GJ-HQ-01T
<14> Target connector[Note 3]	S type	QB-128GF-TC-01S	QB-144GJ-TC-01S
	T type	QB-128GF-NQ-01T	QB-144GJ-NQ-01T
<15> Target system			

Notes 1. The QB-V850ESJX3E (under development) is supplied with a power supply unit, USB interface cable, and flash memory programmer (MINICUBE2). It is also supplied with integrated debugger ID850QB as control software.

2. Under development

3. Supplied with the device depending on the ordering number.

- When QB-V850ESJX3E-ZZZ is ordered: The exchange adapter and the target connector are not supplied.
- When QB-V850ESJX3E-S128GF is ordered: The QB-128GF-EA-01S and QB-128GF-TC-01S are supplied.
- When QB-V850ESJX3E-T128GF is ordered: The QB-128GF-EA-02T, QB-128GF-YQ-01T, and QB-128GF-NQ-01T are supplied.
- When QB-V850ESJX3E-S144GJ is ordered: The QB-144GJ-EA-01S and QB-144GJ-TC-01S are supplied.
- When QB-V850ESJX3E-T144GJ is ordered: The QB-144GJ-EA-01T, QB-144GJ-YQ-01T, and QB-144GJ-NQ-01T are supplied.

4. When using both <9> and <10>, the order between <9> and <10> is not cared.

Remark The numbers in the angle brackets correspond to the numbers in Figure A-2.