Renesas Electronics America Inc - UPD70F3783GF-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	124K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3783gf-gat-ax

(4) Port n function control register (PFCn)

The PFCn register specifies the alternate function of a port pin to be used if the pin has two alternate functions.

Each bit of this register corresponds to one pin of port n, and the alternate function of a port pin can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCnm	Specification of alternate function
0	Alternate function 1
1	Alternate function 2

(5) Port n function control expansion register (PFCEn)

The PFCEn register specifies the alternate function of a port pin to be used if the pin has three or more alternate functions.

Each bit of this register corresponds to one pin of port n, and the alternate function of a port pin can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCEn	PFCEn7	PFCEn6	PFCEn5	PFCEn4	PFCEn3	PFCEn2	PFCEn1	PFCEn0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCEnm	PFCnm	Specification of alternate function
0	0	Alternate function 1
0	1	Alternate function 2
1	0	Alternate function 3
1	1	Alternate function 4

Figure 7-23. Setting of Registers in External Trigger Pulse Output Mode (1/2)

(a) TAAn control register 0 (TAAnCTL0)

	TAAnCE					TAAnCKS2	TAAnCKS1	TAAnCKS0
TAAnCTL0	0/1	0	0	0	0	0/1	0/1	0/1

Select count clock

0: Stops counting
1: Enables counting

(b) TAAn control register 1 (TAAnCTL1)

		TAAnEST	TAAnEEE			TAAnMD2	TAAnMD1	TAAnMD0
TAAnCTL1	0	0/1	0	0	0	0	1	0

0, 1, 0:
External trigger pulse output mode

Generates software trigger when 1 is written

(c) TAAn I/O control register 0 (TAAnIOC0)

					TAAnOL1	TAAnOE1	TAAnOL0	TAAnOE0
TAAnIOC0	0	0	0	0	0/1	0/1	0/1 Note	0/1 Note

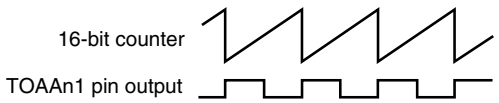
0: Disables TOAAn0 pin output
1: Enables TOAAn0 pin output

Sets output level while operation of TOAAn0 pin is disabled
0: Low level
1: High level

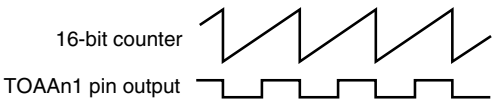
0: Disables TOAAn1 pin output
1: Enables TOAAn1 pin output

Specifies active level of TOAAn1 pin output
0: Active-high
1: Active-low

- When TAAnOL1 bit = 0



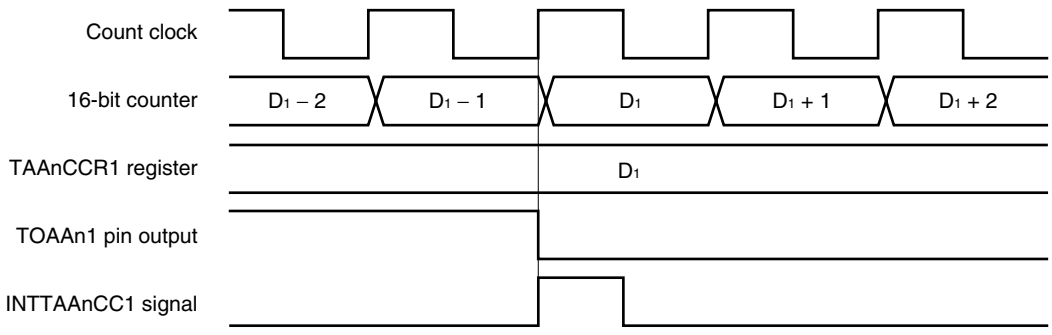
- When TAAnOL1 bit = 1



Note Clear this bit to 0 when the TOAAn0 pin is not used in the external trigger pulse output mode.

(c) Generation timing of compare match interrupt request signal (INTTAAnCC1)

The timing of generation of the INTTAAnCC1 signal in the PWM output mode differs from the timing of other INTTAAnCC1 signals; the INTTAAnCC1 signal in the PWM output mode is generated when the count value of the 16-bit counter matches the value of the TAAnCCR1 register.



Remark n = 0 to 5

Usually, the INTTAAnCC1 signal is generated in synchronization with the next count-up after the count value of the 16-bit counter matches the value of the TAAnCCR1 register.

In the PWM output mode, however, it is generated one clock earlier. This is because the timing is changed to match the change timing of the output signal of the TOAAn1 pin.

(5) TABn I/O control register 2 (TABnIOC2)

The TABnIOC2 register is an 8-bit register that controls the valid edge of the external event count input signal (TIAB00/EVTAB1 pin) and external trigger input signal (TIAB00/TRGAB1 pin).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TAB0IOC2 FFFFF544H, TAB1IOC2 FFFFF564H

TABnIOC2 (n = 0, 1)

7	6	5	4	3	2	1	0
0	0	0	0	TABnEES1	TABnEES0	TABnETS1	TABnETS0

TABnEES1	TABnEES0	External event count input signal (TIAB00/EVTAB1 pin) valid edge setting
0	0	No edge detection (external event count invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

TABnETS1	TABnETS0	External trigger input signal (TIAB00/TRGAB1 pin) valid edge setting
0	0	No edge detection (external trigger invalid)
0	1	Detection of rising edge
1	0	Detection of falling edge
1	1	Detection of both edges

Cautions

1. **Rewrite the TABnEES1, TABnEES0, TABnETS1, and TABnETS0 bits when the TABnCTL0.TABnCE bit = 0. (The same value can be written when the TABnCE bit = 1.) If rewriting was mistakenly performed, clear the TABnCE bit to 0 and then set the bits again.**
2. **The TABnEES1 and TABnEES0 bits are valid only when the TABnCTL1.TABnEEE bit = 1 or when the external event count mode (TABnCTL1.TABnMD2 to TABnCTL1.TABnMD0 bits = 001) has been set.**
3. **The TABnETS1 and TABnETS0 bits are valid only when the external trigger pulse output mode (TABnCTL1.TABnMD2 to TABnCTL1.TABnMD0 bits = 010) or the one-shot pulse output mode (TABnCTL1.TABnMD2 to TABnCTL1.TABnMD0 = 011) is set.**

(a) Setting procedure

(i) Setting of high-impedance control operation

<1> Set the HZA0DCMn, HZA0DCNn, and HZA0DCPn bits.

<2> Set the HZA0DCEn bit to 1 (enable high-impedance control).

(ii) Changing setting after enabling high-impedance control operation

<1> Clear the HZA0DCEn bit to 0 (to stop the high-impedance control operation).

<2> Change the setting of the HZA0DCMn, HZA0DCNn, and HZA0DCPn bits.

<3> Set the HZA0DCEn bit to 1 (to enable the high-impedance control operation again).

(iii) Resuming output when pins are in high-impedance state

If the HZA0DCMn bit is 1, set the HZA0DCCn bit to 1 to clear the high-impedance state after the valid edge of the external pin is detected. However, the high-impedance state cannot be cleared unless this bit is set while the input level of the external pin is inactive.

<1> Set the HZA0DCCn bit to 1 (command signal to clear the high-impedance state).

<2> Read the HZA0DCFn bit and check the flag status.

<3> Return to <1> if the HZA0DCFn bit is 1. The input level of the external pin must be checked.
The pin can function as an output pin if the HZA0DCFn bit is 0.

(iv) Making pin go into high-impedance state by software

The HZA0DCTn bit must be set to 1 by software to make the pin go into a high-impedance state while the input level of the external pin is inactive. The following procedure is an example in which the setting is not dependent upon the setting of the HZA0DCMn bit.

<1> Set the HZA0DCTn bit to 1 (high-impedance output command).

<2> Read the HZA0DCFn bit to check the flag status.

<3> Return to <1> if the HZA0DCFn bit is 0. The input level of the external pin must be checked.
The pin is in a high-impedance state if the HZA0DCFn bit is 1.

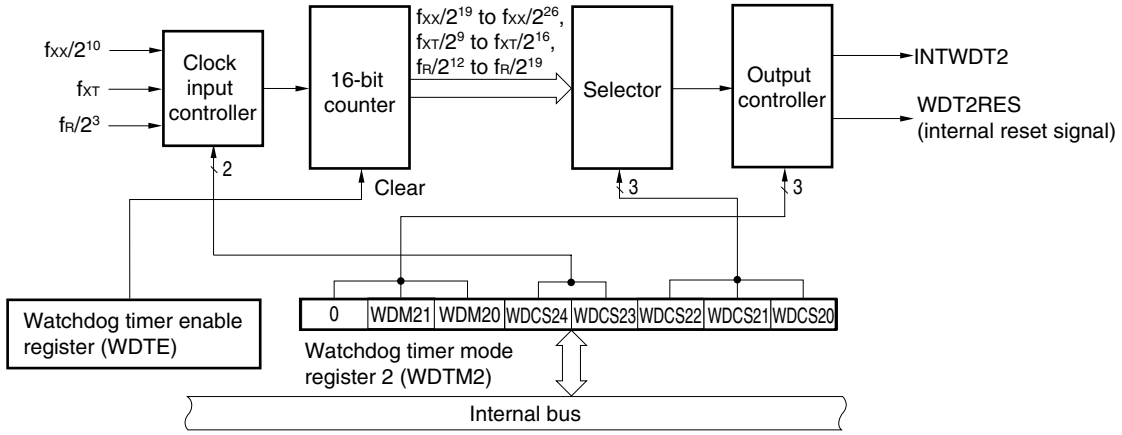
However, if the external pin is not used with the HZA0DCPn bit and HZA0DCNn bit cleared to 0, the pin goes into a high-impedance state when the HZA0DCTn bit is set to 1.

Remark n = 0, 1

13.2 Configuration

The following shows the block diagram of watchdog timer 2.

Figure 13-1. Block Diagram of Watchdog Timer 2



Remark fXX: Main clock frequency
fXT: Subclock frequency
fR: Internal oscillation clock frequency
INTWDT2: Non-maskable interrupt request signal from watchdog timer 2
WDTRES2: Watchdog timer 2 reset signal

Watchdog timer 2 includes the following hardware.

Table 13-1. Configuration of Watchdog Timer 2

Item	Configuration
Control registers	Watchdog timer mode register 2 (WDTM2) Watchdog timer enable register (WDTE)

(5) A/D conversion result registers n, nH (ADA0CRn, ADA0CRnH)

The ADA0CRn and ADA0CRnH registers store the A/D conversion results.

These registers are read-only, in 16-bit or 8-bit units. However, the ADA0CRn register is used for 16-bit access and the ADA0CRnH register for 8-bit access. The 10 bits of the conversion result are read to the higher 10 bits of the ADA0CRn register, and 0 is read to the lower 6 bits. The higher 8 bits of the conversion result are read to the ADA0CRnH register.

Caution Accessing the ADA0CRn and ADA0CRnH registers is prohibited in the following statuses. For details, see 3.4.9 (2) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and the main clock oscillation is stopped**
- **When the CPU operates on the internal oscillation clock**

After reset: Undefined R Address: ADA0CR0 FFFFF210H, ADA0CR1 FFFFF212H, ADA0CR2 FFFFF214H, ADA0CR3 FFFFF216H, ADA0CR4 FFFFF218H, ADA0CR5 FFFFF21AH, ADA0CR6 FFFFF21CH, ADA0CR7 FFFFF21EH, ADA0CR8 FFFFF220H, ADA0CR9 FFFFF222H, ADA0CR10[Note] FFFFF224H, ADA0CR11[Note] FFFFF226H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADA0CRn	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	0	0	0	0	0

After reset: Undefined R Address: ADA0CR0H FFFFF211H, ADA0CR1H FFFFF213H, ADA0CR2H FFFFF215H, ADA0CR3H FFFFF217H, ADA0CR4H FFFFF219H, ADA0CR5H FFFFF21BH, ADA0CR6H FFFFF21DH, ADA0CR7H FFFFF21FH, ADA0CR8H FFFFF221H, ADA0CR9H FFFFF223H, ADA0CR10H[Note] FFFFF225H, ADA0CR11H[Note] FFFFF227H

	7	6	5	4	3	2	1	0
ADA0CRnH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

Note V850ES/JJ3-E only

Caution A write operation to the ADA0M0 and ADA0S registers may cause the contents of the ADA0CRn register to become undefined. After the conversion, read the conversion result before writing to the ADA0M0 and ADA0S registers. Correct conversion results may not be read at a timing other than the above.

(ii) During reception (reading from receive FIFO)

- If data for the first reception end interrupt request signal (INTUBnTIR) is not read from receive FIFO, the second INTUBnTIR signal does not occur (is held pending) even if the generation condition of the second INTUBnTIR is satisfied (if receive data of the number set as the trigger by the UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits can be read from receive FIFO). When data for the first INTUBnTIR signal is later read from the receive FIFO, the pending INTUBnTIR signal is generated[Note].

  Note The number of pending interrupts is as follows.

  When trigger is set to 1 byte (UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits = 0000): 15 times max.
  When trigger is set to 2 bytes (UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits = 0001): 7 times max.
  :
  When trigger is set to 6 bytes (UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits = 0101): 1 time max.
  When trigger is set to 7 bytes (UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits = 0110): 1 time max.
  When trigger is set to 8 bytes (UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits = 0111): 1 time max.

- In the pending mode, receive data of the number set as the trigger by the UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits is always read from receive FIFO when the reception end interrupt request signal (INTUBnTIR) occurs. Reading data from receive FIFO is prohibited if the data is more or less than the specified number. If data more or less than the specified number is read, the operation is not guaranteed.
- Fix the UBnFIC2.UBnRT3 to UBnFIC2.UBnRT0 bits to 0000 (set number of receive data: 1 byte) to read receive data from receive FIFO by DMA. If any other setting is made, the operation is not guaranteed.

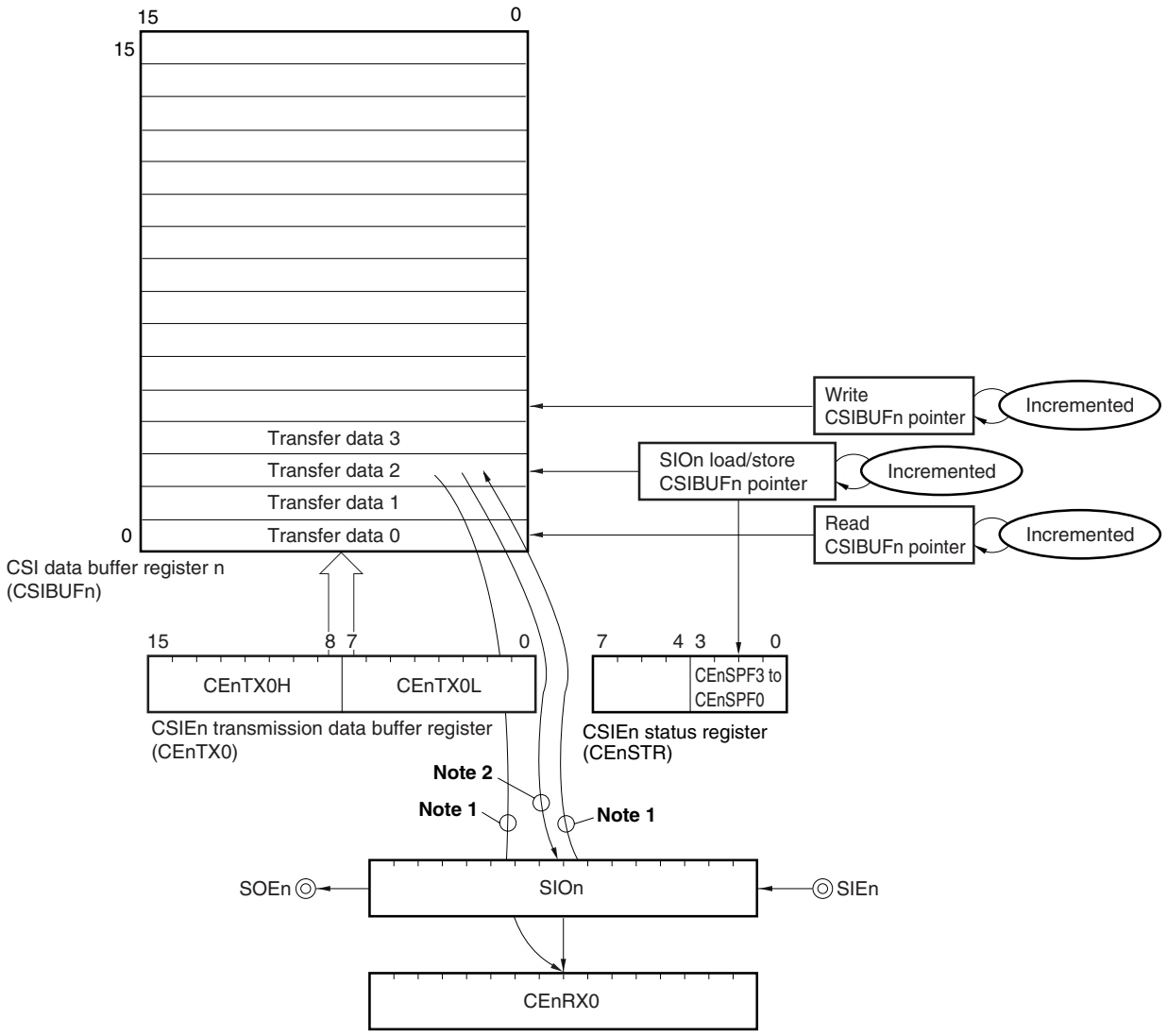
(b) Pointer mode

(i) During transmission (writing to transmit FIFO)

- Each time the data of 1 byte is transferred to the transmit shift register from transmit FIFO, a transmission enable interrupt request signal (INTUBnTIT) occurs.
- In the pointer mode, be sure to fix the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits to 0000 (set number of transmit data: 1 byte) as the number of transmit data set as the trigger for transmit FIFO when the transmission enable interrupt request signal (INTUBnTIT) occurs. If any other setting is made, the operation is not guaranteed.
- Writing transmit data to transmit FIFO by DMA is prohibited. The operation is not guaranteed if DMA control is used.
- After the transmission enable interrupt request signal (INTUBnTIT) has been acknowledged, data of the number of empty bytes of transmit FIFO can be written to transmit FIFO by referencing the UBnFIS1 register.

Remark n = 0, 1

Figure 18-11. Continuous Mode



Notes 1. Reception

2. Transmission

Remark n = 0, 1

19.3.4 Mode switching between CSIF3 and UARTB1

In the V850ES/JH3-E and V850ES/JJ3-E, CSIF3 and UARTB1 share the same pin and therefore cannot be used simultaneously. Set CSIF3 and UARTB1 in advance, using the PMC9, PFC9, and PFCE9 registers, before use.

Caution The transmit/receive operation of CSIF3 and UARTB1 is not guaranteed if these functions are switched during transmission or reception. Be sure to disable the one that is not used.

Figure 19-5. CSIF3 and UARTB1 Mode Switch Settings

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H)	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H)	PFC915	PFC914	PFC913	PFC912	PFC911	PFC910	PFC99	PFC98

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	PFC95	PFC94	PFC93	PFC92	PFC91	PFC90

After reset: 0000H R/W Address: PFCE9 FFFFF712H,
PFCE9L FFFFF712H, PFCE9H FFFFF713H

	15	14	13	12	11	10	9	8
PFCE9 (PFCE9H)	PFCE915	PFCE914	PFCE913	0	PFCE911	PFCE910	PFCE99	PFCE98

	7	6	5	4	3	2	1	0
(PFCE9L)	PFCE97	PFCE96	PFCE95	PFCE94	PFCE93	PFCE92	PFCE91	PFCE90

PMC915	PFCE915	PFC915	Operation mode
0	×	×	Port I/O mode
1	0	0	$\overline{\text{SCKF3}}$ (CSIF3)

PMC914	PFCE914	PFC914	Operation mode
0	×	×	Port I/O mode
1	0	0	SOF3 (CSIF3)
1	0	1	RXDB1 (UARTB1)

PMC913	PFCE913	PFC913	Operation mode
0	×	×	Port I/O mode
1	0	0	SIF3 (CSIF3)
1	0	1	TXDB1 (UARTB1)

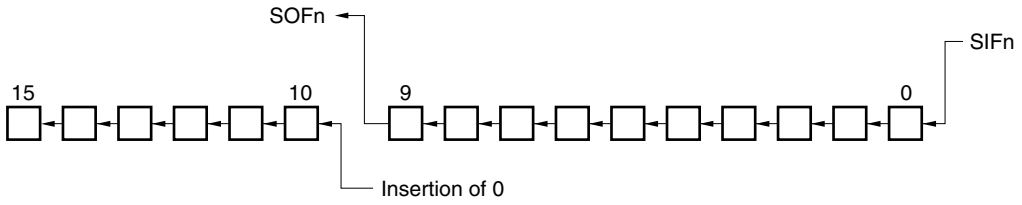
Remark × = don't care

(a) Transfer data length change function

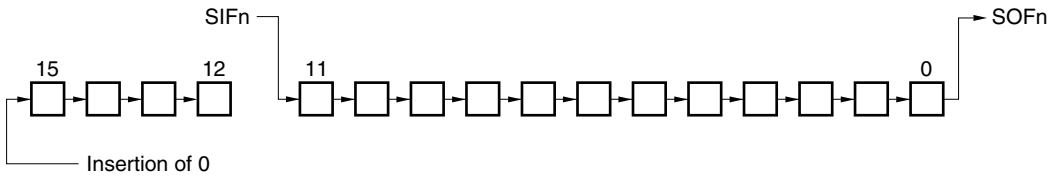
The CSIFn transfer data length can be set in 1-bit units between 8 and 16 bits using the CFnCTL2.CFnCL3 to CFnCTL2.CFnCL0 bits.

When the transfer bit length is set to a value other than 16 bits, set the data to the CFnTX or CFnRX register starting from the LSB, regardless of whether the transfer start bit is the MSB or LSB. Any data can be set for the higher bits that are not used, but the receive data becomes 0 following serial transfer.

(i) Transfer bit length = 10 bits, MSB first



(ii) Transfer bit length = 12 bits, LSB first



Remark n = 0 to 4 (V850ES/JH3-E)
n = 0 to 6 (V850ES/JJ3-E)

21.9.3 Receive history list function

The receive history list (RHL) function records in the receive history list the number of the receive message buffer in which each data frame or remote frame was received and stored. The RHL consists of storage elements equivalent to up to 23 messages, the last in-message pointer (LIPT) with the corresponding C0LIPT register and the receive history list get pointer (RGPT) with the corresponding C0RGPT register.

The RHL is undefined immediately after the transition of the CAN module from the initialization mode to one of the operation modes.

The C0LIPT register holds the contents of the RHL element indicated by the value of the LIPT pointer minus 1. By reading the C0LIPT register, therefore, the number of the message buffer that received and stored a data frame or remote frame first can be checked. The LIPT pointer is utilized as a write pointer that indicates to what part of the RHL a message buffer number is recorded. Any time a data frame or remote frame is received and stored, the corresponding message buffer number is recorded to the RHL element indicated by the LIPT pointer. Each time recording to the RHL has been completed, the LIPT pointer is automatically incremented. In this way, the number of the message buffer that has received and stored a frame will be recorded chronologically.

The RGPT pointer is utilized as a read pointer that reads a recorded message buffer number from the RHL. This pointer indicates the first RHL element that the CPU has not read yet. By reading the C0RGPT register by software, the number of a message buffer that has received and stored a data frame or remote frame can be read. Each time a message buffer number is read from the C0RGPT register, the RGPT pointer is automatically incremented.

If the value of the RGPT pointer matches the value of the LIPT pointer, the C0RGPT.RHPM bit (receive history list pointer match) is set to 1. This indicates that no message buffer number that has not been read remains in the RHL. If a new message buffer number is recorded, the LIPT pointer is incremented and because its value no longer matches the value of the RGPT pointer, the RHPM bit is cleared. In other words, the numbers of the unread message buffers exist in the RHL.

If the LIPT pointer is incremented and matches the value of the RGPT pointer minus 1, the C0RGPT.ROVF bit (receive history list overflow) is set to 1. This indicates that the RHL is full of numbers of message buffers that have not been read. When further message reception and storing occur, the last recorded message buffer number is overwritten by the number of the message buffer that received and stored the new message. After the ROVF bit has been set to 1, the recorded message buffer numbers in the RHL do not completely reflect chronological order. However the messages themselves are not lost and can be located by a CPU search in the message buffer memory with the help of the DN bit.

Caution Even if the receive history list overflows (C0RGPT.ROVF bit = 1), the receive history can be read until no more history is left unread and the C0RGPT.RHPM bit is set (1). However, the ROVF bit is kept set (1) (= overflow occurs) until cleared (0) by software. In this status, the RHPM bit is not cleared (0), unless the ROVF bit is cleared (0), even if a new receive history is stored and written to the list. If ROVF bit = 1 and RHPM bit = 1 and the receive history list overflows, therefore, the RHPM bit indicates that no more history is left unread even if new history is received and stored.

(g) SET_CONFIGURATION() request

If any of wValue, wIndex, or wLength is other than the values shown in Table 22-3, a STALL response is made in the status stage.

- Default state: The CONF bit of the UF0 mode status register (UF0MODS) and the UF0 configuration register (UF0CNF) are set to 1 if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the CONF bit of the UF0MODS register and UF0CNF register are cleared to 0. In other words, the device skips the Addressed state and moves to the Configured state in which it responds to the Default address.
- Addressed state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device enters the Configured state if the specified configuration value is 1 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 0, the device remains in the Addressed state.
- Configured state: The CONF bit of the UF0MODS register and UF0CNF register are set to 1 and the device returns to the Addressed state if the specified configuration value is 0 when the SET_CONFIGURATION() request has been received. If the specified configuration value is 1, the device remains in the Configured state.

If the SET_CONFIGURATION() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) is set to 1, and an interrupt is issued. All Halt Features are cleared after the SET_CONFIGURATION() request has been completed even if the specified configuration value is the same as the current configuration value. If the SET_CONFIGURATION() request has been correctly processed, the data toggle of all endpoints is always initialized to DATA0 again (it is defined that the default status, Alternative Setting 0, is set from when the SET_CONFIGURATION request is received to when the SET_INTERFACE request is received).

(h) SET_FEATURE() request

A STALL response is made in the status stage if the SET_FEATURE() request is for a Feature that cannot be set or does not exist, or if the target is an interface or an endpoint that does not exist. A STALL response is also made if the wLength value is other than 0.

- Default state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Addressed state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or Endpoint0; otherwise a STALL response is made in the status stage.
- Configured state: The correct response is made when the SET_FEATURE() request has been received, only if the request is for a device or an endpoint that exists; otherwise a STALL response is made in the status stage.

When the SET_FEATURE() request has been correctly processed, the target bit of the UF0 SET request register (UF0SET) and the EnHALT bit of the UF0 EPn status register L (UF0EnSL) are set to 1, and an interrupt is issued (n = 0 to 4, 7).

(24) UF0 INT clear 3 register (UF0IC3)

This register controls clearing the interrupt sources indicated by the UF0IS3 register.

This register is write-only, in 8-bit units. If this register is read, the value FFH is read.

FW can clear an interrupt source by writing 0 to the corresponding bit of this register. Even a bit that is automatically cleared to 0 by hardware can be cleared by FW before it is cleared by hardware. Writing 0 to a bit of this register automatically sets the bit to 1. Writing 1 is invalid.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 2, 4) and the current setting of the interface.

	7	6	5	4	3	2	1	0	Address	After reset
UF0IC3	BKO2FLC	BKO2NLC	BKO2NAKC	BKO2DTC	BKO1FLC	BKO1NLC	BKO1NAKC	BKO1DTC	00200042H	FFH

Bit position	Bit name	Function
7, 3	BKOnFLC	These bits clear the BLKOnFL interrupt. 0: Clear
6, 2	BKOnNLC	These bits clear the BLKOnNL interrupt. 0: Clear
5, 1	BKOnNAKC	These bits clear the BLKOnNK interrupt. 0: Clear
4, 0	BKOnDTC	These bits clear the BLKOnDT interrupt. 0: Clear

Remark n = 1, 2

(20) R511: Receive 256- to 511-byte frame counter

Access This register can be read and written in 32-bit units.

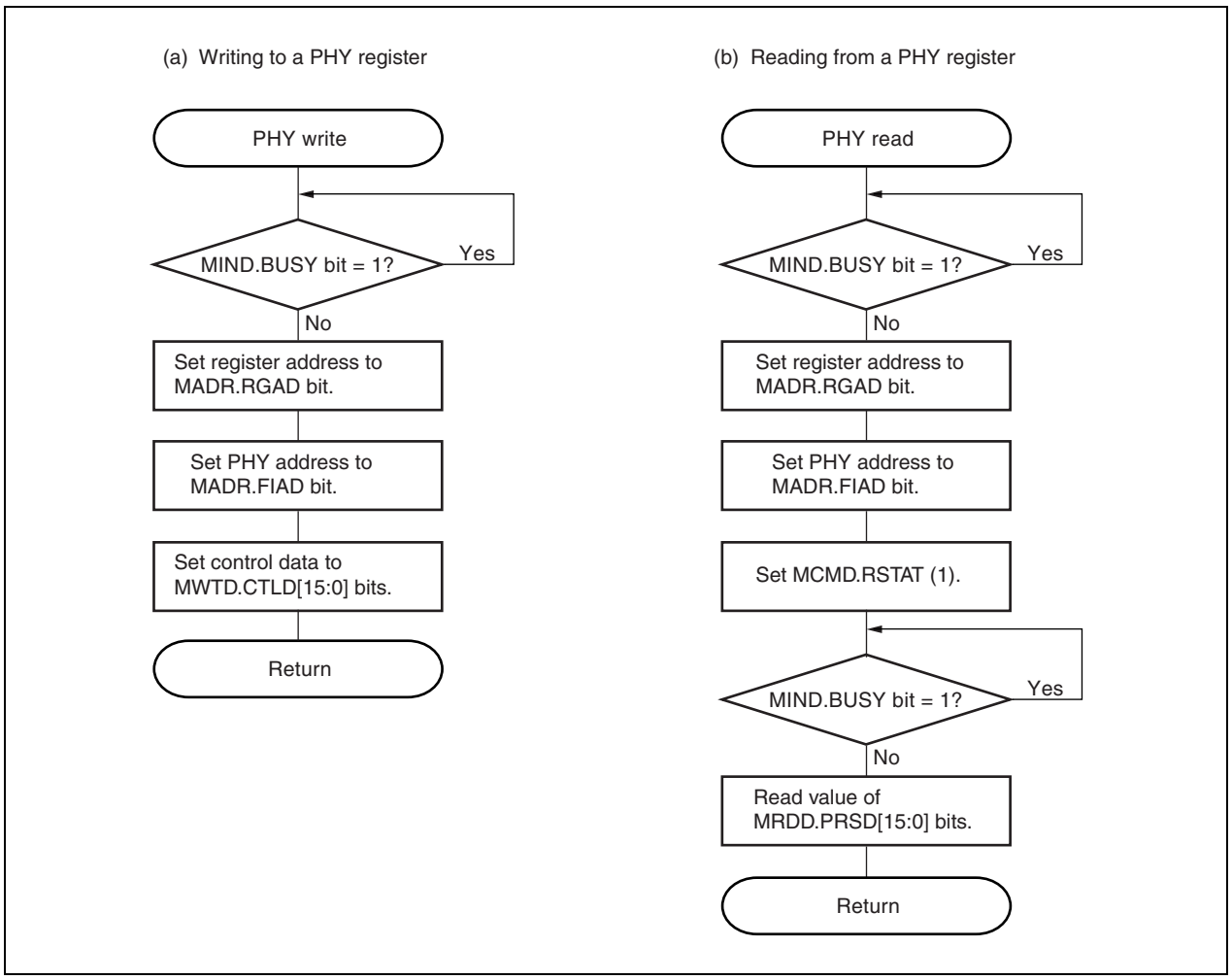
Address 002E 018CH

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

31	30	29	28	27	26	25	24
R51131	R51130	R51129	R51128	R51127	R51126	R51125	R51124
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
23	22	21	20	19	18	17	16
R51123	R51122	R51121	R51120	R51119	R51118	R51117	R51116
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
15	14	13	12	11	10	9	8
R51115	R51114	R51113	R51112	R51111	R51110	R5119	R5118
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
R5117	R5116	R5115	R5114	R5113	R5112	R5111	R5110
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
31 to 0	R511[31:0]	This counter is incremented if the receive packet length is 256 to 511 bytes. A packet containing a CRC error, symbol error, or length/type error is also counted.

Figure 23-15. Accessing a PHY Register



After reset: 01H[Note] R/W Address: FFFFF9FCH

	7	6	5	4	3	2	1	<0>
OCDM	0	0	0	0	0	0	0	OCDM0

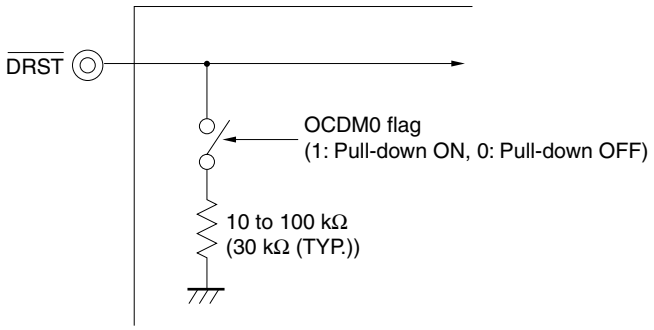
OCDM0	Operation mode
0	Selects normal operation mode (in which a pin that functions alternately as on-chip debug function pin is used as a port/peripheral function pin) and disconnects the on-chip pull-down resistor of the P54/INTP11/$\overline{\text{DRST}}$ pin.
1	When $\overline{\text{DRST}}$ pin is low: Normal operation mode (in which a pin that functions alternately as an on-chip debug function pin is used as a port/peripheral function pin) When $\overline{\text{DRST}}$ pin is high: On-chip debug mode (in which a pin that functions alternately as an on-chip debug function pin is used as an on-chip debug mode pin)

Note $\overline{\text{RESET}}$ input sets this register to 01H. After reset by the WDT2RES signal, clock monitor (CLM), or low-voltage detector (LVI), however, the value of the OCDM register is retained.

Cautions 1. When using the DDI, DDO, DCK, and DMS pins not as on-chip debug pins but as port pins after external reset, any of the following actions must be taken.

- **Input a low level to the P54/INTP11/$\overline{\text{DRST}}$ pin.**
- **Set the OCDM0 bit. In this case, take the following actions.**
  <1> Clear the OCDM0 bit to 0.
  <2> Fix the P54/INTP11/$\overline{\text{DRST}}$ pin to low level until <1> is completed.

2. The $\overline{\text{DRST}}$ pin has an on-chip pull-down resistor. This resistor is disconnected when the OCDM0 flag is set to 0.



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Symbol	Name	Unit	Page
C0MDATA226	CAN0 message data byte 2 register 26	CAN	1104
C0MDATA227	CAN0 message data byte 2 register 27	CAN	1104
C0MDATA228	CAN0 message data byte 2 register 28	CAN	1104
C0MDATA229	CAN0 message data byte 2 register 29	CAN	1104
C0MDATA230	CAN0 message data byte 2 register 30	CAN	1104
C0MDATA2300	CAN0 message data byte 23 register 00	CAN	1104
C0MDATA2301	CAN0 message data byte 23 register 01	CAN	1104
C0MDATA2302	CAN0 message data byte 23 register 02	CAN	1104
C0MDATA2303	CAN0 message data byte 23 register 03	CAN	1104
C0MDATA2304	CAN0 message data byte 23 register 04	CAN	1104
C0MDATA2305	CAN0 message data byte 23 register 05	CAN	1104
C0MDATA2306	CAN0 message data byte 23 register 06	CAN	1104
C0MDATA2307	CAN0 message data byte 23 register 07	CAN	1104
C0MDATA2308	CAN0 message data byte 23 register 08	CAN	1104
C0MDATA2309	CAN0 message data byte 23 register 09	CAN	1104
C0MDATA231	CAN0 message data byte 2 register 31	CAN	1104
C0MDATA2310	CAN0 message data byte 23 register 10	CAN	1104
C0MDATA2311	CAN0 message data byte 23 register 11	CAN	1104
C0MDATA2312	CAN0 message data byte 23 register 12	CAN	1104
C0MDATA2313	CAN0 message data byte 23 register 13	CAN	1104
C0MDATA2314	CAN0 message data byte 23 register 14	CAN	1104
C0MDATA2315	CAN0 message data byte 23 register 15	CAN	1104
C0MDATA2316	CAN0 message data byte 23 register 16	CAN	1104
C0MDATA2317	CAN0 message data byte 23 register 17	CAN	1104
C0MDATA2318	CAN0 message data byte 23 register 18	CAN	1104
C0MDATA2319	CAN0 message data byte 23 register 19	CAN	1104
C0MDATA2320	CAN0 message data byte 23 register 20	CAN	1104
C0MDATA2321	CAN0 message data byte 23 register 21	CAN	1104
C0MDATA2322	CAN0 message data byte 23 register 22	CAN	1104
C0MDATA2323	CAN0 message data byte 23 register 23	CAN	1104
C0MDATA2324	CAN0 message data byte 23 register 24	CAN	1104
C0MDATA2325	CAN0 message data byte 23 register 25	CAN	1104
C0MDATA2326	CAN0 message data byte 23 register 26	CAN	1104
C0MDATA2327	CAN0 message data byte 23 register 27	CAN	1104
C0MDATA2328	CAN0 message data byte 23 register 28	CAN	1104
C0MDATA2329	CAN0 message data byte 23 register 29	CAN	1104
C0MDATA2330	CAN0 message data byte 23 register 30	CAN	1104
C0MDATA2331	CAN0 message data byte 23 register 31	CAN	1104
C0MDATA300	CAN0 message data byte 3 register 00	CAN	1104
C0MDATA301	CAN0 message data byte 3 register 01	CAN	1104
C0MDATA302	CAN0 message data byte 3 register 02	CAN	1104

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Symbol	Name	Unit	Page
CF1TX	CSIF1 transmit data register	CSIF	900
CF1TXL	CSIF1 transmit data register L	CSIF	900
CF2CTL0	CSIF2 control register 0	CSIF	901
CF2CTL1	CSIF2 control register 1	CSIF	904
CF2CTL2	CSIF2 control register 2	CSIF	905
CF2RIC	Interrupt control register	INTC	1577
CF2RX	CSIF2 receive data register	CSIF	900
CF2RXL	CSIF2 receive data register L	CSIF	900
CF2STR	CSIF2 status register	CSIF	907
CF2TIC	Interrupt control register	INTC	1577
CF2TX	CSIF2 transmit data register	CSIF	900
CF2TXL	CSIF2 transmit data register L	CSIF	900
CF3CTL0	CSIF3 control register 0	CSIF	901
CF3CTL1	CSIF3 control register 1	CSIF	904
CF3CTL2	CSIF3 control register 2	CSIF	905
CF3RIC	Interrupt control register	INTC	1577
CF3RX	CSIF3 receive data register	CSIF	900
CF3RXL	CSIF3 receive data register L	CSIF	900
CF3STR	CSIF3 status register	CSIF	907
CF3TIC	Interrupt control register	INTC	1577
CF3TX	CSIF3 transmit data register	CSIF	900
CF3TXL	CSIF3 transmit data register L	CSIF	900
CF4CTL0	CSIF4 control register 0	CSIF	901
CF4CTL1	CSIF4 control register 1	CSIF	904
CF4CTL2	CSIF4 control register 2	CSIF	905
CF4RIC	Interrupt control register	INTC	1577
CF4RX	CSIF4 receive data register	CSIF	900
CF4RXL	CSIF4 receive data register L	CSIF	900
CF4STR	CSIF4 status register	CSIF	907
CF4TIC	Interrupt control register	INTC	1577
CF4TX	CSIF4 transmit data register	CSIF	900
CF4TXL	CSIF4 transmit data register L	CSIF	900
CF5CTL0	CSIF5 control register 0	CSIF	901
CF5CTL1	CSIF5 control register 1	CSIF	904
CF5CTL2	CSIF5 control register 2	CSIF	905
CF5RIC	Interrupt control register	INTC	1577
CF5RX	CSIF5 receive data register	CSIF	900
CF5RXL	CSIF5 receive data register L	CSIF	900
CF5STR	CSIF5 status register	CSIF	907
CF5TIC	Interrupt control register	INTC	1577
CF5TX	CSIF5 transmit data register	CSIF	900