Renesas Electronics America Inc - UPD70F3784GJ-GAE-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	76K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3784gj-gae-ax

(3) Port DH mode control register (PMCDH)

(1/2)

(a) V850ES/JH3-E

After reset: 00H R/W Address: FFFFF046H

	7	6	5	4	3	2	1	0
PMCDH	0	0	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0

PMCDH5	Specification of PDH5 pin operation mode
0	I/O port
1	A21 output/$\overline{\text{SCKF4}}$ I/O

PMCDH4	Specification of PDH4 pin operation mode
0	I/O port
1	A20 output/SOF4 output/RXDB0 input

PMCDH3	Specification of PDH3 pin operation mode
0	I/O port
1	A19 output/SIF4 input/TXDB0 output

PMCDH2	Specification of PDH2 pin operation mode
0	I/O port
1	A18 output/$\overline{\text{SCKE1}}$ I/O

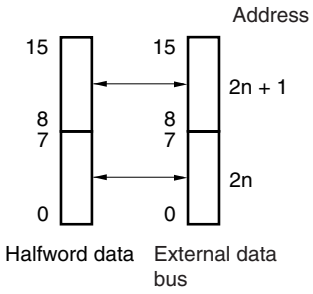
PMCDH1	Specification of PDH1 pin operation mode
0	I/O port
1	A17 output/SOE1 output

PMCDH0	Specification of PDH0 pin operation mode
0	I/O port
1	A16 output/SIE1 input

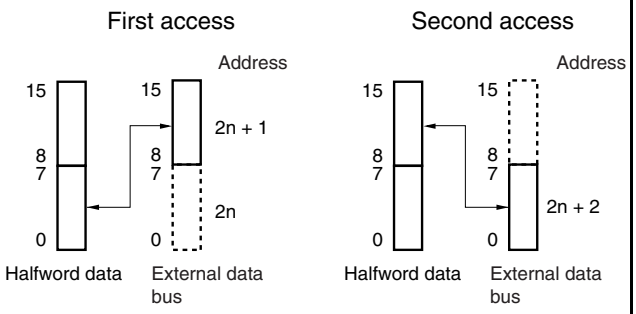
(3) Halfword access (16 bits)

(a) 16-bit data bus width

<1> Access to even address (2n)



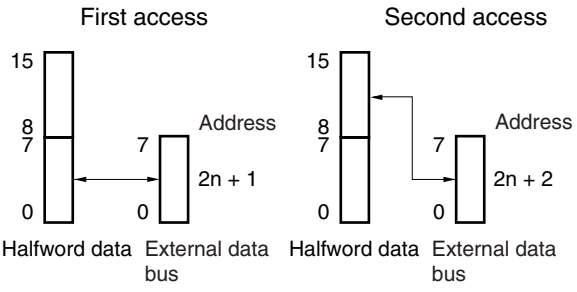
<2> Access to odd address (2n + 1)



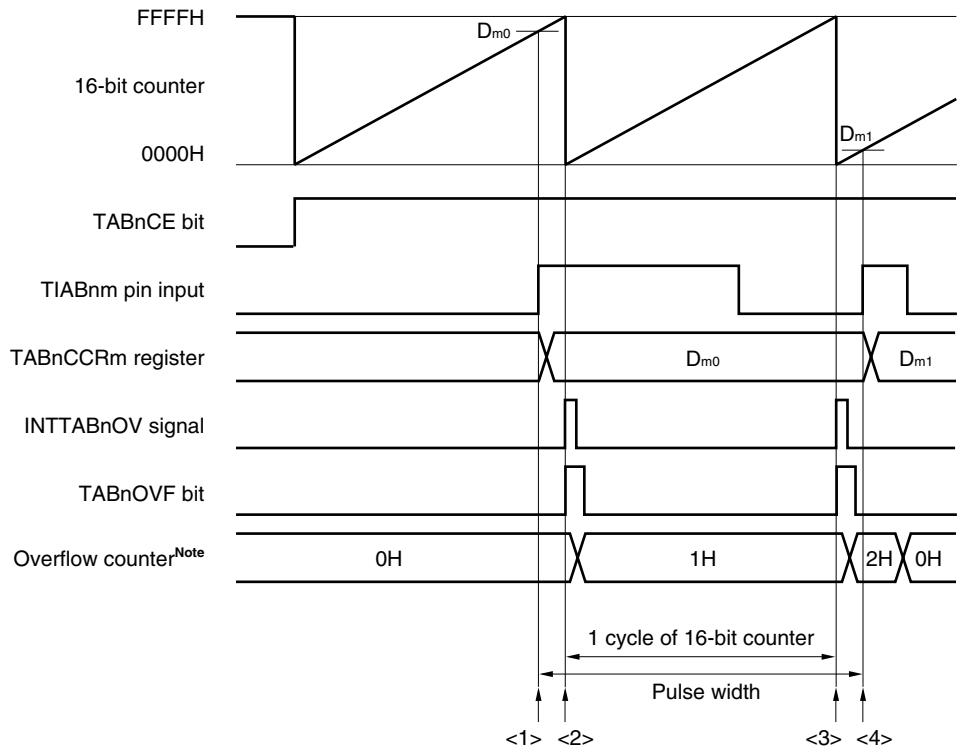
(b) 8-bit data bus width

<1> Access to even address (2n)

<2> Access to odd address (2n + 1)



Example when capture trigger interval is long



Note The overflow counter is set arbitrarily by software in the internal RAM.

<1> Read the TABnCCRm register (setting of the default value of the TIABnm pin input).

<2> An overflow occurs. Increment the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

<3> An overflow occurs a second time. Increment (+1) the overflow counter and clear the overflow flag to 0 in the overflow interrupt servicing.

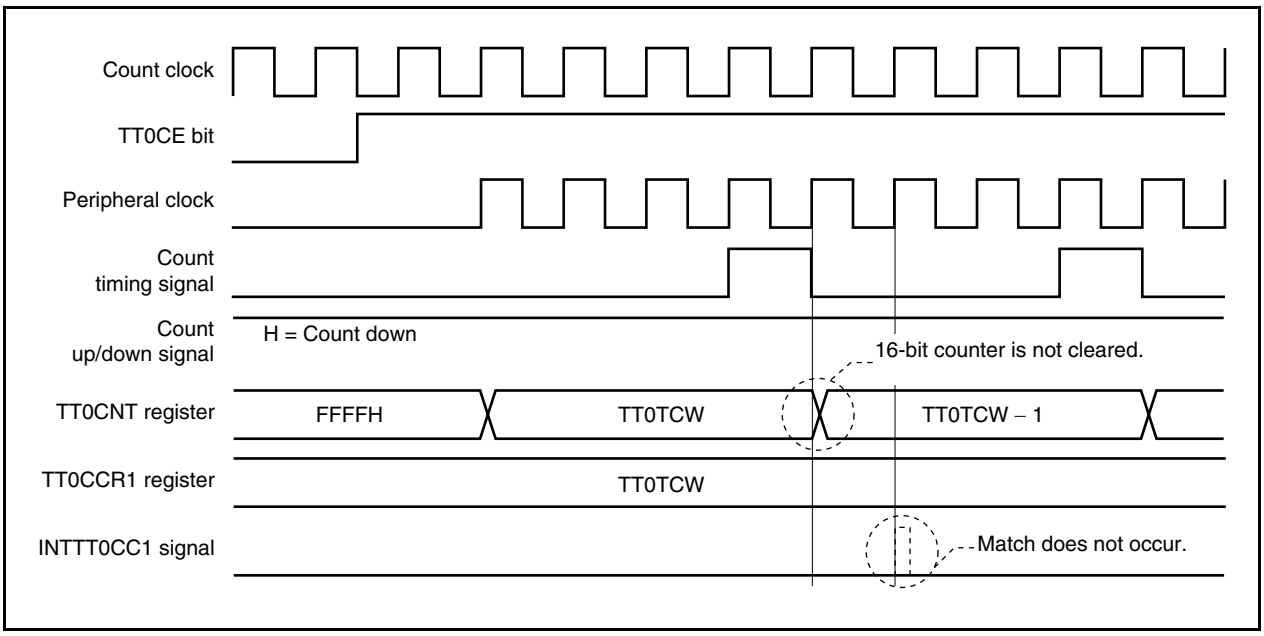
<4> Read the TABnCCRm register.
Read the overflow counter.
When the overflow counter is "N", the pulse width can be calculated by ($N \times 10000H + D_{m1} - D_{m0}$).
In this example, the pulse width is ($20000H + D_{m1} - D_{m0}$) because an overflow occurs twice.
Clear the overflow counter (0H).

Remark m = 0 to 3,
n = 0, 1

(7) Notes on using encoder count function

(a) If compare match interrupt is not generated immediately after operation is started

If a value which is the same as that of the TT0TCW register is set to the TT0CCR0 or TT0CCR1 register and the counter operation is started when the TT0CTL2.TT0ECC bit = 0, and if the count value (TT0TCW) of the 16-bit counter matches the value of the CCRn buffer register immediately after the start of the operation, the match is masked and the compare match interrupt request signal (INTTT0CCn) is not generated (n = 0, 1). In addition, the 16-bit counter is not cleared to 0000H by setting the TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits.



(2/2)

HZA0DCTn	High-impedance output trigger bit
0	No operation
1	Pins are made to go into a high-impedance state by software and the HZA0DCFn bit is set to 1.

- If an edge indicating abnormality is input to the external pin (which is detected according to the setting of the HZA0DCNn and HZA0DCPn bits), the HZA0DCTn bit is invalid even if it is set to 1.
- The HZA0DCTn bit is always 0 when it is read because it is a software-triggered bit.
- The HZA0DCTn bit is invalid even if it is set to 1 when the HZA0DCEn bit = 0.
- Simultaneously setting the HZA0DCTn and HZA0DCCn bits to 1 is prohibited.

HZA0DCCn	High-impedance output control clear bit
0	No operation
1	Pins that have gone into a high-impedance state are output-enabled by software and the HZA0DCFn bit is cleared to 0.

- Pins can function as output pins when the HZA0DCM bit = 0, regardless of the status of the external pin.
- If an edge indicating abnormality is input to the external pin (which is set by the HZA0DCNn and HZA0DCPn bits) when the HZA0DCM bit = 1, the HZA0DCCn bit is invalid even if it is set to 1.
- The HZA0DCCn bit is always 0 when it is read.
- The HZA0DCCn bit is invalid even if it is set to 1 when the HZA0DCEn bit = 0.
- Simultaneously setting the HZA0DCTn and HZA0DCCn bits to 1 is prohibited.

HZA0DCFn	High-impedance output status flag
0	Indicates that output of the pin is enabled. • This bit is cleared to 0 when the HZA0DCEn bit = 0. • This bit is cleared to 0 when the HZA0DCCn bit = 1.
1	Indicates that the pin goes into a high-impedance state. • This bit is set to 1 when the HZA0DCTn bit = 1. • This bit is set to 1 when an edge indicating abnormality is input to the external pin (which is detected according to the setting of the HZA0DCNn and HZA0DCPn bits).

(10) Standby mode

Because the A/D converter stops operating in the STOP mode, the conversion results are invalid, so power consumption can be reduced. Operations are resumed after the STOP mode is released, but the A/D conversion results after the STOP mode is released are invalid. When using the A/D converter after the STOP mode is released, clear the ADA0M0.ADA0CE bit to 0 before setting the STOP mode or after releasing the STOP mode, then set the ADA0CE bit to 1 after releasing the STOP mode.

In the IDLE1, IDLE2, or subclock operation mode, operation continues. To lower the power consumption, therefore, clear the ADA0M0.ADA0CE bit to 0. In the IDLE1 and IDLE2 modes, since the analog input voltage value cannot be retained, the A/D conversion results after the IDLE1 and IDLE2 modes are released are invalid. The results of conversions before the IDLE1 and IDLE2 modes were set are valid.

(11) High-speed conversion mode

In the high-speed conversion mode, rewriting the ADA0M0, ADA0M2, ADA0S, ADA0PFM, and ADA0PFT registers and trigger input during the stabilization time are prohibited.

(12) A/D conversion time

The A/D conversion time is the total of the stabilization time, conversion time, wait time, and trigger response time (for details of these times, refer to **Table 15-2 Conversion Time Selection in Normal Conversion Mode (ADA0HS1 Bit = 0)** and **Table 15-3 Conversion Time Selection in High-Speed Conversion Mode (ADA0HS1 Bit = 1)**).

During A/D conversion in the normal conversion mode, if the ADA0M0, ADA0M2, ADA0S, ADA0PFM, and ADA0PFT registers are written or a trigger is input, reconversion is carried out. However, if the stabilization time end timing conflicts with writing to these registers, or if the stabilization time end timing conflicts with the trigger input, a stabilization time of 64 clocks is reinserted.

If a conflict occurs again with the reinserted stabilization time end timing, the stabilization time is reinserted. Therefore do not set the trigger input interval and control register write interval to 64 clocks or lower.

(13) Variation of A/D conversion results

The results of A/D conversion may vary due to a fluctuation in the supply voltage or the effect of noise. To reduce this variation, take countermeasures with the program such as averaging the A/D conversion results.

(14) A/D conversion result hysteresis characteristics

The successive comparison type A/D converter holds the analog input voltage in the internal sample & hold capacitor and then performs A/D conversion. After A/D conversion has finished, the analog input voltage remains in the internal sample & hold capacitor. As a result, the following phenomena may occur.

- When the same channel is used for A/D conversions, if the voltage is higher or lower than the previous A/D conversion, then hysteresis characteristics may appear in which the conversion result is affected by the previous value. Thus, even if the conversion is performed at the same potential, the result may vary.
- When switching the analog input channel, hysteresis characteristics may appear in which the conversion result is affected by the previous channel value. This is because one A/D converter is used for the A/D conversions. Thus, even if the conversion is performed at the same potential, the result may vary.

(2) UARTBn status register (UBnSTR)

The UBnSTR register indicates the transfer status and reception error contents while UARTBn is transmitting data. The status flag that indicates the transfer status during transmission indicates the data retention status of the transmit shift register and transmit data register (the UBnTX register in the single mode or transmit FIFO in the FIFO mode). The status flag that indicates a reception error holds its status until it is cleared to 0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Caution When the UBnCTL0.UBnPWR bit or UBnCTL0.UBnRXE bit is set to 0, or when 0 is written to the UBnSTR register, the UBnSTR.UBnOVF, UBnSTR.UBnPE, UBnSTR.UBnFE, and UBnSTR.UBnOVE bits are cleared to 0.

After reset: 00H R/W Address: UB0STR FFFFFB84H, UB1STR FFFFFBA4H

	<7>	6	5	4	<3>	<2>	<1>	<0>
UBnSTR (n = 0, 1)	UBnTSF	0	0	0	UBnOVF	UBnPE	UBnFE	UBnOVE

UBnTSF	Transfer status flag
0	• In single mode (UBnFIC0.UBnMOD bit = 0) Data to be transferred to the transmit shift register and UBnTX register does not exist (cleared (0) when UBnCTL0.UBnPWR bit = 0 or UBnCTL0.UBnTXE bit = 0). • In FIFO mode (UBnFIC0.UBnMOD bit = 1) Data to be transferred to the transmit shift register and transmit FIFO does not exist (cleared (0) when UBnCTL0.UBnPWR bit = 0 or UBnCTL0.UBnTXE bit = 0).
1	• In single mode (UBnFIC0.UBnMOD bit = 0) Data to be transferred to the transmit shift register or UBnTX register exists (transmission in progress). • In FIFO mode (UBnFIC0.UBnMOD bit = 1) Data to be transferred to the transmit shift register and transmit FIFO exists (transmission in progress).
The value of the UBnTSF bit is reflected after two periods of f_{XX} have elapsed, after the transmit data is written to the UBnTX register. Therefore, exercise care when referencing the UBnTSF bit after transmit data has been written to the UBnTX	

UBnOVF	Overflow flag
0	Overflow did not occur.
1	Overflow occurred (during reception).
• The UBnOVF bit is valid only in the FIFO mode (when UBnFIC0.UBnMOD bit = 1), and invalid in the single mode (when UBnFIC0.UBnMOD bit = 0). • If an overflow occurs, the received data is not written to receive FIFO but discarded.	

(2/2)

CEnCKS2	CEnCKS1	CEnCKS0	Set Value (N)	Base clock (f_{XCLK})	Mode
0	0	0	0	f_{XX}/2	Master mode
0	0	1	1	f_{XX}/4	Master mode
0	1	0	2	f_{XX}/8	Master mode
0	1	1	3	f_{XX}/16	Master mode
1	0	0	4	f_{XX}/32	Master mode
1	0	1	5	f_{XX}/64	Master mode
1	1	0	6	f_{XX}/128	Master mode
1	1	1	–	External clock ($\overline{SCKEn}$)	Slave mode
• If the CEnCKS2 to CEnCKS0 bits are cleared to 000, setting the CEnMDL2 to CEnMDL0 bit to 001 is prohibited.					

Remark f_{XX}: Main clock frequency

(2) Function of CSI data buffer registers 0, 1 (CSIBUF0, CSIBUF1)

By consecutively writing the transmit data to the CEnTX0 register from where it is transferred, up to sixteen 16-bit data can be stored in the CSIBUFn register while the CSIBUFn pointer for writing is automatically incremented (n = 0, 1).

The condition under which transfer is to be started (CEnSTR.CEnEMF bit = 0) is satisfied when data is written to the lower 8 bits (CEnTX0L register) of the CEnTX0 register. If a transfer data length of 9 bits or more is specified (CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 bits = 0000 or 1001 to 1111), data must be written to the CEnTX0 register in 16-bit units or to the CEnTX0H and CEnTX0L registers, in that order, in 8-bit units. If the transfer data length is set to 8 bits (CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 bits = 1000), data must be written to the CEnTX0L register in 8-bit units or to the CEnTX0 register in 16-bit units. (If data is written to the CEnTX0L register in 16-bit units, however, the higher 8 bits of the data (of the CEnTX0H register) are ignored and not transferred).

The CEnSTR.CEnFLF register is set to 1 when 16 data exist in the CSIBUFn register and outputs a CSIBUFn overflow interrupt (INTCEnTIOF) when the CEnFLF bit = 1 and when the 17th transfer data is written (17th transfer data is not written and ignored).

Sixteen data exist in the CSIBUFn register in the single mode (CEnCTL0.CEnTMS bit = 1) when “CSIBUFn pointer value for writing = CSIBUFn pointer value for SIOn loading, and CEnSTR.CEnFLF bit = 1”. When the CSIBUFn pointer for SIOn loading is incremented after completion of transfer while CEnFLF bit = 1, the CEnFLF bit is cleared to 0 and the next transmission data can be written.

In the continuous mode (CEnCTL0.CEnTMS bit = 1), when one data has been transferred, the CEnFLF bit is cleared to 0, but writing the next transmission data is prohibited (if a receive operation is processed, the received data is stored in the CSIBUFn register. Therefore, if the transmission data is written to the register, the received data is overwritten and destroyed).

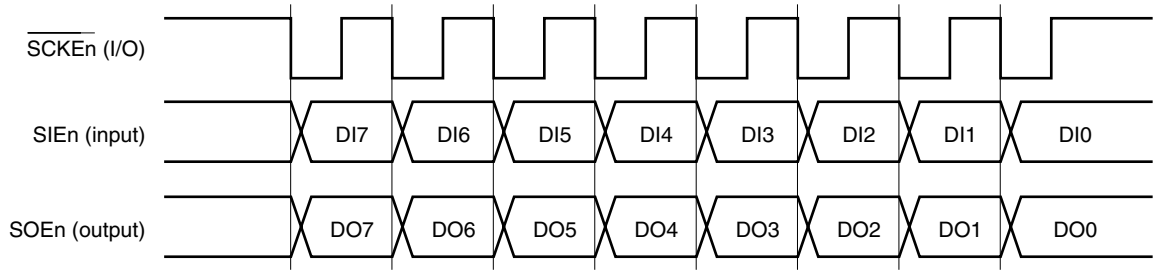
(3) Data transfer direction specification function

The data transfer direction can be changed by using the CEnCTL0.CEnDIR bit (n = 0, 1).

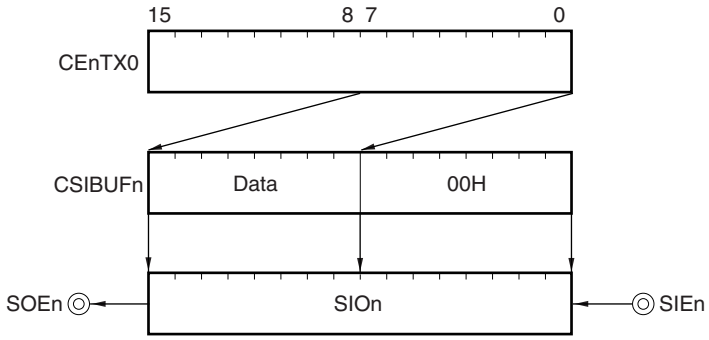
(a) MSB first (CEnDIR bit = 0)

Figure 18-4. Transfer Data Length: 8 Bits (CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 bits = 1000), Transfer Direction: MSB First (CEnCTL0.CEnDIR bit = 0) (1/2)

(i) Transfer direction: MSB first



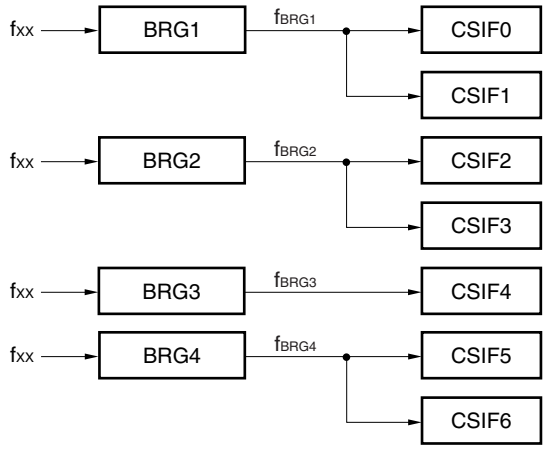
(ii) Writing from CEnTX0 register to CSIBUFn register



Remark n = 0, 1

19.8 Baud Rate Generator

The BRG1 to BRG4 baud rate generators are connected to CSIF0 to CSIF6 as shown in the following block diagram.



(1) Prescaler mode registers 1 to 4 (PRSM1 to PRSM4)

The PRSMm registers control generation of the baud rate signal for CSIF.

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: PRSM1 FFFFF320H, PRSM2 FFFFF324H, PRSM3 FFFFF328H, PRSM4 FFFFF32CH

PRSMm (m = 1 to 4)

7	6	5	<4>	3	2	1	0
0	0	0	BGCEm	0	0	BGCSm1	BGCSm0

BGCEm	Baud rate output
0	Disabled
1	Enabled

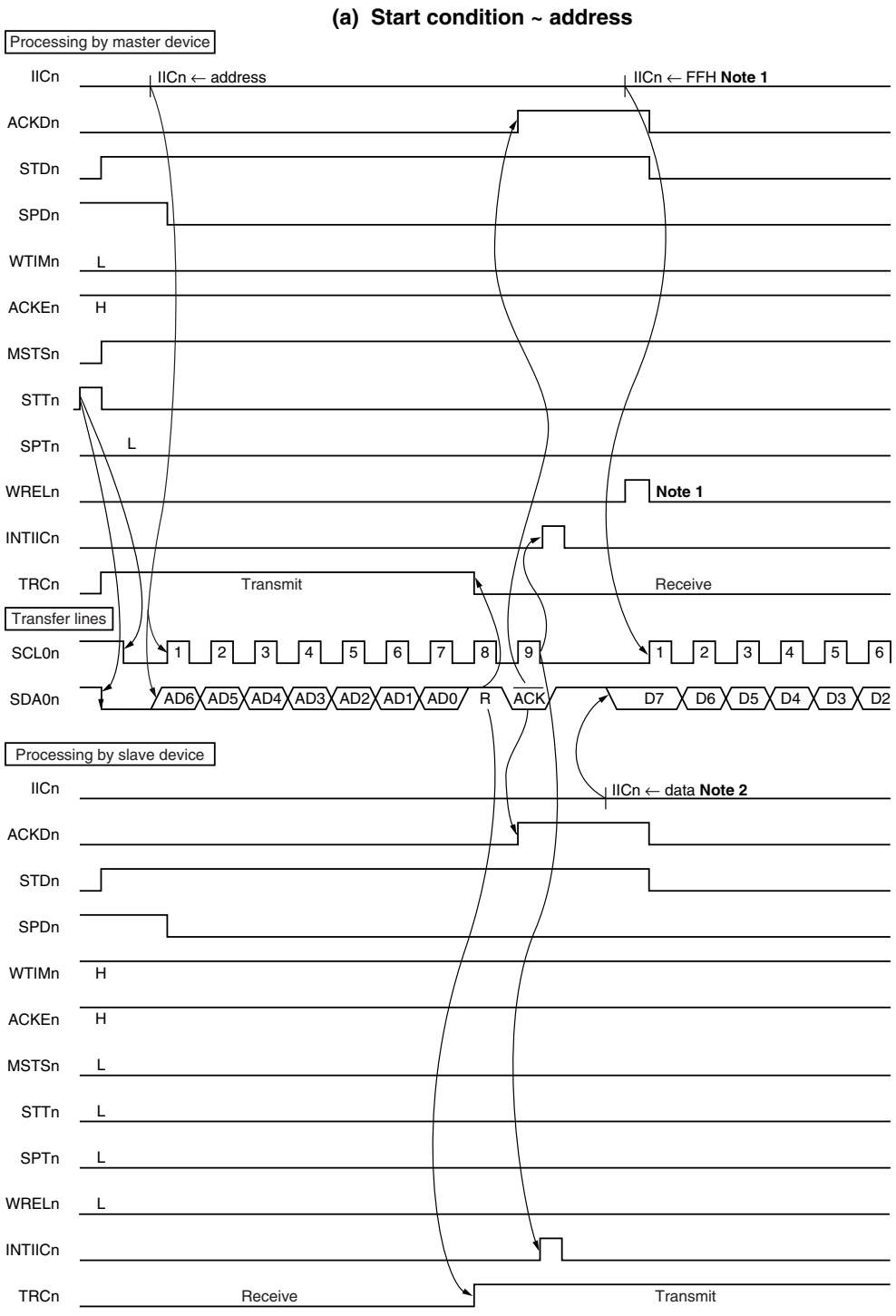
BGCSm1	BGCSm0	Input clock selection (f_{BGCSm})	Setting value (k)
0	0	f_{XX}	0
0	1	$f_{XX}/2$	1
1	0	$f_{XX}/4$	2
1	1	$f_{XX}/8$	3

Cautions 1. Do not rewrite the PRSMm register during operation.

2. Set the PRSMm register before setting the BGCEm bit to 1.

2. Be sure to set bits 7 to 5, 3, and 2 to "0".

Figure 20-25. Example of Slave to Master Communication
(When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected) (1/3)

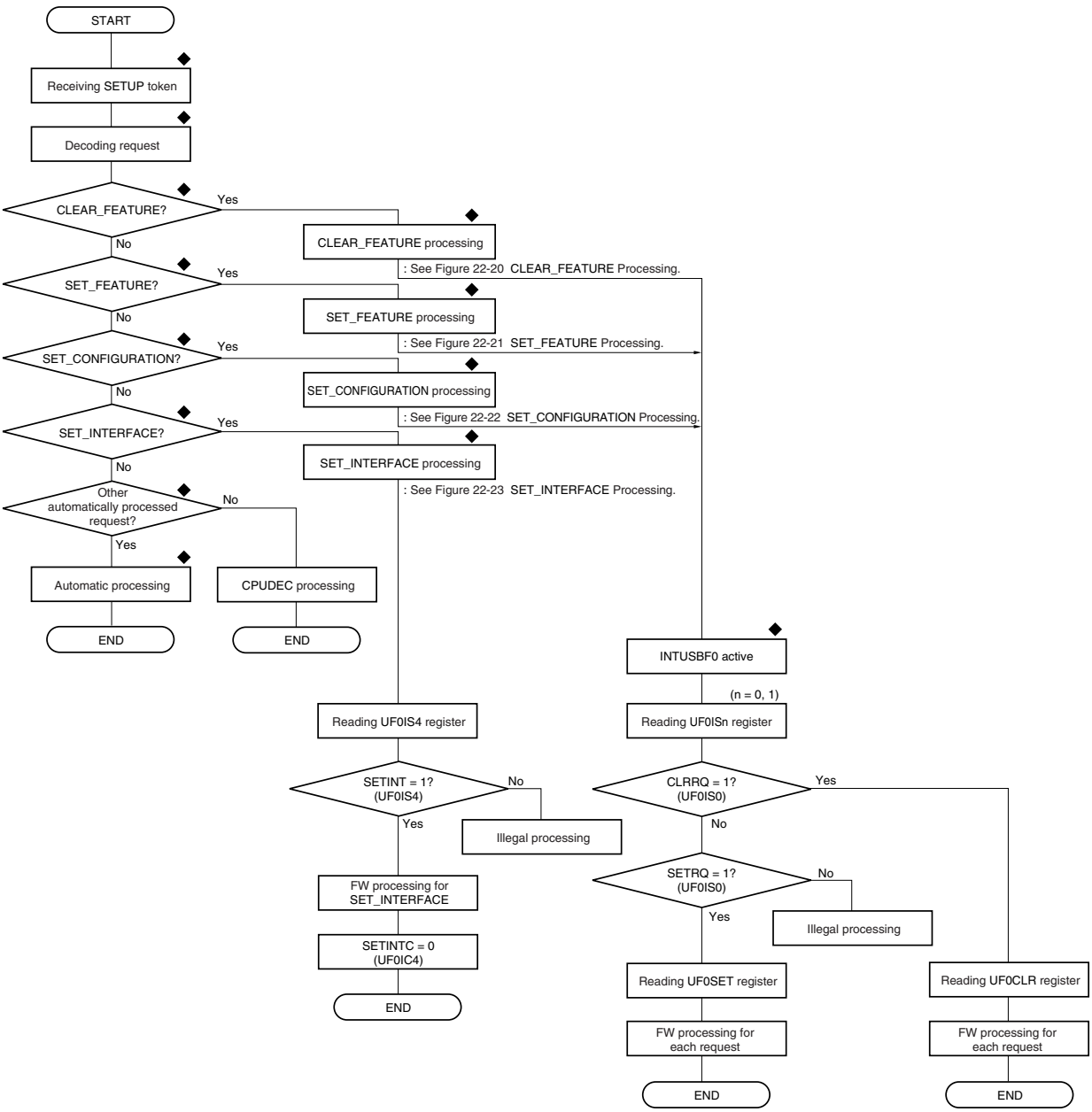


Notes 1. To cancel the master wait state, write FFH to IICn or set WRELn.

2. Cancel the wait during a slave transmission by writing to IICn, not by setting WRELn.

Remark n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

Figure 22-19. Automatically Processed Requests for Control Transfer



Remark ♦: Processing by hardware

Table 23-3. Register List (FIFO Controller)

Offset Address	Symbol	Register Name	R/W	Bit Manipulation Unit			Default Value
				8	16	32	
002E 0200H	MFFCONT	FIFO controller control register	R/W			√	00000000H
002E 0204H	RSTCNT	Software reset control register	R/W			√	00000000H
002E 0218H	FLOWTHRESH	Flow control threshold value register	R/W			√	06000200H
002E 021CH	PAUSETM	Pause timer value register	R/W			√	7FFFFFFFH
002E 0220H	RXERSEL	Receive error selection register	R/W			√	00000001H
002E 0230H	TXSTMONI1	Transmission status monitor 1 register	R			√	00000000H
002E 0234H	TXSTMONI2	Transmission status monitor 2 register	R			√	00000000H
002E 0238H	TXFINF1	Transmission status 1 register	R			√	00000800H
002E 023CH	TXFINF2	Transmission status 2 register	R			√	00000001H
002E 0240H	RXSTMONI	Reception status monitor register	R			√	00000000H
002E 0244H	RXFINF1	Reception status 1 register	R			√	00000000H
002E 0248H	RXFINF2	Reception status 2 register	R			√	00000800H
002E 024CH	RXFINF3	Reception status 3 register	R			√	00000001H
002E 0250H	FSTATUS	FIFO status interrupt register	R			√	00000000H
002E 0254H	FSTATUS_MASK	FIFO status interrupt mask register	R/W			√	01011FFFH
002E 0258H	TXSTATUS	Transmission status interrupt register	R			√	00000000H
002E 025CH	TXSTATUS_MASK	Transmission status interrupt mask register	R/W			√	000101FFH
002E 0260H	RXSTATUS	Reception status interrupt register	R			√	00000000H
002E 0264H	RXSTATUS_MASK	Reception status interrupt mask register	R/W			√	00007FFFH
002E 0270H	TXABTCNT	Transmission abort counter	R/W			√	00000000H
002E 0274H	RXABTCNT	Reception abort counter	R/W			√	00000000H

Table 23-4. Register List (DMAC in Ethernet Controller)

Offset Address	Symbol	Register Name	R/W	Bit Manipulation Unit			Default Value
				8	16	32	
002E 0300H	ETHMODE	Core function control register	R/W			√	00000000H
002E 0304H	INTMS	Interrupt register	R/W			√	07000700H
002E 0308H	TRANSCTL	Transmission control register	R/W			√	00030000H
002E 030CH	SFTRST	Software reset register	R/W			√	00000000H
002E 0310H	DMACM	DMA controller mode control register	R/W			√	00000010H
002E 0320H	RXDP	Reception descriptor pointer register	R/W			√	FFFFFFFCH
002E 0324H	LSTRXDP	Last reception descriptor pointer register	R			√	FFFFFFFCH
002E 0328H	TXDP	Transmission descriptor pointer register	R/W			√	FFFFFFFCH
002E 032CH	LSTTXDP	Last transmission descriptor pointer register	R			√	FFFFFFFCH

(14) FSTATUS: FIFO status interrupt register

An INTETMFS interrupt (FIFO status interrupt) is generated if it is not masked by the FSTATUS_MASK register. The INTETMFS interrupt signal is kept asserted while any bit of this register is set. If the interrupt source masked by a bit of the FSTATUS_MASK register has been generated, the corresponding bit of this register is set as well. All the bits of the FSTATUS register are cleared when the register is read.

Access This register is read-only, in 32-bit units.

Address 002E 0250H

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

Cautions 1. The FIFO status interrupt status register is cleared when it is read. It is recommended to copy interrupt sources to variables so that several interrupt sources that are generated at the same time can be detected.

2. Be sure to set bits 31 to 25, 23 to 17, 15 to 13, 9, 8, 5, and 2 to "0".

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	TACOF
R	R	R	R	R	R	R	R

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	RACOF
R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8
0	0	0	TSUP	TFNRTY	TFWE	0	0
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
RFFE	RSUP	0	RFWE	RFOF	0	RFFLW	RFZP
R	R	R	R	R	R	R	R

(1/2)

Bit	Name	Description
24	TACOF	This bit is set to 1 when the TXABTCNT register (TX abort counter) overflows.
16	RACOF	This bit is set to 1 when the RXABCNT register (RX abort counter) overflows.
12	TSUP	TX status update This bit is set to 1 when the transmission status is updated in the TXSTMONI1 and TXSTMONI2 registers.
11	TFNRTY	Transmit FIFO abort (transmit FIFO no retry) This bit is set to 1 if transmission has failed and the data in the FIFO has been discarded. In this case, TXABTCNT is incremented.
10	TFWE	This bit is set to 1 if a transmit FIFO write error has occurred.

(2) INTMS: Interrupt register

Access This register can be read and written in 32-bit units.

Address 002E 0304H

Default value 0700 0700H. This register is cleared to its default value by all types of resets.

Caution Be sure to set bits 31 to 27, 23 to 19, 15 to 11, and 7 to 3 to "0".

Remark The RBEI, RECI, RXI, TBEI, TECI, and TXI bits of the INTMS register are cleared when they are read.

31	30	29	28	27	26	25	24
0	0	0	0	0	RBEMSK	RECMSK	RXMSK
R	R	R	R	R	R/W	R/W	R/W

23	22	21	20	19	18	17	16
0	0	0	0	0	RBEI	RECI	RXI
R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8
0	0	0	0	0	TBEMSK	TECMSK	TXMSK
R	R	R	R	R	R/W	R/W	R/W

7	6	5	4	3	2	1	0
0	0	0	0	0	TBEI	TECI	TXI
R	R	R	R	R	R	R	R

(1/2)

Bit	Name	Description
26	RBEMSK	This bit masks the RBEI interrupt of bit 18. 0: Interrupt enabled 1: Interrupt masked
25	RECMSK	This bit masks the RECI interrupt of bit 17. 0: Interrupt enabled 1: Interrupt masked
24	RXMSK	This bit masks the RXI interrupt of bit 16. 0: Interrupt enabled 1: Interrupt masked
18	RBEI	This bit indicates the occurrence of the receive data buffer access error interrupt. It is cleared when read. 0: Interrupt did not occur. 1: Interrupt occurred.

Table 24-1. DMA Start Factors (1/2)

IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0	Interrupt Source
0	0	0	0	0	0	DMA request by interrupt disabled
0	0	0	0	0	1	INTP01
0	0	0	0	1	0	INTP02
0	0	0	0	1	1	INTP05
0	0	0	1	0	0	INTP06
0	0	0	1	0	1	INTP13
0	0	0	1	1	0	INTP17
0	0	0	1	1	1	INTTAB0OV
0	0	1	0	0	0	INTTAB0CC0
0	0	1	0	0	1	INTTAB0CC1
0	0	1	0	1	0	INTTAB0CC2
0	0	1	0	1	1	INTTAB0CC3
0	0	1	1	0	0	INTTAB1OV_BASE[Note]
0	0	1	1	0	1	INTTAB1OV
0	0	1	1	1	0	INTTAB1CC0_BASE[Note]
0	0	1	1	1	1	INTTAB1CC0
0	1	0	0	0	0	INTTAB1CC1
0	1	0	0	0	1	INTTAB1CC2
0	1	0	0	1	0	INTTAB1CC3
0	1	0	0	1	1	INTTT0OV
0	1	0	1	0	0	INTTT0CC0
0	1	0	1	0	1	INTTT0CC1
0	1	0	1	1	0	INTTAA0OV
0	1	0	1	1	1	INTTAA0CC0
0	1	1	0	0	0	INTTAA0CC1
0	1	1	0	0	1	INTTAA1OV
0	1	1	0	1	0	INTTAA1CC0
0	1	1	0	1	1	INTTAA1CC1
0	1	1	1	0	0	INTTAA2CC0
0	1	1	1	0	1	INTTAA2CC1
0	1	1	1	1	0	INTTAA3CC0
0	1	1	1	1	1	INTTAA3CC1
1	0	0	0	0	0	INTTAA4CC0
1	0	0	0	0	1	INTTAA4CC1
1	0	0	0	1	0	INTTAA5CC0
1	0	0	0	1	1	INTTAA5CC1
1	0	0	1	0	0	INTTM0EQ0
1	0	0	1	0	1	INTTM1EQ0
1	0	0	1	1	0	INTTM2EQ0
1	0	0	1	1	1	INTTM3EQ0
1	0	1	0	0	0	INTCE0T/INTUC4R
1	0	1	0	0	1	INTCE0TIOF/INTUC4T

Note INTTAB1OV_BASE and INTTAB1CC0_BASE are the interrupt signals before culling by TABOP.

25.3.3 Priorities of maskable interrupts

The INTC performs multiple interrupt servicing in which an interrupt is acknowledged while another interrupt is being serviced. Multiple interrupts can be controlled by priority levels.

There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels that are specified by the interrupt priority level specification bit (xxPRn) of the interrupt control register (xxICn). When two or more interrupts having the same priority level specified by the xxPRn bit are generated at the same time, interrupt request signals are serviced in order depending on the priority level allocated to each interrupt request type (default priority level) beforehand. For more information, see **Table 25-2** and **Table 25-3**. The programmable priority control customizes interrupt request signals into eight levels by setting the priority level specification flag.

Note that when an interrupt request signal is acknowledged, the PSW.ID flag is automatically set to 1. Therefore, when multiple interrupts are to be used, clear the ID flag to 0 beforehand (for example, by placing the EI instruction in the interrupt service program) to set the interrupt enable mode.

Remark xx: Identification name of each peripheral unit (see **Table 25-4 Interrupt Control Register (xxICn)**)
n: Peripheral unit number (see **Table 25-4 Interrupt Control Register (xxICn)**).

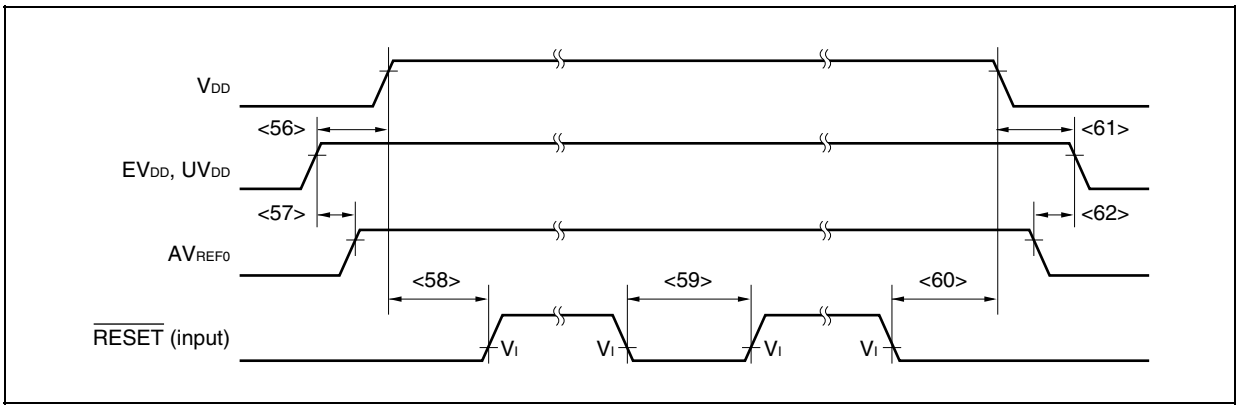
35.8 Basic Operation

(1) Power on/power off/reset timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0}, V_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Time from EV_{DD}, UV_{DD}↑ to V_{DD}↑	t_{REL}	<56>		0		ns
Time from EV_{DD}, UV_{DD}↑ to AV_{REF0}↑	t_{REA}	<57>		0	t_{REL}	ns
Time from V_{DD}↑ to $\overline{RESET}$↑	t_{RER}	<58>		500 + t_{REG} Note		ns
$\overline{RESET}$ low-level width	t_{WRSL}	<59>	Analog noise elimination (during flash erase/writing)	500		ns
			Analog noise elimination	500		ns
Time from $\overline{RESET}$↓ to V_{DD}↓	t_{FRE}	<60>		500		ns
Time from V_{DD}↓ to EV_{DD}, UV_{DD}↓	t_{FEL}	<61>		0		ns
Time from AV_{REF0}↓ to EV_{DD}, UV_{DD}↓	t_{FEA}	<62>		0	t_{FEL}	ns

Note Depends on the on-chip regulator characteristics.



(16/43)

Symbol	Name	Unit	Page
CE0CTL3	CSIE0 control register 3	CSIE	854
CE0RX0	CSIE0 receive data register 0	CSIE	846
CE0RX0H	CSIE0 receive data register 0H	CSIE	846
CE0RX0L	CSIE0 receive data register 0L	CSIE	846
CE0STR	CSIE0 status register	CSIE	855
CE0TIC	Interrupt control register	INTC	1577
CE0TIOFIC	Interrupt control register	INTC	1577
CE0TX0	CSIE0 transmit data register	CSIE	847
CE0TXH0	CSIE0 transmit data register H	CSIE	847
CE0TXL0	CSIE0 transmit data register L	CSIE	847
CE1CTL0	CSIE1 control register 0	CSIE	849
CE1CTL1	CSIE1 control register 1	CSIE	851
CE1CTL2	CSIE1 control register 2	CSIE	853
CE1CTL3	CSIE1 control register 3	CSIE	854
CE1RX0	CSIE1 receive data register	CSIE	846
CE1RX0H	CSIE1 receive data register H	CSIE	846
CE1RX0L	CSIE1 receive data register L	CSIE	846
CE1STR	CSIE1 status register	CSIE	855
CE1TIC	Interrupt control register	INTC	1577
CE1TIOFIC	Interrupt control register	INTC	1577
CE1TX0	CSIE1 transmit data register	CSIE	847
CE1TX0H	CSIE1 transmit data register H	CSIE	847
CE1TX0L	CSIE1 transmit data register L	CSIE	847
CF0CTL0	CSIF0 control register 0	CSIF	901
CF0CTL1	CSIF0 control register 1	CSIF	904
CF0CTL2	CSIF0 control register 2	CSIF	905
CF0RIC	Interrupt control register	INTC	1577
CF0RX	CSIF0 receive data register	CSIF	900
CF0RXL	CSIF0 receive data register L	CSIF	900
CF0STR	CSIF0 status register	CSIF	907
CF0TIC	Interrupt control register	INTC	1577
CF0TX	CSIF0 transmit data register	CSIF	900
CF0TXL	CSIF0 transmit data register L	CSIF	900
CF1CTL0	CSIF1 control register 0	CSIF	901
CF1CTL1	CSIF1 control register 1	CSIF	904
CF1CTL2	CSIF1 control register 2	CSIF	905
CF1RIC	Interrupt control register	INTC	1577
CF1RX	CSIF1 receive data register	CSIF	900
CF1RXL	CSIF1 receive data register L	CSIF	900
CF1STR	CSIF1 status register	CSIF	907
CF1TIC	Interrupt control register	INTC	1577