Renesas Electronics America Inc - UPD70F3785GJ-GAE-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	124K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3785gj-gae-ax

1.6.2 Internal units

(1) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) contribute to faster complex processing.

(2) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU. When an instruction is fetched from external memory space and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an instruction queue.

(3) Flash memory (ROM)

This is a 512/384/256 KB flash memory mapped to addresses 0000000H to 007FFFFH/0000000H to 005FFFFH/0000000H to 003FFFFH. It can be accessed from the CPU in one clock during instruction fetch.

(4) RAM

This is a 60 KB RAM mapped to addresses 3FF0000H to 3FFEFFFH. It can be accessed from the CPU in one clock during data access. An 16/64 KB data-only RAM is incorporated at addresses 00280000H to 00283FFFH/00280000H to 0028FFFFH.

(5) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP00 to INTP25) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed.

(6) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively. There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 8.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(7) Internal oscillator

An internal oscillator is provided on chip. The oscillation frequency is 220 kHz (TYP). The internal oscillator supplies the clock for watchdog timer 2 and timer M.

(8) Timer/counter

Six-channel 16-bit timer/event counter AA (TAA), two-channel 16-bit timer/event counter AB (TAB), one-channel 16-bit timer/event counter T (TMT), and four-channel 16-bit interval timer M (TMM) are provided on chip. The motor control function can be realized using TAB1 and TAA4 in combination.

(2/2)

(b) V850ES/JJ3-E

After reset: 00H R/W Address: FFFFF444H

	7	6	5	4	3	2	1	0
PMC2	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20

PMC27	Specification of P27 pin operation mode
0	I/O port
1	TIAB03 input/TOAB03 output/INTP21 input

PMC26	Specification of P26 pin operation mode
0	I/O port
1	TIAA31 input/TOAA31 output/INTP05 input/$\overline{\text{UDMAAK0}}$ output

PMC25	Specification of P25 pin operation mode
0	I/O port
1	$\overline{\text{SCKF1}}$ I/O/TIAA30 input/TOAA30 output/$\overline{\text{UDMARQ0}}$ input

PMC24	Specification of P24 pin operation mode
0	I/O port
1	SOF1 output/RXDC1 input/SCL00 I/O/INTP04 input

PMC23	Specification of P23 pin operation mode
0	I/O port
1	SIF1 input/TXDC1 output/SDA00 I/O/INTP03 input

PMC22	Specification of P22 pin operation mode
0	I/O port
1	TIAB01 input/TOAB01 output/RTC1HZ output/INTP02 input

PMC21	Specification of P21 pin operation mode
0	I/O port
1	TIAB00 input/TOAB00 output/RTCDIV output/RTCCL output

PMC20	Specification of P20 pin operation mode
0	I/O port
1	TIAB02 input/TOAB02 output/INTP01 input

PFCDH2	Specification of PDH2 pin alternate function
0	A18 output
1	$\overline{\text{SCKE1}}$ I/O

Caution The $\overline{\text{SCKE1}}$ function is assigned to the PDH2 pin as well as the P911 pin. When using the PDH2 pin for the $\overline{\text{SCKE1}}$ function, do not set the P911 pin to be used for this function.

PFCDH1	Specification of PDH1 pin alternate function
0	A17 output
1	SOE1 output

Caution The SOE1 function is assigned to the PDH1 pin as well as the P910 pin. When using the PDH1 pin for the SOE1 function, do not set the P910 pin to be used for this function.

PFCDH0	Specification of PDH0 pin alternate function
0	A16 output
1	SIE1 input

Caution The SIE1 function is assigned to the PDH0 pin as well as the P99 pin. When using the PDH0 pin for the SIE1 function, do not set the P99 pin to be used for this function.

Table 4-18. Using Port Pin as Alternate-Function Pin (8/13)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Name	I/O						
P93	TOAB1B2	Output	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFCE93 = 0	PFC93 = 0	
	TRGAB1Note 1	Input	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFCE93 = 0	PFC93 = 1	KRM3 (KRM) = 0
	KR3Note 1	Input	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFCE93 = 0	PFC93 = 1	TAB1ETS1, TAB1ETS0 (TAB1I0C1) = 0
	INTP14	Input	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFCE93 = 1	PFC93 = 0	
	A3Note 2	Output	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFCE93 = 1	PFC93 = 1	
P94	TOAB1T3	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 0	PFC94 = 0	
	TOAB13	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 0	PFC94 = 0	
	TIAB13Note 3	Input	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 0	PFC94 = 1	KRM2 (KRM) = 0
	KR4Note 3	Input	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 0	PFC94 = 1	TAB1TIS7, TAB1TIS6 (TAB1I0C1) = 0
	INTP15	Input	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 1	PFC94 = 0	
	A4Note 2	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFCE94 = 1	PFC94 = 1	
P95	TOAB1B3	Output	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFCE95 = 0	PFC95 = 0	
	EVTAB1Note 4	Input	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFCE95 = 0	PFC95 = 1	KRM5 (KRM) = 0
	KR5Note 4	Input	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFCE95 = 0	PFC95 = 1	TAB1EES1, TAB1EES0 (TAB1I0C1) = 0
	INTP16	Input	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFCE95 = 1	PFC95 = 0	
	A5Note 2	Output	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFCE95 = 1	PFC95 = 1	

Notes 1. KR3 and TRGAB1 are alternate functions. When using the pin for the TRGAB1 function, disable key return detection of KR3, which is the alternate function (set the KRM.KRM3 bit to 0). Also, when using the pin for the KR3 function, disable edge detection of TRGAB1, which is the alternate function (set the TAB1IOC2.TAB1ETS1 and TAB1ETS0 bits to 00).

2. When using as the A0 to A15 pins, be sure to set all 16 bits of the PMC9 register to FFFFH at once.

3. KR4 and TIAB13 are alternate functions. When using the pin for the TIAB13 function, disable key return detection of KR4, which is the alternate function (set the KRM.KRM4 bit to 0). Also, when using the pin for the KR4 function, disable edge detection of TIAB13, which is the alternate function (set the TAB1IOC1.TAB1IS7 and TAB1IS6 bits to 00).

4. KR5 and EVTAB1 are alternate functions. When using the pin for the EVTAB1 function, disable key return detection of KR5, which is the alternate function (set the KRM.KRM5 bit to 0). Also, when using the pin for the KR5 function, disable edge detection of EVTAB1, which is the alternate function (set the TAB1IOC2.TAB1EES1 and TAB1EES0 bits to 00).

6.4 Operation

6.4.1 Operation of each clock

The following table shows the operation status of each clock.

Table 6-1. Operation Status of Each Clock

Register Setting and Operation Status / Target Clock	PCC Register								
	CLK Bit = 0, MCK Bit = 0					CLS Bit = 1, MCK Bit = 0		CLS Bit = 1, MCK Bit = 1	
	During Reset	During Oscillation Stabilization Time Count	HALT Mode	IDLE1, IDLE2 Mode	STOP Mode	Subclock Mode	Sub-IDLE Mode	Subclock Mode	Sub-IDLE Mode
Main clock oscillator (f_X)	×	○	○	○	×	○	○	×	×
Subclock oscillator (f_{XT})	○	○	○	○	○	○	○	○	○
CPU clock (f_{CPU})	×	×	×	×	×	○	×	○	×
Internal system clock (f_{CLK})	×	×	○	×	×	○	×	○	×
Main clock (in PLL mode, f_{XX})	×	○Note	○	×	×	○	○	×	×
Peripheral clock (f_{XX} to f_{XX}/1,024)	×	×	○	×	×	○	×	×	×
WT clock (main)	×	○	○	○	×	○	○	×	×
WT clock (sub)	○	○	○	○	○	○	○	○	○
WDT2 clock (internal oscillation)	×	○	○	○	○	○	○	○	○
WDT2 clock (main)	×	×	○	×	×	○	×	×	×
WDT2 clock (sub)	○	○	○	○	○	○	○	○	○

Note Lockup time

Remark ○: Operable
×: Stopped

6.4.2 Clock output function

The clock output function is used to output the internal system clock (f_{CLK}) from the CLKOUT pin.

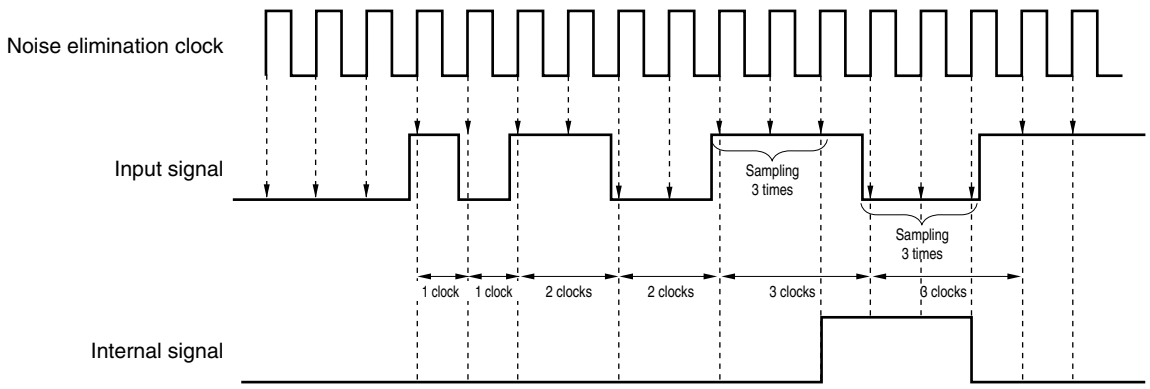
The internal system clock (f_{CLK}) is selected by using the PCC.CK3 to PCC.CK0 bits.

The CLKOUT pin functions alternately as the PCM1 pin and functions as a clock output pin if so specified by the control register of port CM.

The status of the CLKOUT pin is the same as the internal system clock in Table 6-1 and the pin can output the clock when it is in the operable status. It outputs a low level in the stopped status. However, the CLKOUT pin is in the port mode (PCM1 pin: input mode) after reset and until it is set in the output mode. Therefore, the status of the pin is Hi-Z.

A timing example of noise elimination performed by the timer AA input pin digital filter is shown Figure 7-2.

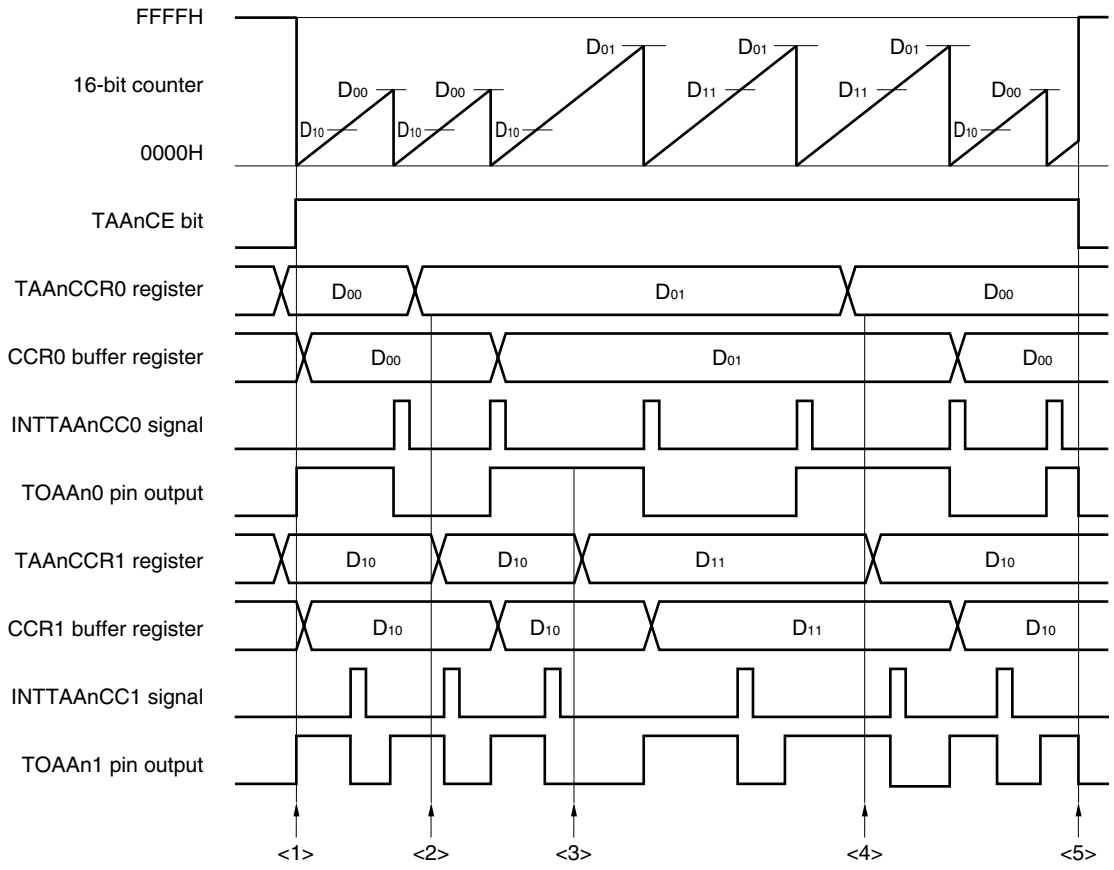
Figure 7-2. Example of Digital Noise Elimination Timing



Remark If there are two or fewer noise elimination clocks while the TIAAn0 or TIAAn1 input signal is high level (or low level), that input signal is eliminated as noise. If it is sampled three times or more, the edge is detected as a valid input (n = 0 to 5).

(1) Operation flow in PWM output mode

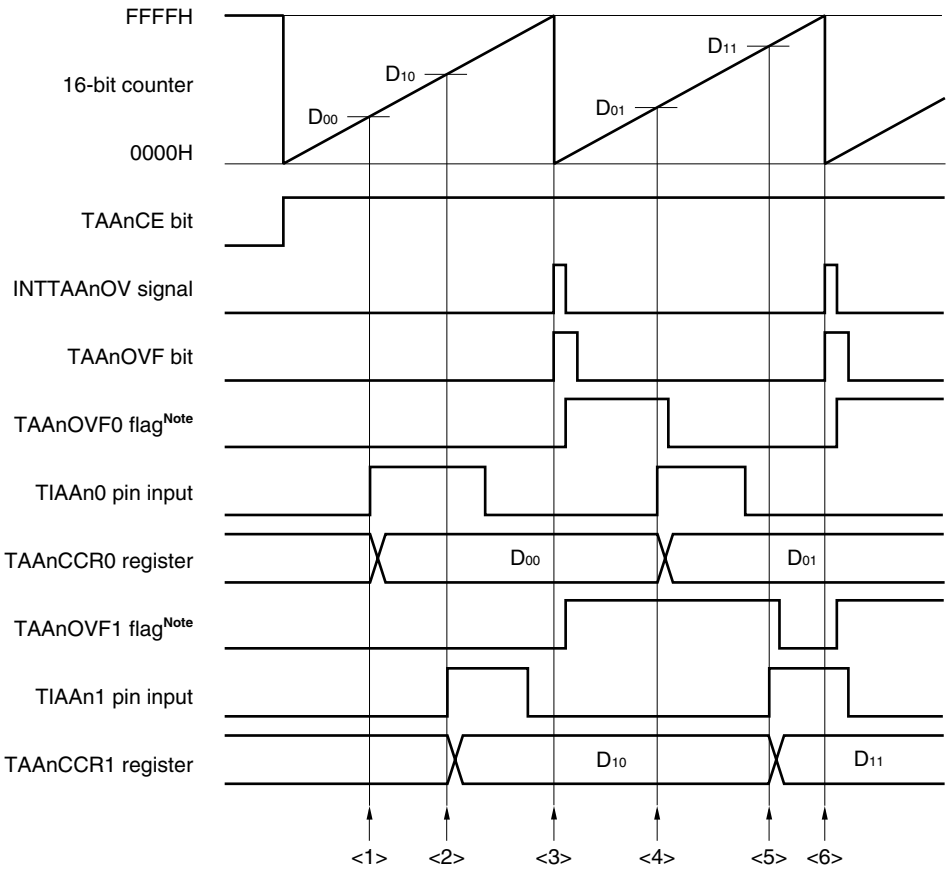
Figure 7-32. Software Processing Flow in PWM Output Mode (1/2)



Remark n = 0 to 5
m = 0, 1

(1/2)

Example when two capture registers are used (using overflow interrupt)



Note The TAAnOVF0 and TAAnOVF1 flags are set on the internal RAM by software.

<1> Read the TAAnCCR0 register (setting of the default value of the TIAAn0 pin input).

<2> Read the TAAnCCR1 register (setting of the default value of the TIAAn1 pin input).

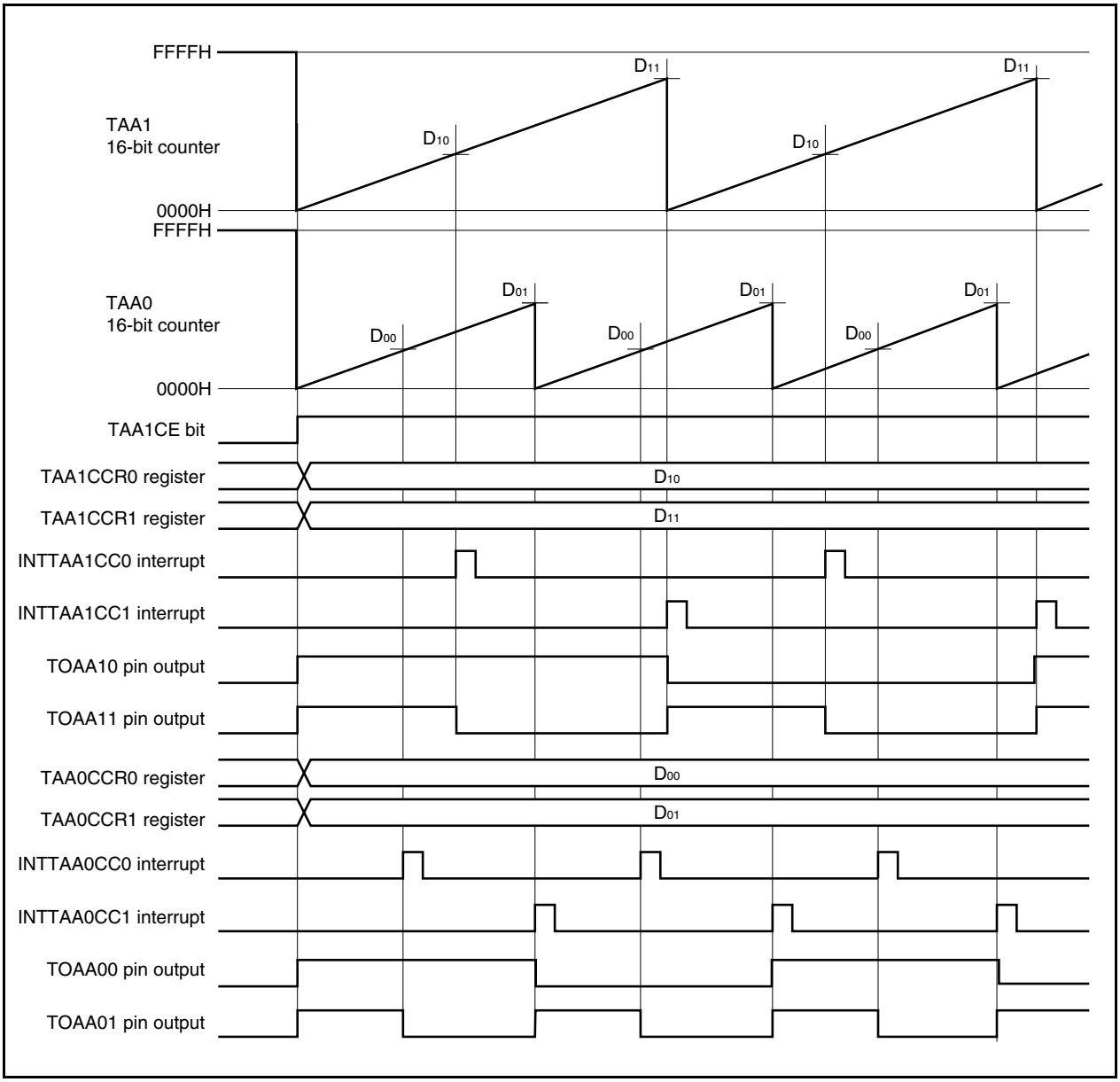
<3> An overflow occurs. Set the TAAnOVF0 and TAAnOVF1 flags to 1 in the overflow interrupt servicing, and clear the overflow flag to 0.

<4> Read the TAAnCCR0 register.
Read the TAAnOVF0 flag. If the TAAnOVF0 flag is 1, clear it to 0.
Because the TAAnOVF0 flag is 1, the pulse width can be calculated by (10000H + D_{01} – D_{00}).

<5> Read the TAAnCCR1 register.
Read the TAAnOVF1 flag. If the TAAnOVF1 flag is 1, clear it to 0 (the TAAnOVF0 flag is cleared in <4>, and the TAAnOVF1 flag remains 1).
Because the TAAnOVF1 flag is 1, the pulse width can be calculated by (10000H + D_{11} – D_{10}) (correct).

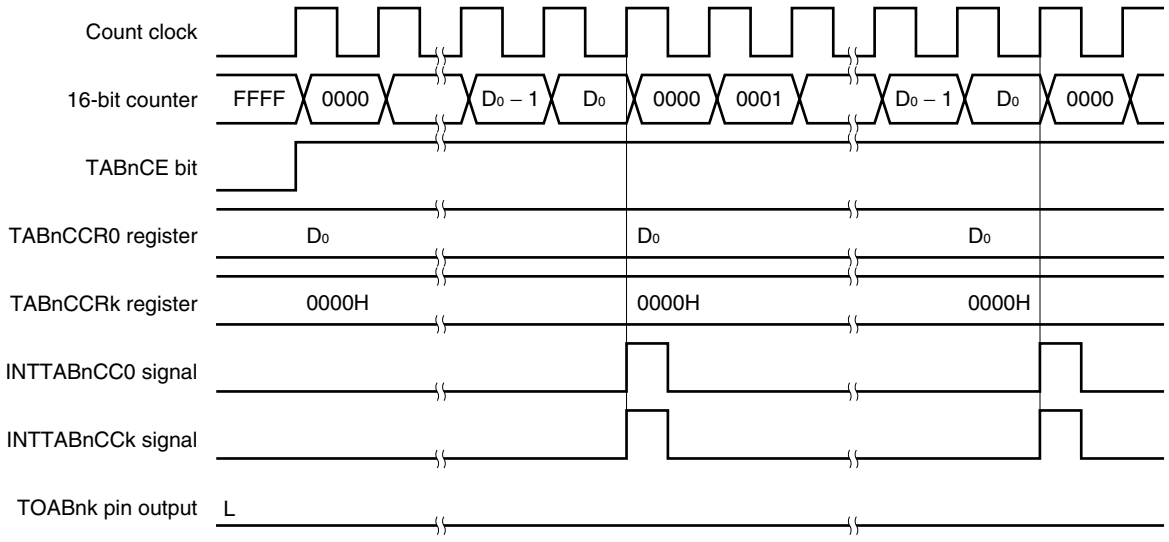
<6> Same as <3>

Figure 7-49. Timing Example of Simultaneous-Start Function (TAA1: Master, TAA0: Slave)



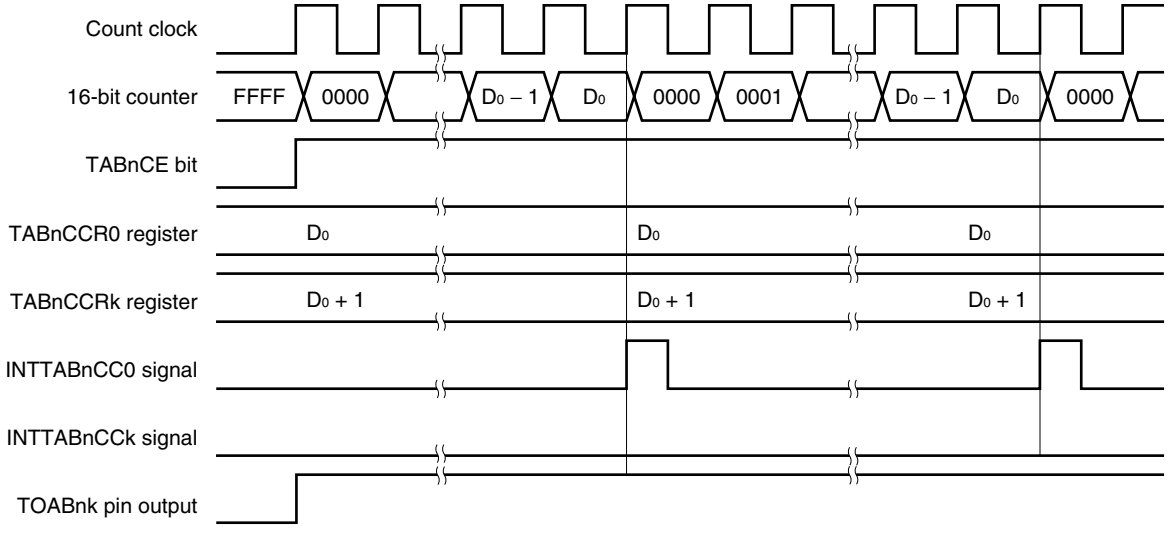
(b) 0%/100% output of PWM waveform

To output a 0% waveform, set the TABnCCRk register to 0000H. If the set value of the TABnCCR0 register is FFFFH, the INTTABnCCk signal is generated periodically.



Remark k = 1 to 3,
n = 0, 1

To output a 100% waveform, set a value of “set value of TABnCCR0 register + 1” to the TABnCCRk register. If the set value of the TABnCCR0 register is FFFFH, 100% output cannot be produced.



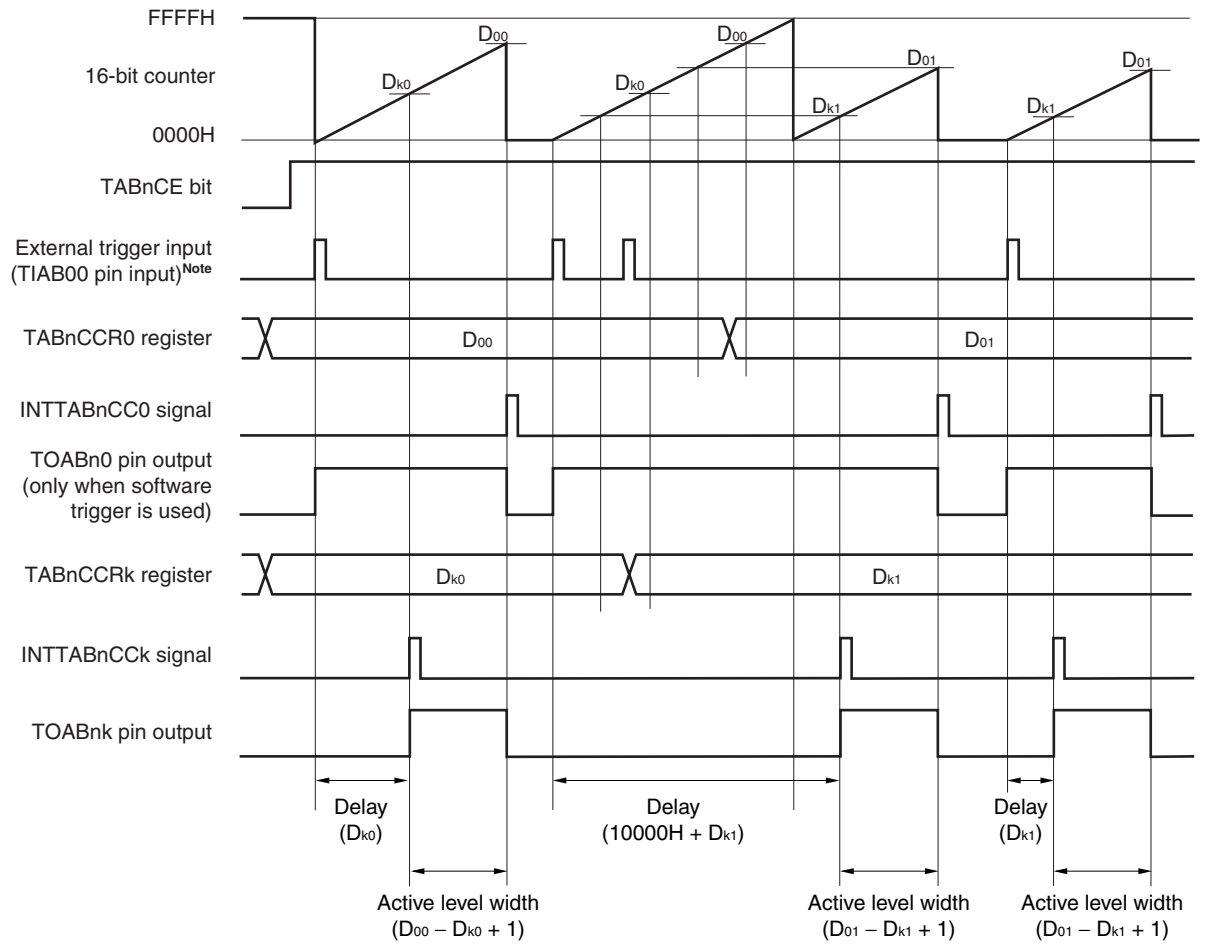
Remark k = 1 to 3,
n = 0, 1

(2) Operation timing in one-shot pulse output mode

(a) Notes on rewriting TABnCCRm register

To change the set value of the TABnCCRm register to a smaller value, stop counting once, and then change the set value.

If the value of the TABnCCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



Note TAB1: TRGAB1 pin

When the TABnCCR0 register is rewritten from D_{00} to D_{01} and the TABnCCRk register from D_{k0} to D_{k1} where $D_{00} > D_{01}$ and $D_{k0} > D_{k1}$, if the TABnCCRk register is rewritten when the count value of the 16-bit counter is greater than D_{k1} and less than D_{k0} and if the TABnCCR0 register is rewritten when the count value is greater than D_{01} and less than D_{00}, each set value is reflected as soon as the register has been rewritten and compared with the count value. The counter counts up to FFFFH and then counts up again from 0000H. When the count value matches D_{k1}, the counter generates the INTTABnCCk signal and asserts the TOABnk pin. When the count value matches D_{01}, the counter generates the INTTABnCC0 signal, deasserts the TOABnk pin, and stops counting.

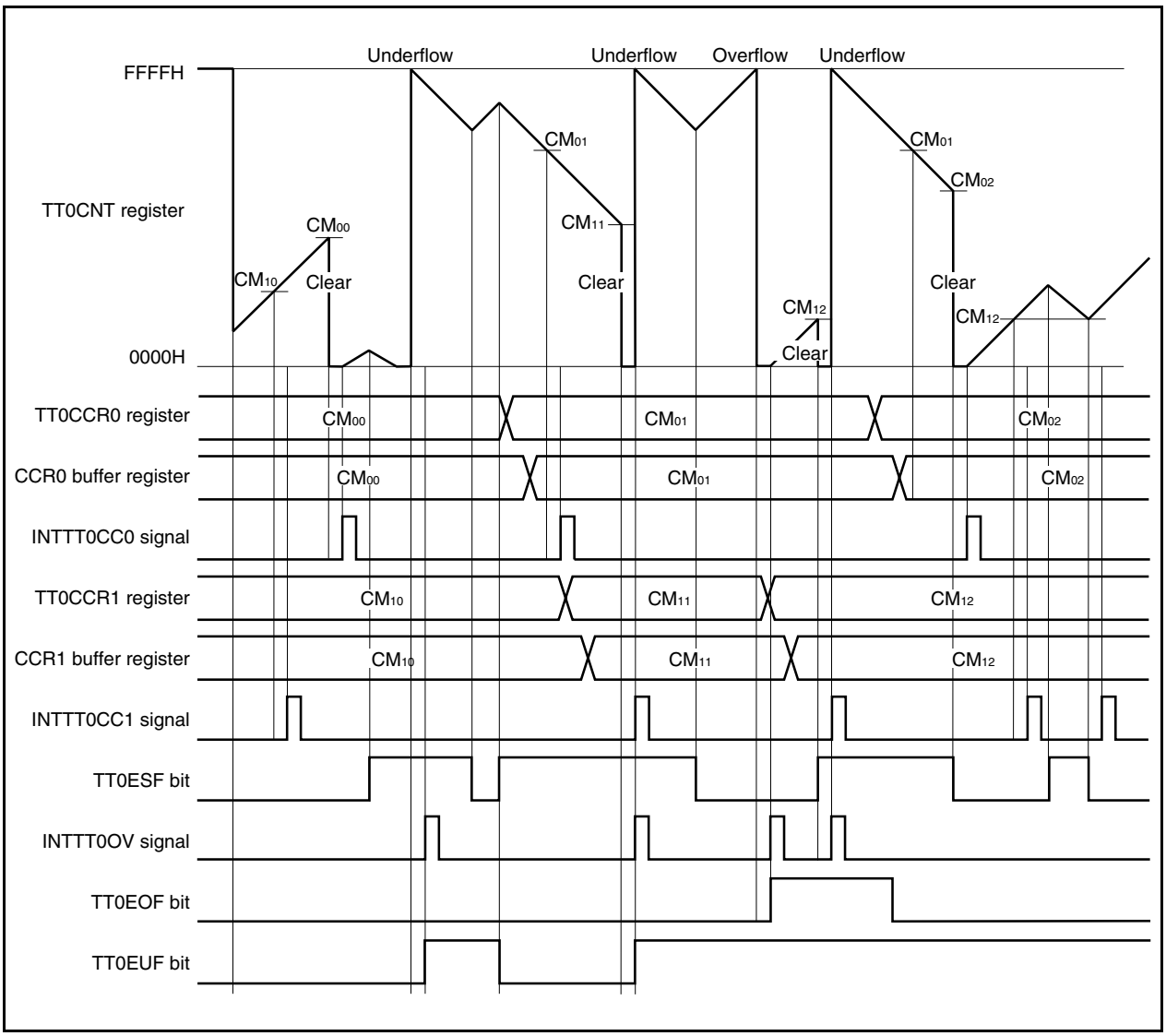
Therefore, the counter may output a pulse with a delay period or active period different from that of the one-shot pulse that is originally expected.

Remark k = 1 to 3,
n = 0, 1

(c) Basic timing 3

[Register setting condition]

- TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits = 11
  The count value of the 16-bit counter is cleared to 0000H when its value matches the value of the CCR0 buffer register.
  The count value of the 16-bit counter is cleared to 0000H when its value matches the value of the CCR1 buffer register.
- Setting of the TT0CTL2.TT0LDE bit is invalid.
- TT0IOC3.TT0SCE bit = 0, and TT0IOC3.TT0ECS1 and TT0IOC3.TT0ECS0 bits = 00
  Specification of clearing the 16-bit counter when the edge of the encoder clear input signal (TECR0 pin) is detected (no edge specified)



(3) Real-time counter control register 2 (RC1CC2)

The RC1CC2 register is an 8-bit register that controls the alarm interrupt function and waiting of counters.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFADFH

	7	6	5	4	3	2	1	0
RC1CC2	WALE	0	0	0	0	0	RWST	RWAIT

WALE	Alarm interrupt (INTRTC1) operation control
0	Does not generate interrupt upon alarm match.
1	Generates interrupt upon alarm match.

RWST	Real-time counter wait state
0	Counter operating
1	Counting up of second to year counters stopped (Reading and writing of counter values enabled)
This is a status flag indicating whether the RWAIT bit setting is valid. Read or write counter values after confirming that the RWST bit is 1.	

RWAIT	Real-time counter wait control
0	Sets counter operation.
1	Stops count operation of second to year counters. (Counter value read/write mode)
This bit controls the operation of the counters. Be sure to write 1 to this bit when reading or writing counter values. If the RC1SUBC register overflows while the RWAIT bit is 1, the overflow information is retained internally and the RC1SEC register is counted up after two clocks or less (2 × 32.768 kHz) after 0 is written to the RWAIT bit. However, if the second counter value is rewritten while the RWAIT bit is 1, the retained overflow information is discarded.	

Cautions 1. See **12.4.5 Changing INTRTC1 interrupt setting during real-time counter operation** when rewriting the WALE bit while the real-time counter operates (RC1PWR bit = 1).

2. Confirm that the RWST bit is set to 1 when reading or writing each counter value.

3. The RWST bit does not become 0 while each counter is being written, even if the RWAIT bit is set to 0. It becomes 0 when writing to each counter is completed.

16.10 Cautions

Cautions concerning UARTBn are shown below.

(1) When supply clock to UARTBn is stopped

When the supply of clocks to UARTBn is stopped (for example, IDLE and STOP modes), operation stops with each register retaining the value it had immediately before the supply of clocks was stopped. The TXDBn pin output also holds and outputs the value it had immediately before the supply of clocks was stopped. However, operation is not guaranteed after the supply of clocks is restarted. Therefore, after the supply of clocks is restarted, the circuits should be initialized by setting the UBnPWR bit = 0, UBnRXE bit = 0, and UBnTXE bit = 0.

(2) Caution on setting UBnCTL0 register

- When using UARTBn, set the external pins related to the UARTBn function to the alternate function and set the UBnCTL2 register. Then set the UBnCTL0.UBnPWR bit to 1 before setting the other bits.
- Be sure to input a high level to the RXDBn pin when setting the external pins related to the UARTBn function to the alternate function. If a low level is input, it is judged that a falling edge is input after the UBnCTL0.UBnRXE bit has been set to 1, and reception may be started.

(3) Caution on setting UBnFIC2 register

Be sure to clear the UBnCTL0.UBnTXE bit (to disable transmission) and UBnCTL0.UBnRXE bit (to disable reception) to 0 before writing data to the UBnFIC2 register. If data is written to the UBnFIC2 register with the UBnTXE or UBnRXE bit set to 1, the operation is not guaranteed.

(4) Transmission interrupt request si**g**nal

In the single mode, the transmission enable interrupt request signal (INTUBnTIT) occurs when the UBnTX register becomes empty (when 1 byte of data is transferred from the UBnTX register to the transmit shift register). In the FIFO mode, the FIFO transmission end interrupt request signal (INTUBnTIF) occurs when data is no longer in transmit FIFO and the transmit shift register (when the FIFO and register are empty). However, the INTUBnTIT signal or INTUBnTIF signal does not occur if the transmit data register becomes empty due to $\overline{\text{RESET}}$ input.

(5) Initialization during continuous transmission in single mode

Confirm that the UBnSTR.UBnTSF bit is 0 before executing initialization during transmission processing. If initialization is executed while the UBnTSF bit is 1, the transmit data is not guaranteed.

(6) Initialization during continuous transmission (pending mode) in FIFO mode

Confirm that the UBnSTR.UBnTSF bit is 0 before executing initialization during transmission processing (this can also be done by checking the FIFO transmission end interrupt request signal (INTUBnTIF)). If initialization is executed while the UBnTSF bit is 1, the transmit data is not guaranteed.

To write transmit data to transmit FIFO by DMA control, set the number of transmit data specified as the trigger by the UBnFIC2.UBnTT3 to UBnFIC2.UBnTT0 bits to 1 byte; otherwise the operation will not be guaranteed.

(7) Initialization during continuous transmission (pointer mode) in FIFO mode

Confirm that the UBnSTR.UBnTSF bit is 0 before executing initialization during transmission processing (this can also be done by checking the FIFO transmission end interrupt request signal (INTUBnTIF)). If initialization is executed while the UBnTSF bit is 1, the transmit data is not guaranteed.

17.3.2 Mode switching between UARTC1, CSIF1 and I²C00

In the V850ES/JH3-E and V850ES/JJ3-E, UARTC1, CSIF1 and I²C00 share the same pin, so these functions cannot be used simultaneously. Set UARTC1 in advance, using the PMC2, PFC2 and PFCE2 registers.

Caution The transmit/receive operation of UARTC1, CSIF1, and I²C00 is not guaranteed if these functions are switched during transmission or reception. Be sure to disable the one that is not used.

Figure 17-3. UARTC1, CSIF1 and I²C00 Mode Switch Settings

After reset: 00H R/W Address: FFFFF444H

	7	6	5	4	3	2	1	0
PMC2	PMC27Note	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20

After reset: 00H R/W Address: FFFFF464H

	7	6	5	4	3	2	1	0
PFC2	PFC27Note	PFC26	PFC25	PFC24	PFC23	PFC22	PFC21	PFC20

After reset: 00H R/W Address: FFFFF704H

	7	6	5	4	3	2	1	0
PFCE2	PFCE27Note	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20

PMC25	PFCE25	PFC25	Operation mode
0	×	×	Port I/O mode
1	0	0	$\overline{\text{SCKF1}}$ (CSIF1)

PMC24	PFCE24	PFC24	Operation mode
0	×	×	Port I/O mode
1	0	0	SOF1 (CSIF1)
1	0	1	RXDC1 (UARTC1)
1	1	0	SCL00 (I²C00)

PMC23	PFCE23	PFC23	Operation mode
0	×	×	Port I/O mode
1	0	0	SIF1 (CSIF1)
1	0	1	TXDC1 (UARTC1)
1	1	0	SDA00 (I²C00)

Note V850ES/JJ3-E only

Remark × = don't care

20.4 Registers

I²C0n is controlled by the following registers.

- IIC control register n (IICCn)
- IIC status register n (IICSn)
- IIC flag register n (IICFn)
- IIC clock select register n (IICCLn)
- IIC function expansion register n (IICXn)
- IIC division clock select register 0 to 2 (OCKS0 to OCKS2)

The following registers are also used.

- IIC shift registers n (IICn)
- Slave address registers n (SVAn)

Remark For the alternate-function pin settings, see **Table 4-18 Settings When Port Pins Are Used for Alternate Functions**.

(1) IIC control registers n (IICCn)

The IICCn registers enable/stop I²C0n operations, set the wait timing, and set other I²C operations.

These registers can be read or written in 8-bit or 1-bit units. However, set the SPIEn, WTIMn, and ACKEn bits when the IICEn bit is 0 or during the wait period. When changing the IICEn bit from “0” to “1”, these bits can also be set at the same time.

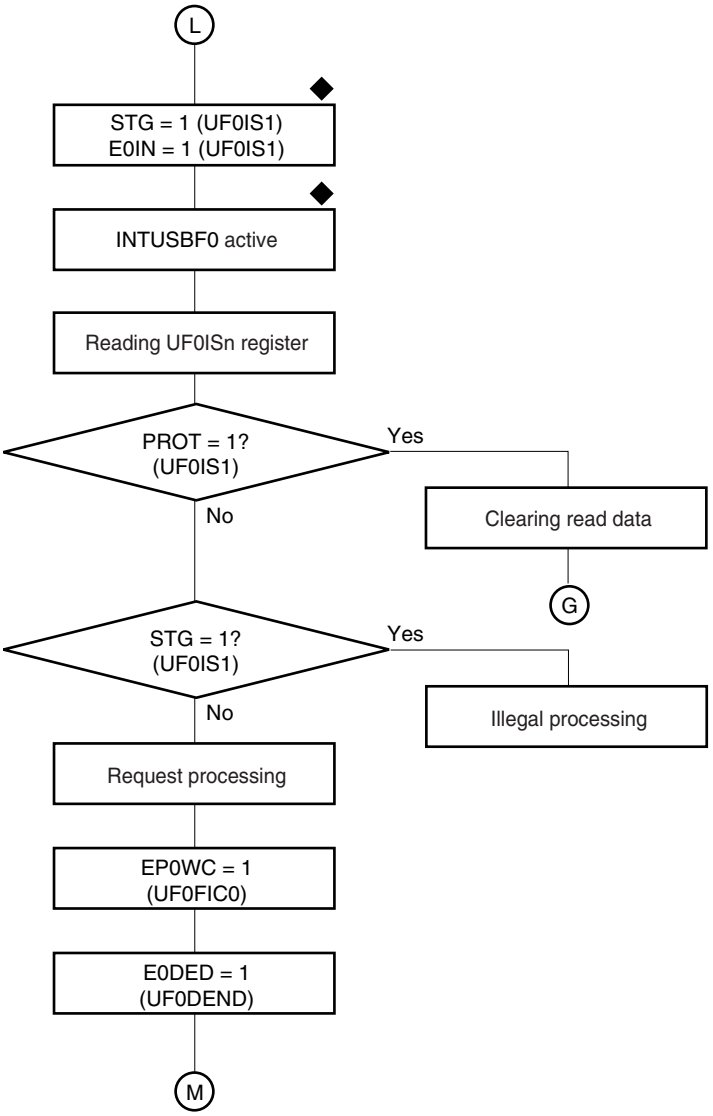
Reset sets these registers to 00H.

(5/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
0020024AH	UF0 configuration/interface/endpoint descriptor register 66	UF0CIE66	R/W		√		Undefined
0020024CH	UF0 configuration/interface/endpoint descriptor register 67	UF0CIE67	R/W		√		Undefined
0020024EH	UF0 configuration/interface/endpoint descriptor register 68	UF0CIE68	R/W		√		Undefined
00200250H	UF0 configuration/interface/endpoint descriptor register 69	UF0CIE69	R/W		√		Undefined
00200252H	UF0 configuration/interface/endpoint descriptor register 70	UF0CIE70	R/W		√		Undefined
00200254H	UF0 configuration/interface/endpoint descriptor register 71	UF0CIE71	R/W		√		Undefined
00200256H	UF0 configuration/interface/endpoint descriptor register 72	UF0CIE72	R/W		√		Undefined
00200258H	UF0 configuration/interface/endpoint descriptor register 73	UF0CIE73	R/W		√		Undefined
0020025AH	UF0 configuration/interface/endpoint descriptor register 74	UF0CIE74	R/W		√		Undefined
0020025CH	UF0 configuration/interface/endpoint descriptor register 75	UF0CIE75	R/W		√		Undefined
0020025EH	UF0 configuration/interface/endpoint descriptor register 76	UF0CIE76	R/W		√		Undefined
00200260H	UF0 configuration/interface/endpoint descriptor register 77	UF0CIE77	R/W		√		Undefined
00200262H	UF0 configuration/interface/endpoint descriptor register 78	UF0CIE78	R/W		√		Undefined
00200264H	UF0 configuration/interface/endpoint descriptor register 79	UF0CIE79	R/W		√		Undefined
00200266H	UF0 configuration/interface/endpoint descriptor register 80	UF0CIE80	R/W		√		Undefined
00200268H	UF0 configuration/interface/endpoint descriptor register 81	UF0CIE81	R/W		√		Undefined
0020026AH	UF0 configuration/interface/endpoint descriptor register 82	UF0CIE82	R/W		√		Undefined
0020026CH	UF0 configuration/interface/endpoint descriptor register 83	UF0CIE83	R/W		√		Undefined
0020026EH	UF0 configuration/interface/endpoint descriptor register 84	UF0CIE84	R/W		√		Undefined
00200270H	UF0 configuration/interface/endpoint descriptor register 85	UF0CIE85	R/W		√		Undefined
00200272H	UF0 configuration/interface/endpoint descriptor register 86	UF0CIE86	R/W		√		Undefined
00200274H	UF0 configuration/interface/endpoint descriptor register 87	UF0CIE87	R/W		√		Undefined

Figure 22-24. CPUDEC Request for Control Transfer (9/12)

(c) Control transfer (write) (3/4)

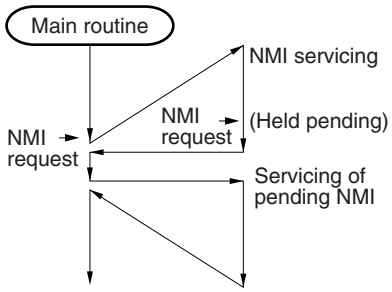
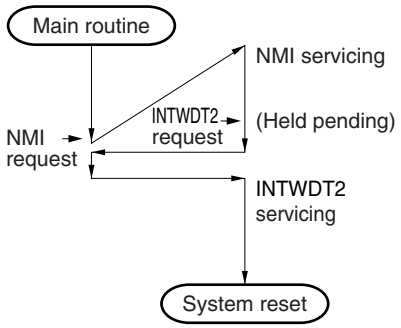
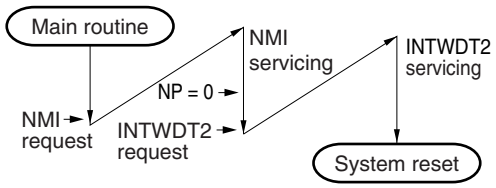
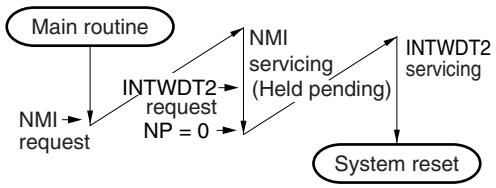
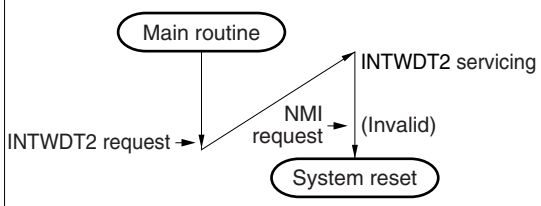
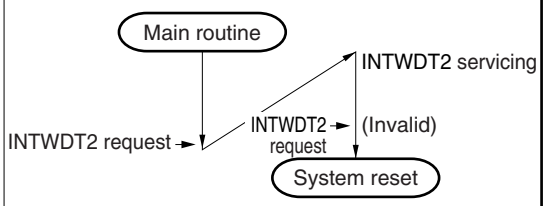


Remarks 1. n = 0, 1

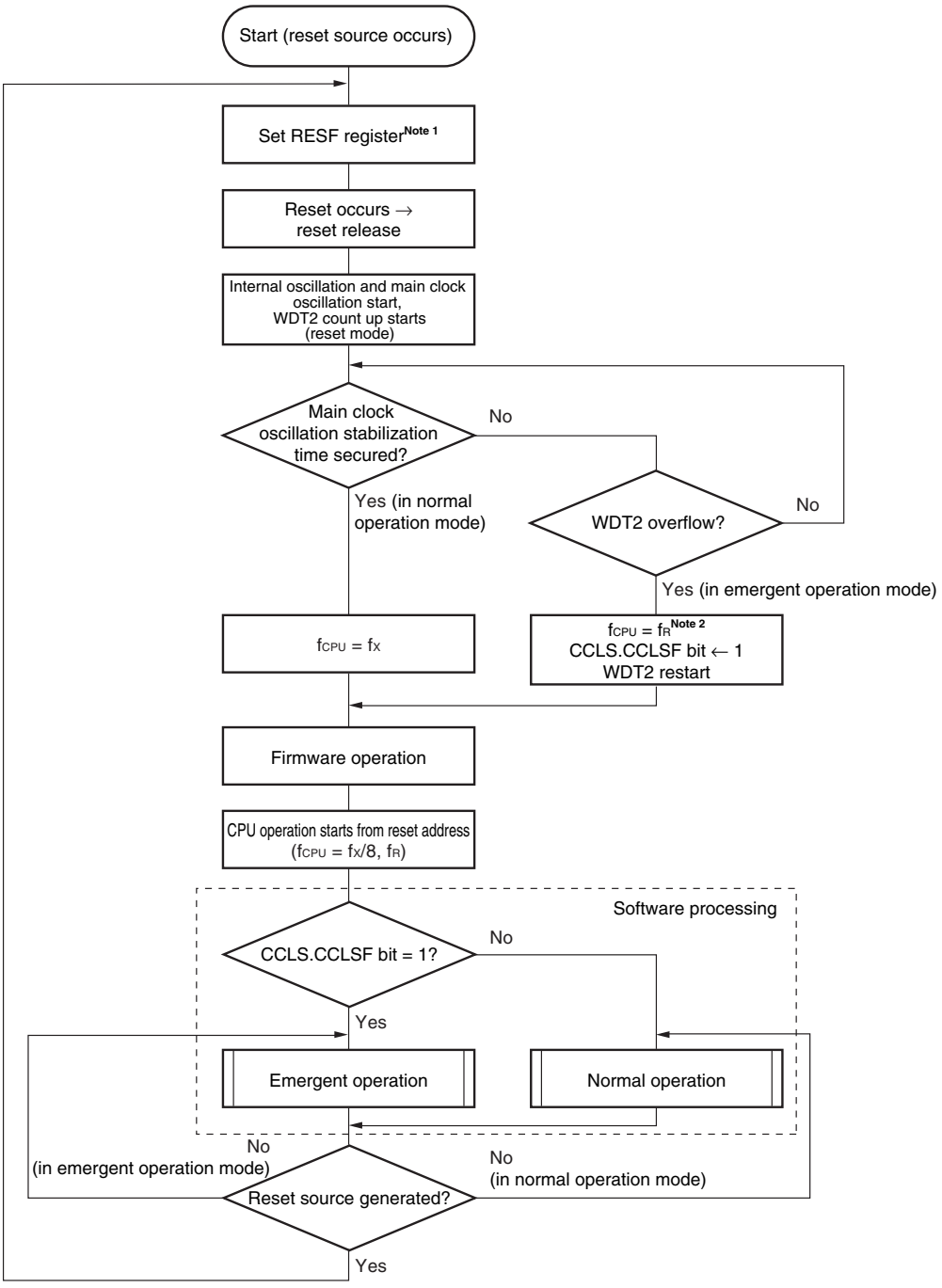
2. ♦: Processing by hardware

Figure 25-1. Non-Maskable Interrupt Request Signal Acknowledgment Operation (2/2)

(b) Non-maskable interrupt request signal generated during non-maskable interrupt servicing

Non-maskable interrupt being serviced	Non-maskable interrupt request signal generated during non-maskable interrupt servicing	
	NMI	INTWDT2
NMI	• NMI request generated during NMI servicing 	• INTWDT2 request generated during NMI servicing (NP bit = 1 retained before INTWDT2 request)  • INTWDT2 request generated during NMI servicing (NP bit = 0 set before INTWDT2 request)  • INTWDT2 request generated during NMI servicing (NP = 0 set after INTWDT2 request) 
INTWDT2	• NMI request generated during INTWDT2 servicing 	• INTWDT2 request generated during INTWDT2 servicing 

28.3.6 Reset function operation flow



Notes 1. Bit to be set differs depending on the reset source.

Reset Source	WDT2RF Bit	CRMRF Bit	LVIRF Bit
$\overline{\text{RESET}}$ pin	0	0	0
WDT2	1	Value before reset is retained.	Value before reset is retained.
CLM	Value before reset is retained.	1	Value before reset is retained.
LVI	Value before reset is retained.	Value before reset is retained.	1

2. The internal oscillator cannot be stopped.