Renesas Electronics America Inc - UPD70F3786GJ-GAE-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, EBI/EMI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	100
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	124K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3786gj-gae-ax

(2/3)

Pin Name	I/O	Function	Alternate Function	Pin No.	
				JH3-E	JJ3-E
P50	I/O	Port 5 5-bit I/O port (V850ES/JH3-E) 10-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units. 5 V tolerant.	INTP07/DDI	23	23
P51			INTP08/DDO	24	24
P52			INTP09/DCK	25	25
P53			INTP10/DMS	26	26
P54			INTP11/$\overline{\text{DRST}}$	27	27
P55			SDA04/INTP23/$\overline{\text{UDMARQ1}}$	–	42
P56			SCL04/INTP24/$\overline{\text{UDMAAK1}}$	–	43
P57			SIF6/TXDC7	–	62
P58			SOF6/RXDC7	–	63
P59			$\overline{\text{SCKF6}}$/INTP25	–	64
P70	I/O	Port 7 10-bit I/O port (V850ES/JH3-E) 12-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	ANI0	128	144
P71			ANI1	127	143
P72			ANI2	126	142
P73			ANI3	125	141
P74			ANI4	124	140
P75			ANI5	123	139
P76			ANI6	122	138
P77			ANI7	121	137
P78			ANI8	120	136
P79			ANI9	119	135
P710			ANI10	–	134
P711			ANI11	–	133
P90	I/O	Port 9 16-bit I/O port Input/output can be specified in 1-bit units. 5 V tolerant.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12/A0	65	71
P91			TOAB1B1/TIAB10/KR1/TOAB10/A1	66	72
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13/A2	67	73
P93			TOAB1B2/TRGAB1/KR3/INTP14/A3	68	74
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15/A4	69	75
P95			TOAB1B3/EVTB1/KR5/INTP16/A5	70	76
P96			TECR0/TIT00/KR6/TOT00/A6	71	77
P97			TENC00/TIT01/KR7/TOT01/A7	72	78
P98			TENC01/INTP17/A8	73	79
P99			SIE1/TXDC5/SDA03/A9	74	80
P910			SOE1/RXDC5/SCL03/A10	75	81
P911			$\overline{\text{SCKE1}}$/TIAA50/TOAA50/A11	76	82
P912			TOAB1OFF/INTP18/A12	77	83
P913			SIF3/TXDB1/INTP19/A13	78	84
P914			SOF3/RXDB1/INTP20/A14	79	85
P915			$\overline{\text{SCKF3}}$/TIAA51/TOAA51/A15	80	86

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

(2) Clock control register (CKC)

The CKC register is a special register. Data can be written to this register only in a combination of specific sequence (see **3.4.8 Special registers**).

The CKC register controls the internal system clock in the PLL mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 0AH.

After reset: 0AH R/W Address: FFFFF822H

	7	6	5	4	3	2	1	0
CKC	0	0	0	0	1	0	1	CKDIV0

CKDIV0	Internal system clock (f_{XX}) in PLL mode
0	Setting prohibited
1	$f_{XX} = 8 \times f_X$ (f_X = 3.0 to 6.25 MHz)

Caution 1. Be sure to set the CKC register to 0BH. When setting this register to a value other than 0BH or leaving it set to its initial value without setting it to 0BH, enabling PLL operation (PLLCTL.SELPLL = 1) is prohibited.

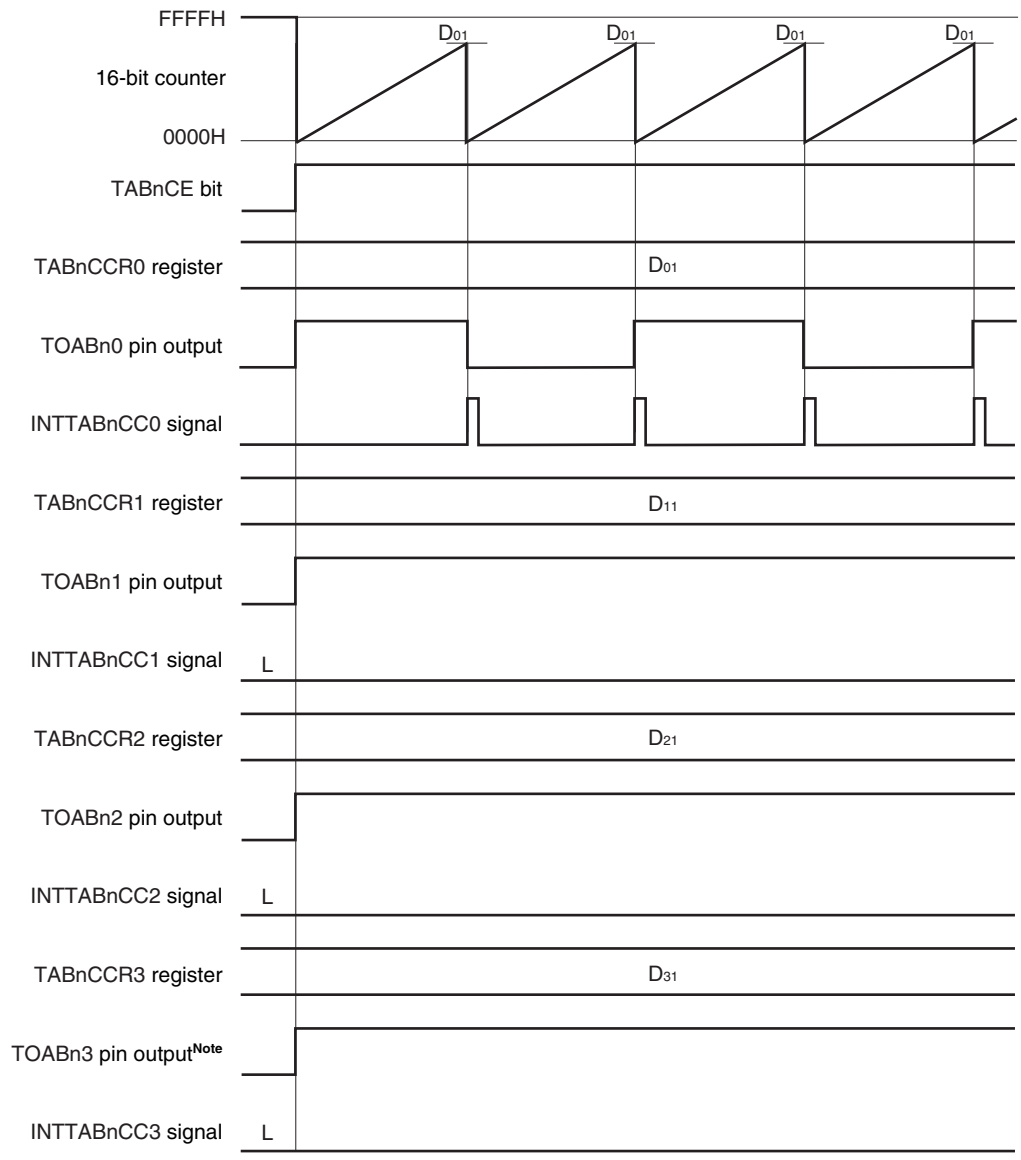
2. Be sure to set bits 3 and 1 to "1" and clear bits 7 to 4 and 2 to "0".

Remark Both the CPU clock and peripheral clock are divided by the CKC register, but only the CPU clock is divided by the PCC register.

If the set value of the TABnCCRk register is greater than the set value of the TABnCCR0 register, the count value of the 16-bit counter does not match the value of the TABnCCRk register. Consequently, the INTTABnCCk signal is not generated, nor is the output of the TOABnk pin changed.

Remark k = 1 to 3,
n = 0, 1

Figure 8-8. Timing Chart When $D_{01} < D_{k1}$

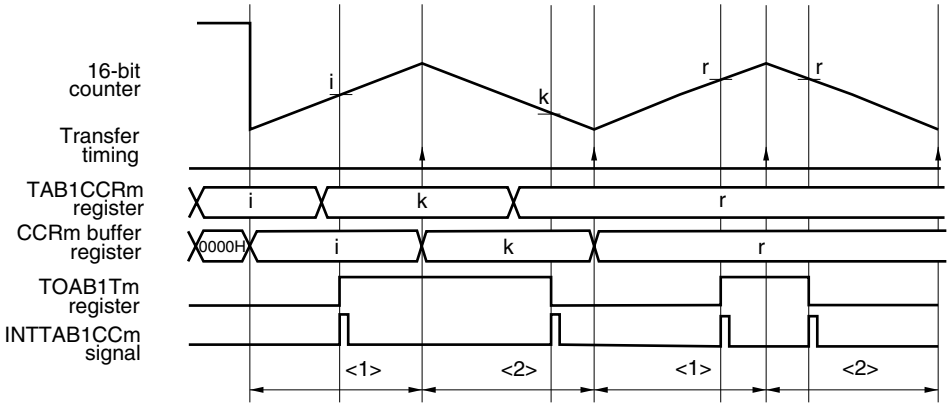


Note The V850ES/JH3-E only includes the TOAB13 pin; it is not provided with the TOAB03 pin.

Remark n = 0, 1

(c) Rewriting TAB1CCRm register

Figure 11-30. Example of Rewriting TAB1CCRm Register



Rewriting during period <1> (rewriting during counting up)

Because the TAB1CCRm register value is transferred at the transfer timing of the crest (match between the 16-bit counter value and TAB1CCRm register value), an asymmetrical triangular wave is output.

Rewriting during period <2> (rewriting during counting down)

Because the TAB1CCRm register value is transferred at the transfer timing of the valley (match between the 16-bit counter value and 0001H), a symmetrical triangular wave is output.

Remark m = 1 to 3

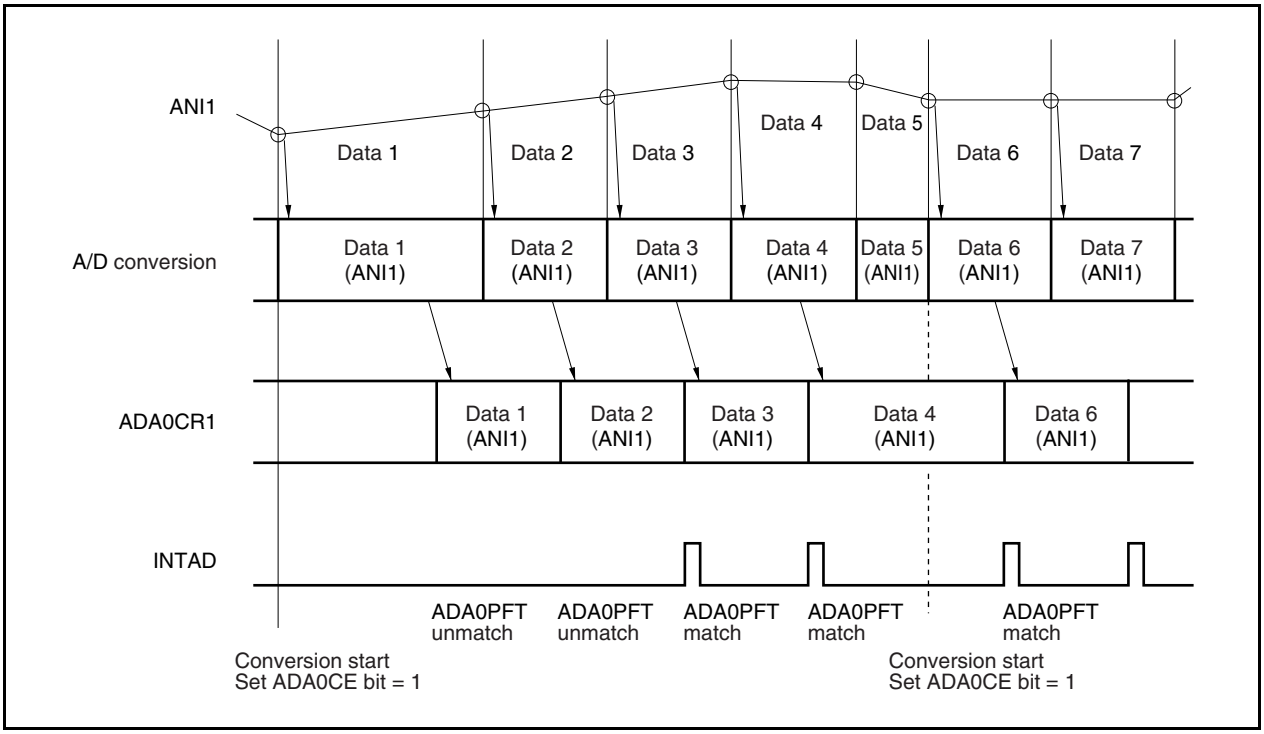
(d) Transferring TAB1OPT1 register value

Do not set the TAB1OPT1.TAB1ID4 to TAB1OPT1.TAB1ID0 bits to other than 00000. When using the interrupt culling function, rewrite the TAB1OPT1 register in the intermittent batch rewrite mode (transfer culling mode). For details of rewriting the TAB1OPT1 register, see **11.4.3 Interrupt culling function**.

(1) Continuous select mode

In this mode, the result of converting the voltage of the analog input pin specified by the ADA0S register is compared with the set value of the ADA0PFT register. If the result of power-fail comparison matches the condition set by the ADA0PFC bit, the conversion result is stored in the ADA0CRn register, and the INTAD signal is generated. If it does not match, the conversion result is stored in the ADA0CRn register, and the INTAD signal is not generated. After completion of the first conversion, the next conversion is started, unless the ADA0M0.ADA0CE bit is cleared to 0.

Figure 15-8. Timing Example of Continuous Select Mode Operation (When Power-Fail Comparison Is Made: ADA0S Register = 01H)



(2) Continuous scan mode

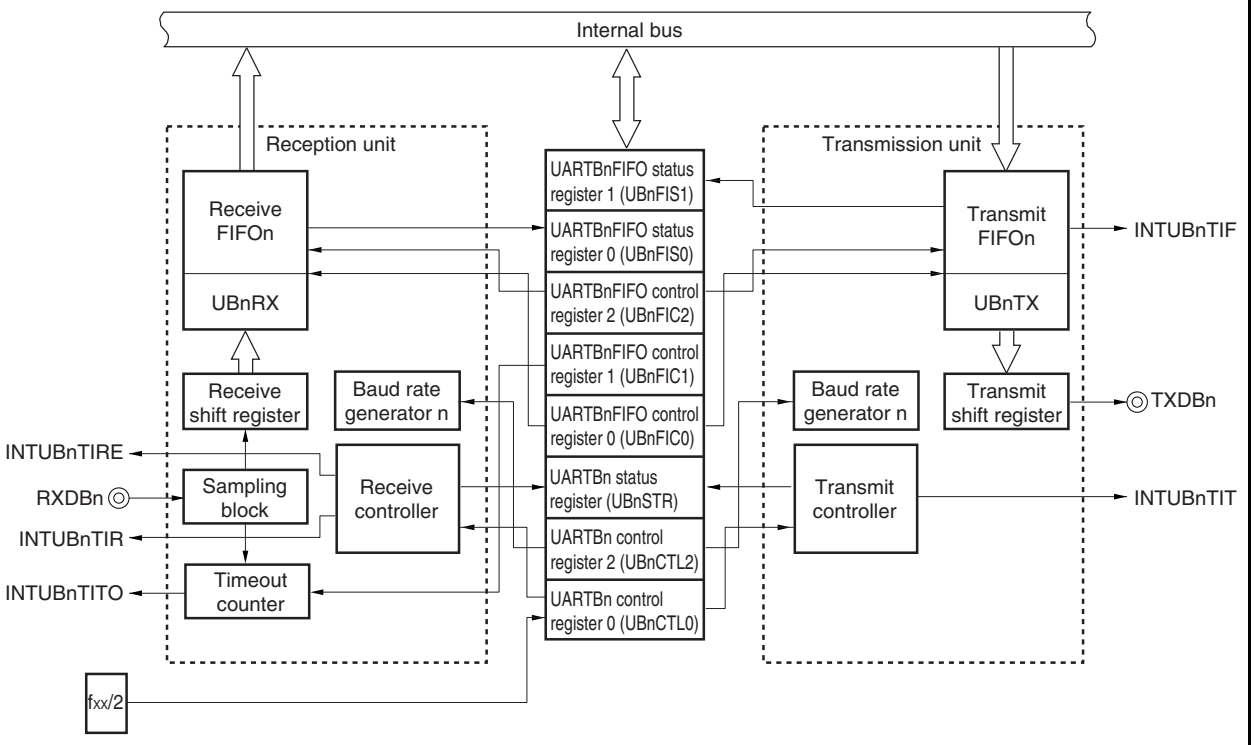
In this mode, the results of converting the voltages of the analog input pins sequentially selected from the ANI0 pin to the pin specified by the ADA0S register are stored, and the set value of the ADA0CR0H register of channel 0 is compared with the value of the ADA0PFT register. If the result of power-fail comparison matches the condition set by the ADA0PFC bit, the conversion result is stored in the ADA0CR0 register, and the INTAD signal is generated. If it does not match, the conversion result is stored in the ADA0CR0 register, and the INTAD signal is not generated.

After the result of the first conversion has been stored in the ADA0CR0 register, the results of sequentially converting the voltages on the analog input pins up to the pin specified by the ADA0S register are continuously stored. After completion of conversion, the next conversion is started from the ANI0 pin again, unless the ADA0CE bit is cleared to 0.

16.2 Configuration

The block diagram of the UARTBn is shown below.

Figure 16-1. Block Diagram of UARTBn



Remark **1.** fxx: Main clock frequency

2. For the configuration of the baud rate generator, see **Figure 16-10**.

3. n = 0, 1

UARTBn consists of the following hardware units.

Table 16-1. Configuration of UARTBn

Item	Configuration
Registers	UARTBn control register 0 (UBnCTL0) UARTBn control register 2 (UBnCTL2) UARTBn status register (UBnSTR) UARTBn FIFO control register 0 (UBnFIC0) UARTBn FIFO control register 1 (UBnFIC1) UARTBn FIFO control register 2 (UBnFIC2) UARTBn FIFO status register 0 (UBnFIS0) UARTBn FIFO status register 1 (UBnFIS1) Receive shift register UARTBn receive data register AP (UBnRXAP) UARTBn receive data register (UBnRX) Transmit shift register UARTBn transmit data register (UBnTX)

(7) UARTBn FIFO control register 1 (UBnFIC1)

The UBnFIC1 register is valid in the FIFO mode (UBnFIC0.UBnMOD bit = 1). It generates a reception timeout interrupt request signal (INTUBnTITO) if data is stored in receive FIFO when the next data does not come (start bit is not detected) after the lapse of the time set by the UBnTC4 to UBnTC0 bits (next data reception wait time), after the stop bit has been received.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: UB0FIC1 FFFFFB8BH, UB1FIC1 FFFFFBABH

	7	6	5	4	3	2	1	0
UBnFIC1 (n = 0, 1)	UBnTCE	0	0	UBnTC4	UBnTC3	UBnTC2	UBnTC1	UBnTC0

UBnTCE	Specification of timeout counter function disable/enable
0	Disable use of timeout counter function.
1	Enable use of timeout counter function.

UBnTC4	UBnTC3	UBnTC2	UBnTC1	UBnTC0	Next data reception wait time
0	0	0	0	0	32 bytes (32 × 8/baud rate)
0	0	0	0	1	31 bytes (31 × 8/baud rate)
0	0	0	1	0	30 bytes (30 × 8/baud rate)
0	0	0	1	1	29 bytes (29 × 8/baud rate)
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
1	1	1	0	0	4 bytes (4 × 8/baud rate)
1	1	1	0	1	3 bytes (3 × 8/baud rate)
1	1	1	1	0	2 bytes (2 × 8/baud rate)
1	1	1	1	1	1 byte (1 × 8/baud rate)

When counting up of the reception wait time, set by the UBnTC4 to UBnTC0 bits, is complete, the count value of the timeout counter is cleared to 0, regardless of the status of the data stored in receive FIFO. When the next start bit is later detected, counting is started again from the stop bit of that data.

(2) Function of CSI data buffer registers 0, 1 (CSIBUF0, CSIBUF1)

By consecutively writing the transmit data to the CEnTX0 register from where it is transferred, up to sixteen 16-bit data can be stored in the CSIBUFn register while the CSIBUFn pointer for writing is automatically incremented (n = 0, 1).

The condition under which transfer is to be started (CEnSTR.CEnEMF bit = 0) is satisfied when data is written to the lower 8 bits (CEnTX0L register) of the CEnTX0 register. If a transfer data length of 9 bits or more is specified (CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 bits = 0000 or 1001 to 1111), data must be written to the CEnTX0 register in 16-bit units or to the CEnTX0H and CEnTX0L registers, in that order, in 8-bit units. If the transfer data length is set to 8 bits (CEnCTL2.CEnDLS3 to CEnCTL2.CEnDLS0 bits = 1000), data must be written to the CEnTX0L register in 8-bit units or to the CEnTX0 register in 16-bit units. (If data is written to the CEnTX0L register in 16-bit units, however, the higher 8 bits of the data (of the CEnTX0H register) are ignored and not transferred).

The CEnSTR.CEnFLF register is set to 1 when 16 data exist in the CSIBUFn register and outputs a CSIBUFn overflow interrupt (INTCEnTIOF) when the CEnFLF bit = 1 and when the 17th transfer data is written (17th transfer data is not written and ignored).

Sixteen data exist in the CSIBUFn register in the single mode (CEnCTL0.CEnTMS bit = 1) when “CSIBUFn pointer value for writing = CSIBUFn pointer value for SIOn loading, and CEnSTR.CEnFLF bit = 1”. When the CSIBUFn pointer for SIOn loading is incremented after completion of transfer while CEnFLF bit = 1, the CEnFLF bit is cleared to 0 and the next transmission data can be written.

In the continuous mode (CEnCTL0.CEnTMS bit = 1), when one data has been transferred, the CEnFLF bit is cleared to 0, but writing the next transmission data is prohibited (if a receive operation is processed, the received data is stored in the CSIBUFn register. Therefore, if the transmission data is written to the register, the received data is overwritten and destroyed).

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 01H.

(1/3)

After reset: 01H R/W Address: CF0CTL0 FFFFFD00H, CF1CTL0 FFFFFD10H, CF2CTL0 FFFFFD20H, CF3CTL0 FFFFFD30H, CF4CTL0 FFFFFD40H, CF5CTL0 FFFFFD50H, CF6CTL0 FFFFFD60H

	<7>	<6>	<5>	<4>	3	2	1	<0>
CFnCTL0	CFnPWR	CFnTXE[Note]	CFnRXE[Note]	CFnDIR[Note]	0	0	CFnTMS[Note]	CFnSCE

CFnPWR	Specification of CSIFn operation disable/enable
0	Disables CSIFn operation and resets the CFnSTR register
1	Enables CSIFn operation
• The CFnPWR bit controls the CSIFn operation and resets the internal circuit.	

CFnTXE[Note]	Specification of transmit operation disable/enable
0	Disables transmit operation
1	Enables transmit operation
• The SOFn output is low level when the CFnTXE bit is 0.	

CFnRXE[Note]	Specification of receive operation disable/enable
0	Disables receive operation
1	Enables receive operation
• No reception completion interrupt is output even when the prescribed data is transferred, and the receive data (CFnRX register) is not updated, because the receive operation is disabled by clearing the CFnRXE bit to 0.	

Note These bits can only be rewritten when the CFnPWR bit = 0. However, CFnPWR bit = 1 can also be set at the same time as rewriting these bits.

Caution To forcibly suspend transmission/reception, clear the CFnPWR bit to 0 instead of the CFnRXE and CFnTXE bits. At this time, the clock output is stopped.

Remark n = 0 to 4 (V850ES/JH3-E)
n = 0 to 6 (V850ES/JJ3-E)

(4) CSIFn control register 1 (CFnCTL1)

CFnCTL1 is an 8-bit register that controls the CSIFn serial transfer operation.

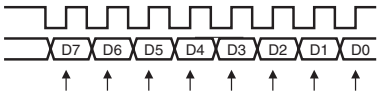
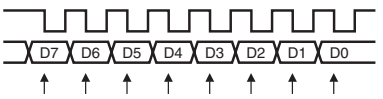
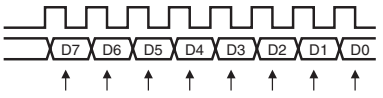
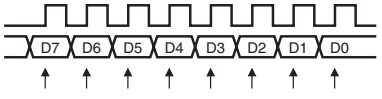
This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Caution The CFnCTL1 register can be rewritten only when the CFnCTL0.CFnPWR bit = 0.

After reset: 00H R/W Address: CF0CTL1 FFFFFD01H, CF1CTL1 FFFFFD11H, CF2CTL1 FFFFFD21H, CF3CTL1 FFFFFD31H, CF4CTL1 FFFFFD41H, CF5CTL1 FFFFFD51H, CF6CTL1 FFFFFD61H

	7	6	5	4	3	2	1	0
CFnCTL1	0	0	0	CFnCKP	CFnDAP	CFnCKS2	CFnCKS1	CFnCKS0

	CFnCKP	CFnDAP	Specification of data transmission/ reception timing in relation to $\overline{SCKFn}$
Communication type 1	0	0	
Communication type 2	0	1	
Communication type 3	1	0	
Communication type 4	1	1	

CFnCKS2	CFnCKS1	CFnCKS0	Communication clock (f_{CCLK})[Note]	Mode
0	0	0	$f_{XX}/4$	Master mode
0	0	1	$f_{XX}/6$	Master mode
0	1	0	$f_{XX}/8$	Master mode
0	1	1	$f_{XX}/12$	Master mode
1	0	0	$f_{XX}/16$	Master mode
1	0	1	$f_{XX}/32$	Master mode
1	1	0	f_{BRGm}	Master mode
1	1	1	External clock ($\overline{SCKFn}$)	Slave mode

Notes 1. If n is 0, 4, or 5, set the communication clock (f_{CCLK}) to 8 MHz or lower.

2. If n is 1 to 3, or 6, set the communication clock (f_{CCLK}) to 5 MHz or lower.

Remarks 1. n = 0 to 4 (V850ES/JH3-E)
n = 0 to 6 (V850ES/JJ3-E)

2. When n = 0 or 1, m = 1
When n = 2 or 3, m = 2
When n = 4, m = 3
When n = 5 or 6, m = 4
For details of f_{BRGm}, see **19.8 Baud Rate Generator**.

(5) IIC function expansion registers n (IICXn)

The IICXn registers set I²C0n function expansion (valid only in the high-speed mode).

These registers can be read or written in 8-bit or 1-bit units.

Setting of the CLXn bit is performed in combination with the SMCn, CLn1, and CLn0 bits of the IICCLn register and the OCKSTHm, OCKSm1, and OCKSm0 bits of the OCKSm register (see **20.4 (6) I²C0n transfer clock setting method**) (m = 0 to 2).

Set the IICXn registers when the IICCn.IICEn bit = 0.

Reset sets these registers to 00H.

After reset: 00H R/W Address: IICX0 FFFFFD85H, IICX1 FFFFFD95H, IICX2 FFFFFDA5H, IICX3 FFFFFDB5H, IICX4 FFFFFBC5H

	7	6	5	4	3	2	1	<0>
IICXn	0	0	0	0	0	0	0	CLXn

Remark n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

(6) I²C0n transfer clock setting method

The I²C0n transfer clock frequency (f_{SCL}) is calculated using the following expression.

$$f_{SCL} = 1/(m \times T + t_R + t_F)$$

m = 72, 88, 96, 108, 120, 144, 192, 240, 264, 344, 352, 396, 440, 516, 688, 860 (see **Table 20-2 Clock Settings**).

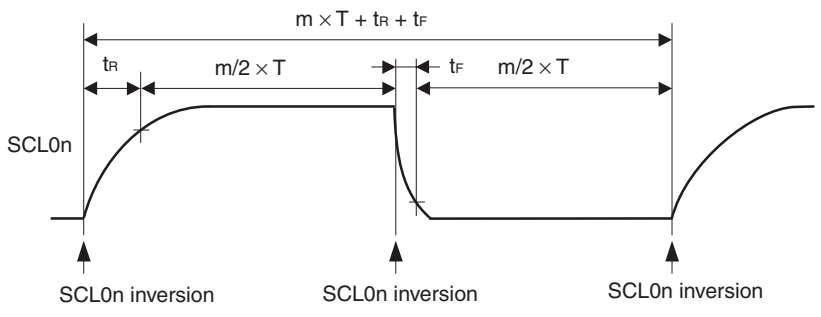
T: $1/f_{XX}$

t_R: SCL0n pin rise time

t_F: SCL0n pin fall time

For example, the I²C0n transfer clock frequency (f_{SCL}) when f_{XX} = 24 MHz, m = 264, t_R = 200 ns, and t_F = 50 ns is calculated using following expression.

$$f_{SCL} = 1/(264 \times 41.7 \text{ ns} + 200 \text{ ns} + 50 \text{ ns}) \cong 88.9 \text{ kHz}$$



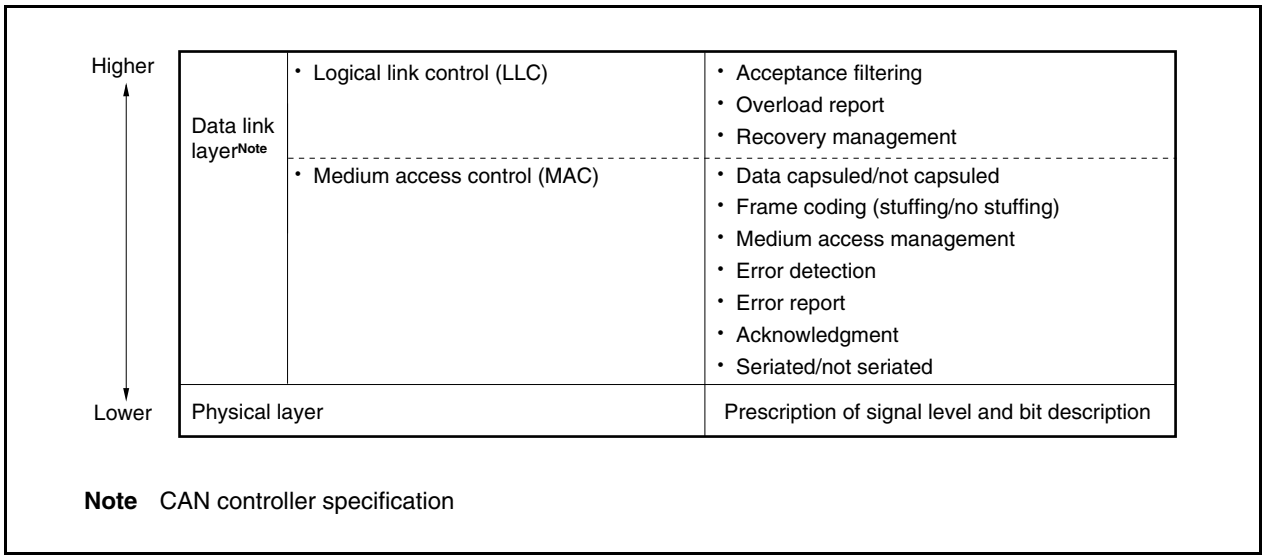
The clock to be selected can be set by combining of the SMCn, CLn1, and CLn0 bits of the IICCLn register, the CLXn bit of the IICXn register, and the OCKSTHm, OCKSm1, and OCKSm0 bits of the OCKSm register (m = 0 to 2).

21.2 CAN Protocol

CAN (Controller Area Network) is a high-speed multiplex communication protocol for real-time communication in automotive applications (class C). CAN is prescribed by ISO 11898. For details, refer to the ISO 11898 specifications.

The CAN specification is generally divided into two layers: a physical layer and a data link layer. In turn, the data link layer includes logical link and medium access control. The composition of these layers is illustrated below.

Figure 21-2. Composition of Layers



Note CAN controller specification

21.2.1 Frame format

(1) Standard format frame

- The standard format frame uses 11-bit identifiers, which means that it can handle up to 2,048 messages.

(2) Extended format frame

- The extended format frame uses 29-bit (11 bits + 18 bits) identifiers, which increases the number of messages that can be handled to $2{,}048 \times 2^{18}$ messages.
- An extended format frame is set when “recessive level” (CMOS level of “1”) is set for both the SRR and IDE bits in the arbitration field.

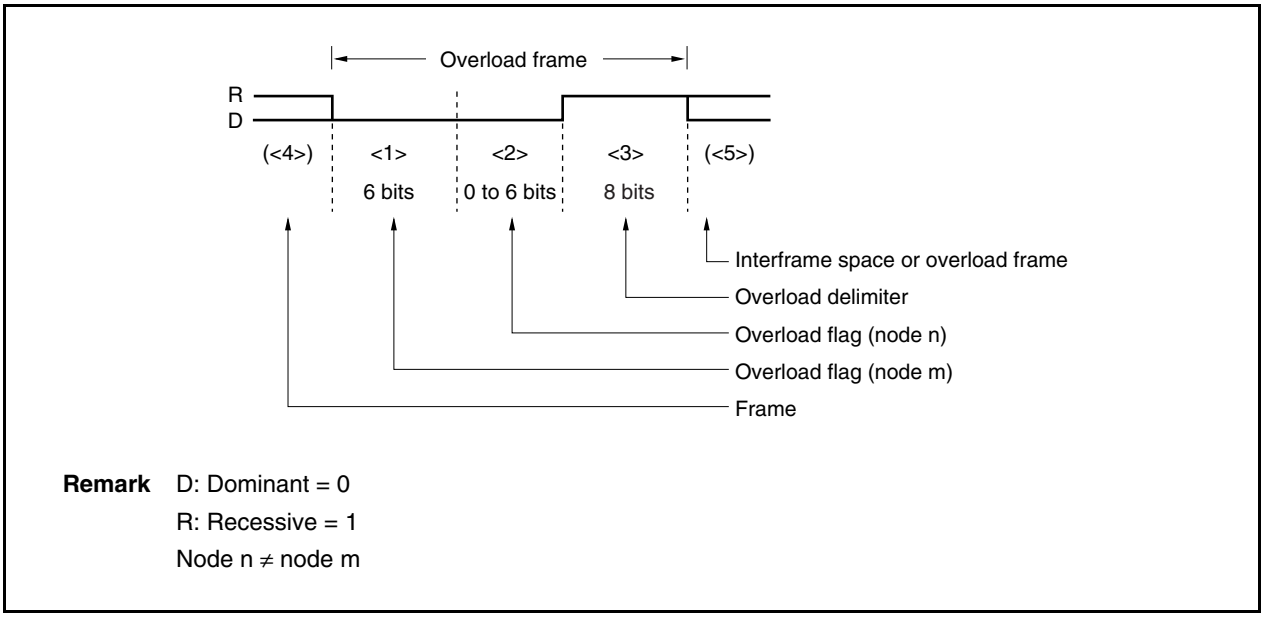
21.2.5 Overload frame

An overload frame is transmitted under the following conditions.

- When the receiving node has not completed the reception operation[Note]
- If a dominant level is detected at the first two bits during intermission
- If a dominant level is detected at the last bit (7th bit) of the end of frame or at the last bit (8th bit) of the error delimiter/overload delimiter

Note In this CAN controller, all reception frames can be loaded without outputting an overload frame because of the enough high-speed internal processing.

Figure 21-16. Overload Frame



Remark D: Dominant = 0
R: Recessive = 1
Node n ≠ node m

Table 21-8. Definition of Overload Frame Fields

No	Name	Bit Count	Definition
<1>	Overload flag	6	Outputs 6 dominant-level bits consecutively.
<2>	Overload flag from other node	0 to 6	The node that received an overload flag in the interframe space outputs an overload flag.
<3>	Overload delimiter	8	Outputs 8 recessive-level bits consecutively. If a dominant level is detected at the 8th bit, an overload frame is transmitted from the next bit.
<4>	Frame	–	Output following an end of frame, error delimiter, or overload delimiter.
<5>	Interframe space/overload frame	–	An interframe space or overload frame starts from here.

(3/3)

Set TRQ	Clear TRQ	Setting of TRQ bit
0	1	TRQ bit is cleared to 0.
1	0	TRQ bit is set to 1.
Other than above		TRQ bit is not changed.

Caution Even if the TRQ bit is set (1), transmission may not be immediately executed depending on the situation such as when a message is received from another node or when a message is transmitted from the message buffer.
Transmission under execution is not terminated midway even if the TRQ bit is cleared. Transmission is continued until it is completed (regardless of whether it is executed successfully or fails).

Set RDY	Clear RDY	Setting of RDY bit
0	1	RDY bit is cleared to 0.
1	0	RDY bit is set to 1.
Other than above		RDY bit is not changed.

Caution Be sure to set the TRQ and RDY bits separately.

(5) Processing for bulk transfer (OUT)

Bulk transfer (OUT) is allocated to Endpoint2 and Endpoint4. The flowchart shown below illustrates how Endpoint2 is controlled. Endpoint4 can also be controlled in the same sequence. To use this flowchart as the control flow of Endpoint4, therefore, read the bit names of Endpoint2 in the flowchart as those of Endpoint4.

(10) VLTP: VLAN type register

This register is used to specify the operation to be performed on a VLAN frame.

Access This register can be read and written in 32-bit units.

Address 002E 0064H

Default value 0000 0000H. This register is cleared to its default value by all types of resets.

Caution Be sure to set bits 31 to 16 to "0".

31	30	29	28	27	26	25	24
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

15	14	13	12	11	10	9	8
VLTP15	VLTP14	VLTP13	VLTP12	VLTP11	VLTP10	VLTP9	VLTP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

7	6	5	4	3	2	1	0
VLTP7	VLTP6	VLTP5	VLTP4	VLTP3	VLTP2	VLTP1	VLTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
15 to 0	VLTP[15:0]	VLAN frame operation These bits specify the operation to be performed or a VLAN frame (refer to **23.5.4 (3) Operations related to VLAN frame**). During reception: The value of VLTP[15:0] is compared with the value of the TPID field (2 bytes following the source address) of a frame to detect a VLAN frame. During transmission: If the value of the VLAN field matches the value of VLTP[15:0] when the MACC2.APD bit is set to 1, PAD is appended to the VLAN frame.

CHAPTER 29 CLOCK MONITOR

29.1 Functions

The clock monitor samples the main clock by using the internal oscillation clock and generates a reset request signal when oscillation of the main clock is stopped.

Once the operation of the clock monitor has been enabled by an operation enable flag, it cannot be cleared to 0 by any means other than reset.

When a reset by the clock monitor occurs, the RESF.CLMRF bit is set. For details on the RESF register, see **28.2 Registers to Check Reset Source**.

The clock monitor automatically stops under the following conditions.

- During oscillation stabilization time after STOP mode is released
- When the main clock is stopped (from when the PCC.MCK bit = 1 during subclock operation, until the PCC.CLS bit = 0 during main clock operation)
- When the sampling clock (internal oscillation clock) is stopped
- When the CPU operates with the internal oscillation clock

29.2 Configuration

The clock monitor includes the following hardware.

Table 29-1. Configuration of Clock Monitor

Item	Configuration
Control register	Clock monitor mode register (CLM)

Figure 29-1. Timing of Reset via $\overline{\text{RESET}}$ Pin Input

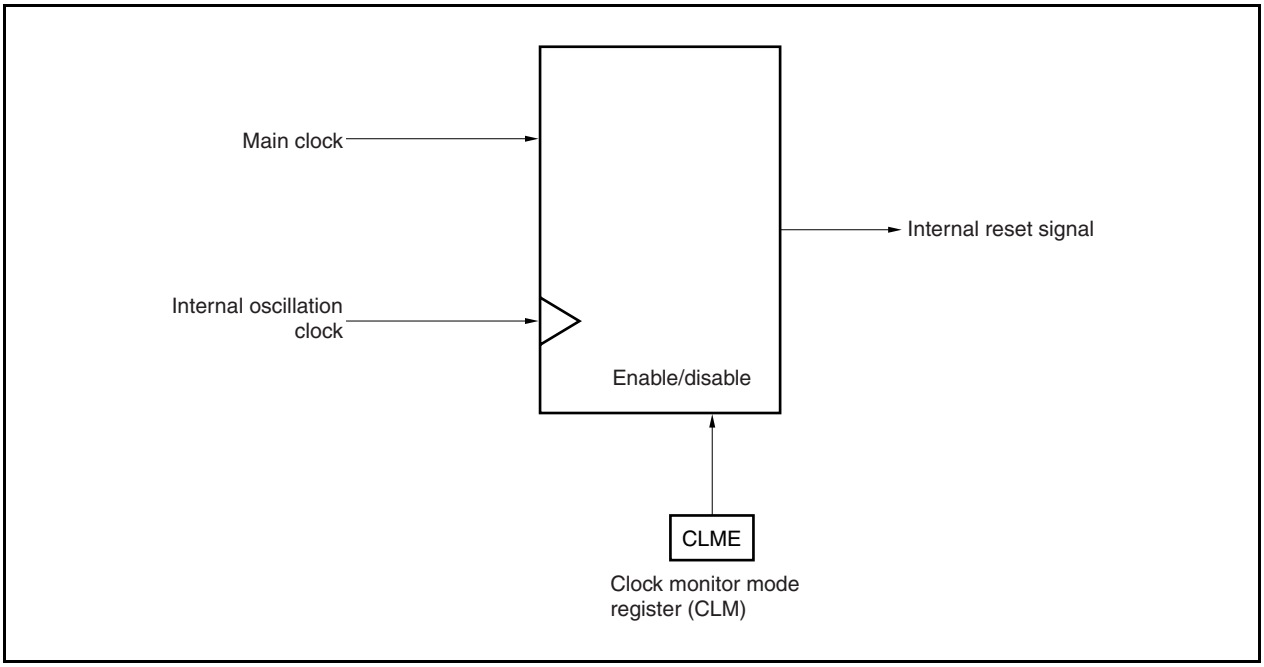


Table 33-2. Basic Functions

Function	Functional Outline	Support (√: Supported, ×: Not supported)	
		On-Board/Off-Board Programming	Self Programming
Block erasure	The contents of specified memory blocks are erased.	√	√
Chip erasure	The contents of the entire memory area are erased all at once.	√	×
Write	Writing to specified addresses, and a verify check to see if write level is secured are performed.	√	√
Verify/checksum	Data read from the flash memory is compared with data transferred from the flash programmer.	√	× (Can be read by user program)
Blank check	The erasure status of the entire memory is checked.	√	√
Security setting	Use of the block erase command, chip erase command, program command, and read command is prohibited, and rewriting of the boot area is prohibited.	√	× (Supported only when setting is changed from enable to disable)

The following table lists the security functions. The block erase command prohibit, chip erase command prohibit, and program command prohibit functions are enabled by default after shipment, and security can be set by rewriting via on-board/off-board programming. Each security function can be used in combination with the others at the same time.

Table 33-3. Security Functions

Function	Function Outline
Block erase command prohibit	Execution of a block erase command on all blocks is prohibited. Setting of prohibition can be initialized by execution of a chip erase command.
Chip erase command prohibit	Execution of block erase and chip erase commands on all the blocks is prohibited. Once prohibition is set, setting of prohibition cannot be initialized because the chip erase command cannot be executed.
Program command prohibit	Execution of program and block erase commands on all the blocks is prohibited. Setting of prohibition can be initialized by execution of the chip erase command.
Read command prohibit	Execution of a read command on all of the blocks is prohibited. Setting of the prohibition can be initialized by execution of a chip erase command.
Boot area rewrite prohibit	Execution of write, block erase, and chip erase commands on the boot area is prohibited. Setting of the prohibition of rewriting the boot area cannot be initialized after it is once set.

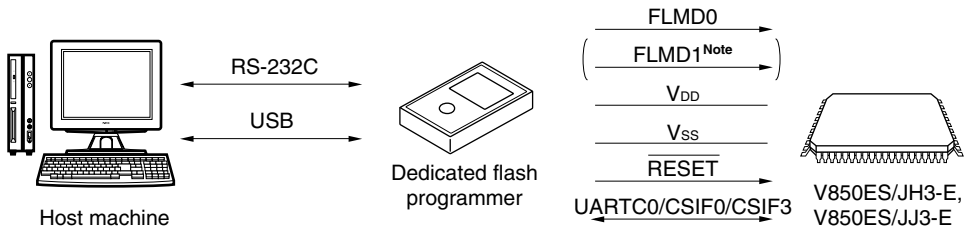
33.4 Rewriting by Dedicated Flash Programmer

The flash memory can be rewritten by using a dedicated flash programmer after the V850ES/JH3-E and V850ES/JJ3-E are mounted on the target system (on-board programming). The flash memory can also be rewritten before the device is mounted on the target system (off-board programming) by using a dedicated program adapter (FA series).

33.4.1 Programming environment

The following shows the environment required for writing programs to the flash memory of the V850ES/JH3-E and V850ES/JJ3-E.

Figure 33-2. Environment Required for Writing Programs to Flash Memory



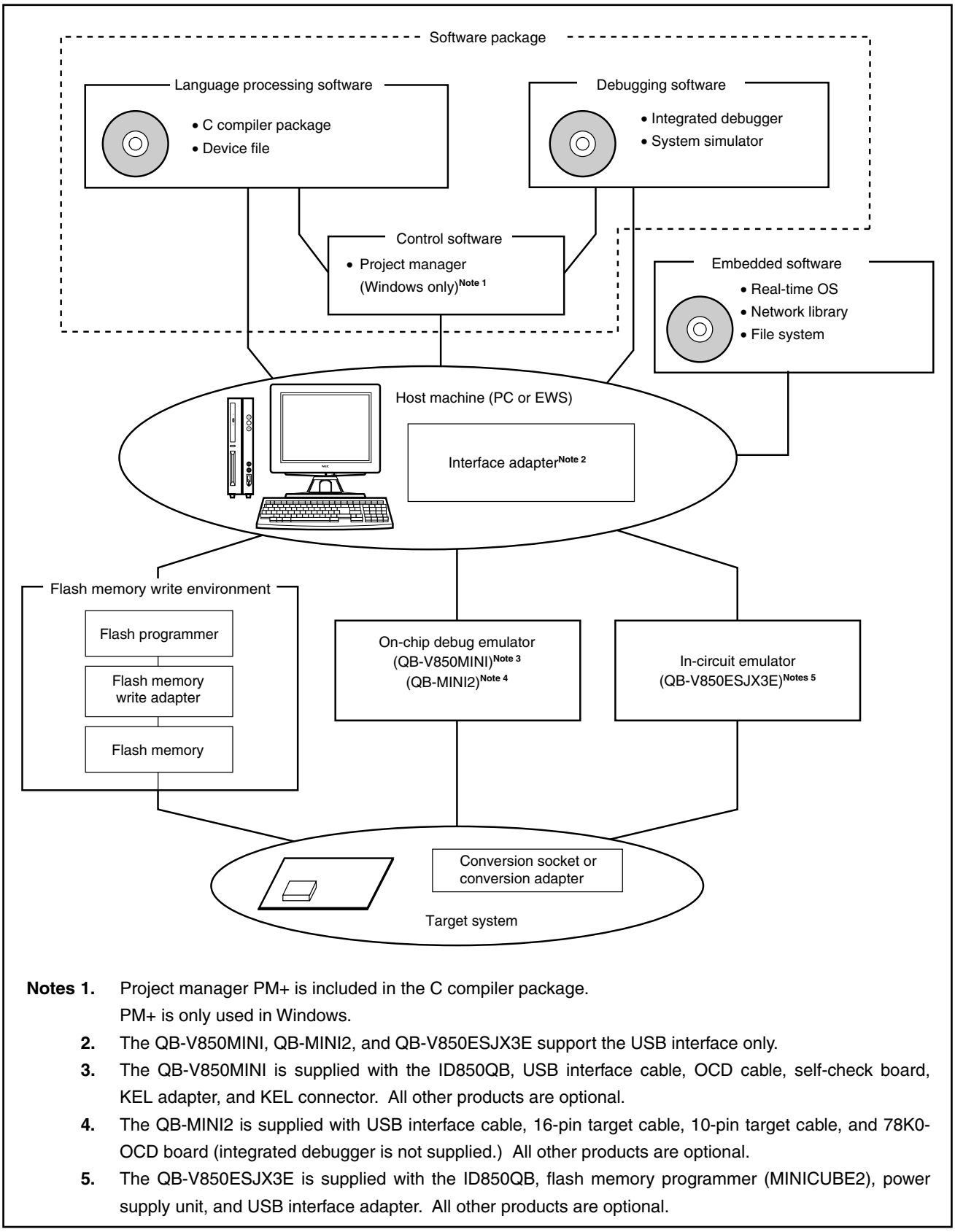
Note Connect the FLMD1 pin to the flash programmer or connect to GND via a pull-down resistor on the board.

A host machine is required for controlling the dedicated flash programmer.

UARTC0, CSIF0, or CSIF3 is used for the interface between the dedicated flash programmer and the V850ES/JH3-E and V850ES/JJ3-E to perform writing, erasing, etc. A dedicated program adapter (FA series) required for off-board writing.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Figure A-1. Development Tool Configuration



Notes 1. Project manager PM+ is included in the C compiler package.
PM+ is only used in Windows.

2. The QB-V850MINI, QB-MINI2, and QB-V850ESJX3E support the USB interface only.

3. The QB-V850MINI is supplied with the ID850QB, USB interface cable, OCD cable, self-check board, KEL adapter, and KEL connector. All other products are optional.

4. The QB-MINI2 is supplied with USB interface cable, 16-pin target cable, 10-pin target cable, and 78K0-OCD board (integrated debugger is not supplied.) All other products are optional.

5. The QB-V850ESJX3E is supplied with the ID850QB, flash memory programmer (MINICUBE2), power supply unit, and USB interface adapter. All other products are optional.