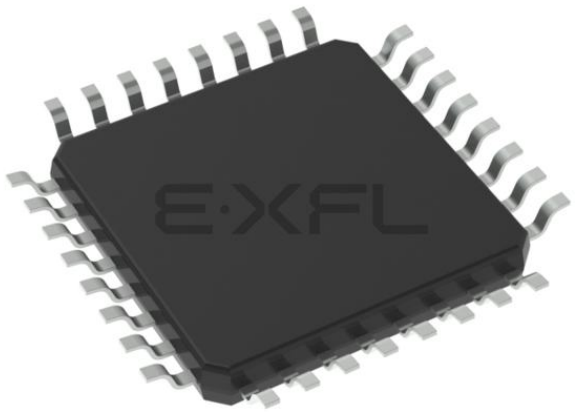

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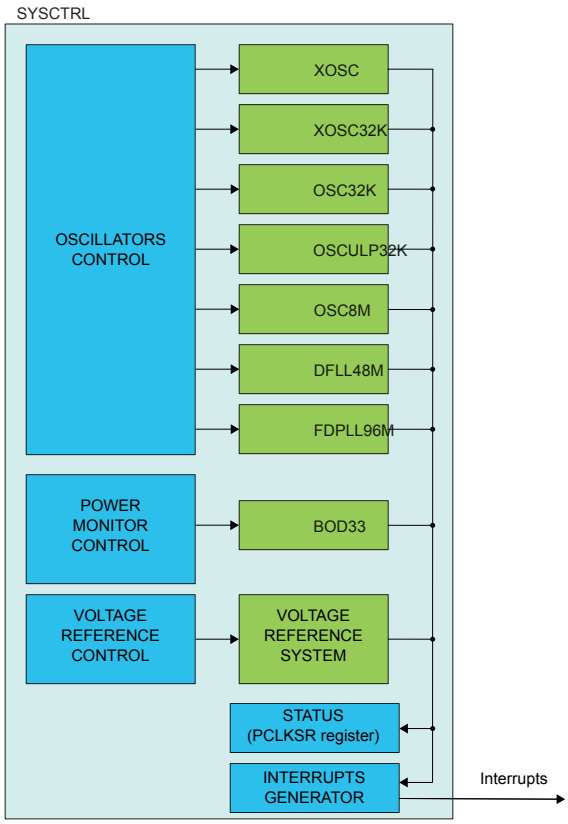
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e15b-aut

17.3 Block Diagram

Figure 17-1. SYSCTRL Block Diagram



17.4 Signal Description

Signal Name	Types	Description
XIN	Analog Input	Multipurpose Crystal Oscillator or external clock generator input
XOUT	Analog Output	External Multipurpose Crystal Oscillator output
XIN32	Analog Input	32kHz Crystal Oscillator or external clock generator input
XOUT32	Analog Output	32kHz Crystal Oscillator output

The I/O lines are automatically selected when XOSC or XOSC32K are enabled. Refer to *Oscillator Pinout*.

Related Links

I/O Multiplexing and Considerations

17.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

FILTER[1:0]	Name	Description
0x2	HBFILT	High bandwidth filter
0x3	HDFILT	High damping filter

17.8.20 DPLL Status

Name: DPLLSTATUS
Offset: 0x50
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					DIV	ENABLE	CLKRDY	LOCK
Access					R	R	R	R
Reset					0	0	0	0

Bit 3 – DIV: Divider Enable

Value	Description
0	The reference clock divider is disabled.
1	The reference clock divider is enabled.

Bit 2 – ENABLE: DPLL Enable

Value	Description
0	The DPLL is disabled.
1	The DPLL is enabled.

Bit 1 – CLKRDY: Output Clock Ready

Value	Description
0	The DPLL output clock is off
1	The DPLL output clock in on.

Bit 0 – LOCK: DPLL Lock Status

Value	Description
0	The DPLL Lock signal is cleared.
1	The DPLL Lock signal is asserted.

Bit	7	6	5	4	3	2	1	0
	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVFEO: Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 8 – CMPEO0: Compare 0 Event Output Enable

Value	Description
0	Compare 0 event is disabled and will not be generated.
1	Compare 0 event is enabled and will be generated for every compare match.

Bits 7,6,5,4,3,2,1,0 – PEREOx : Periodic Interval x Event Output Enable [x=7:0]

Value	Description
0	Periodic Interval x event is disabled and will not be generated.
1	Periodic Interval x event is enabled and will be generated.

19.8.6 Event Control - MODE1

Name: EVCTRL
Offset: 0x04
Reset: 0x0000
Property: Enable-Protected, Write-Protected

Bit	15	14	13	12	11	10	9	8
	OVFEO						CMPEO1	CMPEO0
Access	R/W						R/W	R/W
Reset	0						0	0

Bit	7	6	5	4	3	2	1	0
	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVFEO: Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bits 9,8 – CMPEOx : Compare x Event Output Enable [x=1:0]

Value	Description
0	Compare x event is disabled and will not be generated.
1	Compare x event is enabled and will be generated for every compare match.

Value	Description
0	The correction value is positive, i.e., frequency will be increased.
1	The correction value is negative, i.e., frequency will be decreased.

Bits 6:0 – VALUE[6:0]: Correction Value
These bits define the amount of correction applied to the RTC prescaler.

1–127: The RTC frequency is adjusted according to the value.

Value	Description
0	Correction is disabled and the RTC frequency is unchanged.

19.8.20 Counter Value - MODE0

Name: COUNT
Offset: 0x10
Reset: 0x00000000
Property: Read-Synchronized, Write-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0]: Counter Value
These bits define the value of the 32-bit RTC counter.

19.8.21 Counter Value - MODE1

Name: COUNT
Offset: 0x10
Reset: 0x0000
Property: Read-Synchronized, Write-Protected, Write-Synchronized

IDLE No frame is transferred on the communication line. Signal is always high in this state.

26.6.2 Basic Operation

26.6.2.1 Initialization

The following registers are enable-protected, meaning they can only be written when the USART is disabled (CTRL.ENABLE=0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits.
- Control B register (CTRLB), except the Receiver Enable (RXEN) and Transmitter Enable (TXEN) bits.
- Baud register (BAUD)

When the USART is enabled or is being enabled (CTRLA.ENABLE=1), any writing attempt to these registers will be discarded. If the peripheral is being disabled, writing to these registers will be executed after disabling is completed. Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the USART is enabled, it must be configured by these steps:

1. Select either external (0x0) or internal clock (0x1) by writing the Operating Mode value in the CTRLA register (CTRLA.MODE).
2. Select either asynchronous (0) or or synchronous (1) communication mode by writing the Communication Mode bit in the CTRLA register (CTRLA.CMODE).
3. Select pin for receive data by writing the Receive Data Pinout value in the CTRLA register (CTRLA.RXPO).
4. Select pads for the transmitter and external clock by writing the Transmit Data Pinout bit in the CTRLA register (CTRLA.TXPO).
5. Configure the Character Size field in the CTRLB register (CTRLB.CHSIZE) for character size.
6. Set the Data Order bit in the CTRLA register (CTRLA.DORD) to determine MSB- or LSB-first data transmission.
7. To use parity mode:
    7.1. Enable parity mode by writing 0x1 to the Frame Format field in the CTRLA register (CTRLA.FORM).
    7.2. Configure the Parity Mode bit in the CTRLB register (CTRLB.PMODE) for even or odd parity.
8. Configure the number of stop bits in the Stop Bit Mode bit in the CTRLB register (CTRLB.SBMODE).
9. When using an internal clock, write the Baud register (BAUD) to generate the desired baud rate.
10. Enable the transmitter and receiver by writing '1' to the Receiver Enable and Transmitter Enable bits in the CTRLB register (CTRLB.RXEN and CTRLB.TXEN).

26.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing ‘1’ to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

Refer to the CTRLA register description for details.

CPOL	TxD Change	RxD Sample
0x0	Rising XCK edge	Falling XCK edge
0x1	Falling XCK edge	Rising XCK edge

Bit 28 – CMODE: Communication Mode
This bit selects asynchronous or synchronous communication.

This bit is not synchronized.

Value	Description
0	Asynchronous communication.
1	Synchronous communication.

Bits 27:24 – FORM[3:0]: Frame Format
These bits define the frame format.

These bits are not synchronized.

FORM[3:0]	Description
0x0	USART frame
0x1	USART frame with parity
0x2-0x3	Reserved
0x4	Auto-baud - break detection and auto-baud.
0x5	Auto-baud - break detection and auto-baud with parity
0x6-0xF	Reserved

Bits 23:22 – SAMPA[1:0]: Sample Adjustment
These bits define the sample adjustment.

These bits are not synchronized.

SAMPA[1:0]	16x Over-sampling (CTRLA.SAMPR=0 or 1)	8x Over-sampling (CTRLA.SAMPR=2 or 3)
0x0	7-8-9	3-4-5
0x1	9-10-11	4-5-6
0x2	11-12-13	5-6-7
0x3	13-14-15	6-7-8

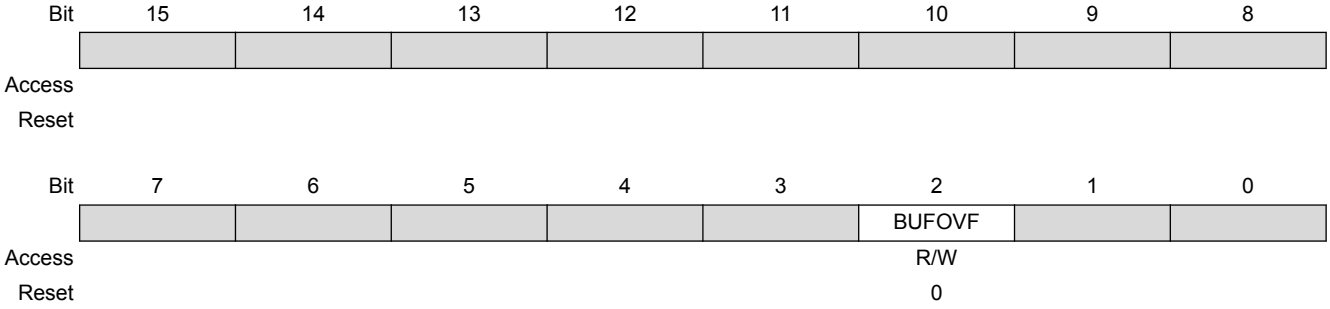
Bits 21:20 – RXPO[1:0]: Receive Data Pinout
These bits define the receive data (RxD) pin configuration.

These bits are not synchronized.

RXPO[1:0]	Name	Description
0x0	PAD[0]	SERCOM PAD[0] is used for data reception
0x1	PAD[1]	SERCOM PAD[1] is used for data reception

27.8.7 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: –



Bit 2 – BUFOVF: Buffer Overflow
Reading this bit before reading DATA will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a buffer overflow condition is detected. See also CTRLA.IBON for overflow handling.

When set, the corresponding RxDATA will be zero.

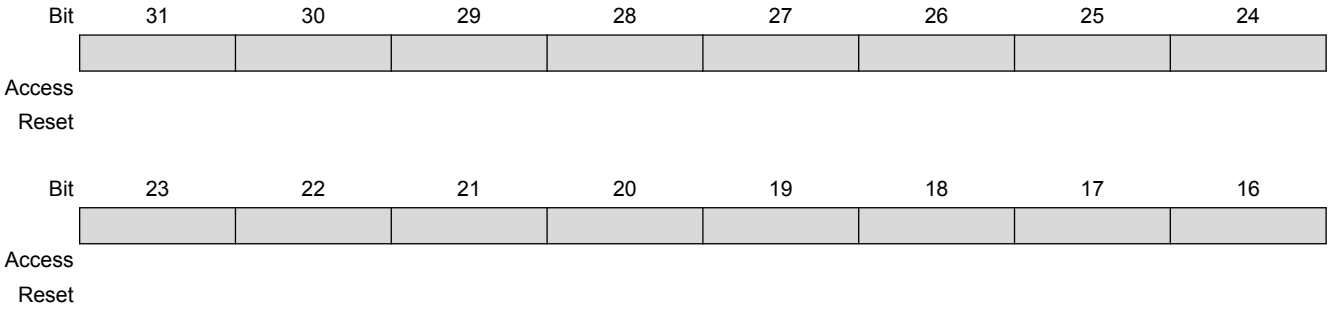
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Buffer Overflow has occurred.
1	A Buffer Overflow has occurred.

27.8.8 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -



- Data (DATA) when in master operation

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

Related Links

Register Synchronization

28.10 Register Description - I²C Master

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to Synchronization.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

28.10.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		LOWTOUT	INACTOUT[1:0]		SCLSM		SPEED[1:0]	
Access		R/W	R/W	R/W	R/W		R/W	R/W
Reset		0	0	0	0		0	0

Bit	23	22	21	20	19	18	17	16
	SEXTTOEN	MEXTTOEN	SDAHOLD[1:0]					PINOUT
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

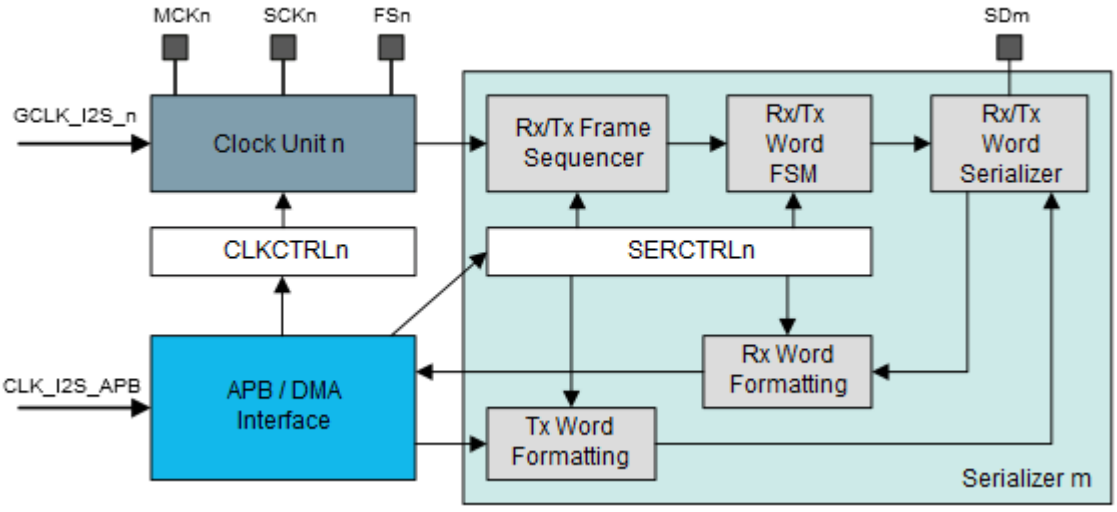
Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – LOWTOUT: SCL Low Time-Out
This bit enables the SCL low time-out. If SCL is held low for 25ms-35ms, the master will release its clock hold, if enabled, and complete the current transaction. A stop condition will automatically be transmitted.

INTFLAG.SB or INTFLAG.MB will be set as normal, but the clock hold will be released. The STATUS.LOWTOUT and STATUS.BUSERR status bits will be set.

This bit is not synchronized.

Figure 29-3. I²S Functional Block Diagram



29.6.1.1 Initialization

The I²S features two Clock Units, and two Serializers configurable as Receiver or Transmitter. The two Serializers can either share the same Clock Unit or use separate Clock Units.

Before enabling the I²S, the following registers must be configured:

- Clock Control registers (CLKCTRLn)
- Serializer Control registers (SERCTRLm)

In Master mode, one of the generic clocks for the I²S must also be configured to operate at the required frequency, as described in Principle of Operation.

- *fs* is the sampling frequency that defines the frame period
- CLKCTRLn.NBSLOTS defines the number of slots in each frame
- CLKCTRLn.SLOTSIZE defines the number of bits in each slot
- SCKn frequency must be f_{SCKn} = *fs* × number_of_slots × number_of_bits_per_slot)

Once the configuration has been written, the I²S Clock Units and Serializers can be enabled by writing a '1' to the CKENn and SERENm bits and to the ENABLE bit in the Control register (CTRLA). The Clock Unit n can be enabled alone, in Controller Mode, to output clocks to the MCKn, SCKn, and FSn pins. The Clock Units must be enabled if Serializers are enabled.

The Clock Units and the Serializers can be disabled independently by writing a '0' to CTRLA.CKENn or CTRLA.SERENm, respectively. Once requested to stop, they will only stop when the pending transmit frames will be completed, if any. When requested to stop, the ongoing reception of the current slot will be completed and then the Serializer will be stopped.

Example Requirements: fs*=48kHz, MCKn=384×*fs

If a 384×*fs* MCKn Master Clock is required (i.e. 18.432MHz), the I²S generic clock could run at 18.432MHz with a Master Clock Output Division Factor of 1 (selected by writing CLKCTRLn.MCKOUTDIV=0x0) in order to obtain the desired MCKn frequency.

When using 6 slots per frame (CLKCTRLn.NBSLOTS=0x5) and 32-bit slots (CLKCTRLn.SLOTSIZE=0x3), the desired SCKn frequency is

f_{SCKn} = 48kHz × 6 × 32 = 9.216MHz

data is also received. For instance, writing SERCTRL0.RXLOOP=1 will connect SD1 output to SD0 input, or writing SERCTRL1.RXLOOP=1 will connect SD0 output to SD1 input.

RXLOOP=1 will connect the Transmitter output of the other Serializer to the Receiver input of the current Serializer. For the Loop-back Mode to work, the current Serializer must be configured as receiver and the other Serializer as transmitter.

Writing SERCTRLm.RXLOOP=0 will restore normal behavior and connection between Serializer m and SDm pin input.

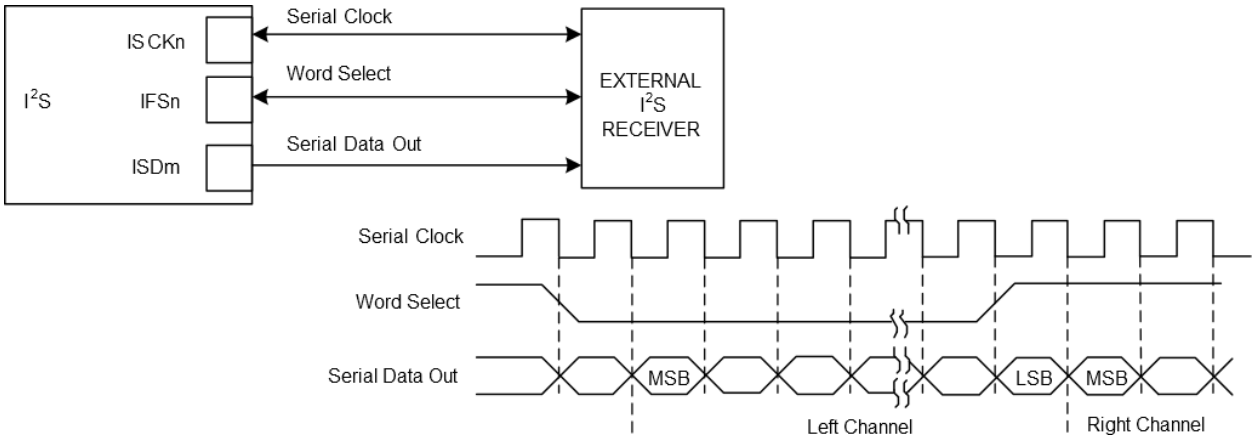
As for other changes to the Serializer configuration, Serializer m must be disabled before writing the SERCTRLm register to update SERCTRLm.RXLOOP.

29.7 I²S Application Examples

The I²S can support several serial communication modes used in audio or high-speed serial links. Some standard applications are shown in the following figures.

Note: The following examples are not a complete list of serial link applications supported by the I²S.

Figure 29-7. Audio Application Block Diagram



31. TCC – Timer/Counter for Control Applications

31.1 Overview

The device provides three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC[2:0].

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation such as frequency generation and pulse-width modulation.

Waveform extensions are intended for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. They allow for low- and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

Figure 31-1 shows all features in TCC.

Related Links

TCC Configurations

31.2 Features

- Up to four compare/capture channels (CC) with:
  - Double buffered period setting
  - Double buffered compare or capture channel
  - Circular buffer on period and compare channel registers
- Waveform generation:
  - Frequency generation
  - Single-slope pulse-width modulation (PWM)
  - Dual-slope pulse-width modulation with half-cycle reload capability
- Input capture:
  - Event capture
  - Frequency capture
  - Pulse-width capture
- Waveform extensions:
  - Configurable distribution of compare channels outputs across port pins
  - Low- and high-side output with programmable dead-time insertion
  - Waveform swap option with double buffer support
  - Pattern generation with double buffer support
  - Dithering support
- Fault protection for safe disabling of drivers:
  - Two recoverable fault sources
  - Two non-recoverable fault sources
  - Debugger can be source of non-recoverable fault

Bit	31	30	29	28	27	26	25	24
					FILTERVAL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BLANKVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bits 27:24 – FILTERVAL[3:0]: Recoverable Fault n Filter Value
These bits define the filter value applied on MCEx (x=0,1) event input line. The value must be set to zero when MCEx event is used as synchronous event.

Bits 23:16 – BLANKVAL[7:0]: Recoverable Fault n Blanking Value
These bits determine the duration of the blanking of the fault input source. Activation and edge selection of the blank filtering are done by the BLANK bits (FCTRLn.BLANK).

When enabled, the fault input source is internally disabled for BLANKVAL* prescaled GCLK_TCC periods after the detection of the waveform edge.

Bits 14:12 – CAPTURE[2:0]: Recoverable Fault n Capture Action
These bits select the capture and Fault n interrupt/event conditions.

Table 31-8. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.

Bits 16, 17, 18, 19 – POLn: Channel Polarity x
Setting these bits enables the output polarity in single-slope and dual-slope PWM operations.

Value	Name	Description
0	(single-slope PWM waveform generation)	Compare output is initialized to ~DIR and set to DIR when TCC counter matches CCx value
1	(single-slope PWM waveform generation)	Compare output is initialized to DIR and set to ~DIR when TCC counter matches CCx value.
0	(dual-slope PWM waveform generation)	Compare output is set to ~DIR when TCC counter matches CCx value
1	(dual-slope PWM waveform generation)	Compare output is set to DIR when TCC counter matches CCx value.

Bits 8, 9, 10, 11 – CICCENn: Circular CC Enable x
Setting this bits enables the compare circular buffer option on channel. When the bit is set, CCx register value is copied-back into the CCx register on UPDATE condition.

Bit 7 – CIPEREN: Circular Period Enable
Setting this bits enable the period circular buffer option. When the bit is set, the PER register value is copied-back into the PERB register on UPDATE condition.

Bits 5:4 – RAMP[1:0]: Ramp Operation
These bits select Ramp operation (RAMP). These bits are not synchronized.

Value	Name	Description
0x0	RAMP1	RAMP1 operation
0x1	RAMP2A	Alternative RAMP2 operation
0x2	RAMP2	RAMP2 operation
0x3	-	Reserved

Bits 2:0 – WAVEGEN[2:0]: Waveform Generation Operation
These bits select the waveform generation operation. The settings impact the top value and control if frequency or PWM waveform generation should be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Top	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/Event Up Down	
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3	Reserved	–	–	–	–	–	–	–
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	–	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	–	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	–

31.8.17 Period Value

Name: PER

32.8.3.7 Device Interrupt EndPoint Set n

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Endpoint Interrupt Enable Set (EPINTENCLR) register. This register is cleared by USB reset or when EPEN[n] is zero.

Name: EPINTENSETn
Offset: 0x109 + (n x 0x20)
Reset: 0x0000
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
			STALL	RXSTP		TRFAIL		TRCPT
Access			R/W	R/W		R/W		R/W
Reset			0	0		0		0

Bit 5 – STALL: Transmit Stall x Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will enable the Transmit bank x Stall interrupt.

Value	Description
0	The Transmit Stall x interrupt is disabled.
1	The Transmit Stall x interrupt is enabled.

Bit 4 – RXSTP: Received Setup Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will enable the Received Setup interrupt.

Value	Description
0	The Received Setup interrupt is disabled.
1	The Received Setup interrupt is enabled.

Bit 2 – TRFAIL: Transfer Fail bank x Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will enable the Transfer Fail interrupt.

Value	Description
0	The Transfer Fail interrupt is disabled.
1	The Transfer Fail interrupt is enabled.

Bit 0 – TRCPT: Transfer Complete bank x interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will enable the Transfer Complete x interrupt.

0.2.4 Device Registers - Endpoint RAM

Value	Description
0	The Transfer Complete bank x interrupt is disabled.
1	The Transfer Complete bank x interrupt is enabled.

35. DAC – Digital-to-Analog Converter

35.1 Overview

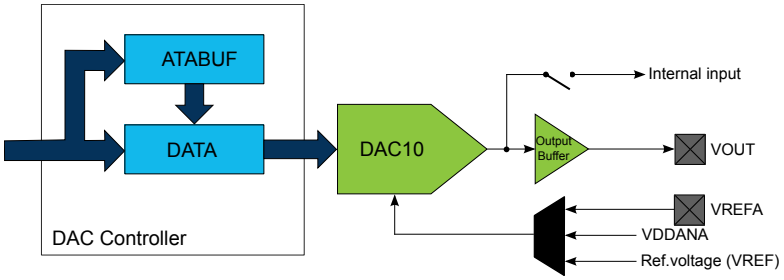
The Digital-to-Analog Converter (DAC) converts a digital value to a voltage. The DAC has one channel with 10-bit resolution, and it is capable of converting up to 350,000 samples per second (350ksps).

35.2 Features

- DAC with 10-bit resolution
- Up to 350ksps conversion rate
- Multiple trigger sources
- High-drive capabilities
- Output can be used as input to the Analog Comparator (AC)
- DMA support

35.3 Block Diagram

Figure 35-1. DAC Block Diagram



35.4 Signal Description

Signal Name	Type	Description
VOUT	Analog output	DAC output
VREFA	Analog input	External reference

Related Links

I/O Multiplexing and Considerations

35.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

35.5.1 I/O Lines

Using the DAC Controller's I/O lines requires the I/O pins to be configured using the port configuration (PORT).

37. Electrical Characteristics

37.1 Disclaimer

All typical values are measured at T = 25°C unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

37.2 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 37-1. Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Units
V_{DD}	Power supply voltage	0	3.8	V
I_{VDD}	Current into a V_{DD} pin	-	92(1)	mA
I_{GND}	Current out of a GND pin	-	130(1)	mA
V_{PIN}	Pin voltage with respect to GND and V_{DD}	GND-0.6V	V_{DD}+0.6V	V
$T_{storage}$	Storage temperature	-60	150	°C

1. Maximum source current is 46mA and maximum sink current is 65mA per cluster. A cluster is a group of GPIOs as shown in the table below. Also note that each VDD/GND pair is connected to two clusters so current consumption through the pair will be a sum of the clusters source/sink currents.

Caution: This device is sensitive to electrostatic discharges (ESD). Improper handling may lead to permanent performance degradation or malfunctioning.
Handle the device following best practice ESD protection rules: Be aware that the human body can accumulate charges large enough to impair functionality or destroy the device.

Caution: In debugger cold-plugging mode, NVM erase operations are not protected by the BOD33 and BOD12. NVM erase operation at supply voltages below specified minimum can cause corruption of NVM areas that are mandatory for correct device behavior.

Related Links
GPIO Clusters

37.3 General Operating Ratings

The device must operate within the ratings in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 37-57. FDPLL96M Characteristics(1) (Device Variant B / Die Revision E)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input frequency		32	-	2000	KHz
f_{OUT}	Output frequency		48	-	96	MHz
$I_{FDPLL96M}$	Current consumption	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	500	700	µA
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	900	1200	
J_p	Period jitter	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	1.5	2.1	%
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	4.0	10.0	
		f_{IN}= 2 MHz, f_{OUT}= 48 MHz	-	1.6	2.2	
		f_{IN}= 2 MHz, f_{OUT}= 96 MHz	-	4.6	10.2	
t_{LOCK}	Lock Time	After start-up, time to get lock signal. f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	1.2	2	ms
		f_{IN}= 2 MHz, f_{OUT}= 96 MHz	-	25	50	µs
Duty	Duty cycle		40	50	60	%

Table 37-58. FDPLL96M Characteristics(1) (Device Variant B and C / Die Revision F)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input frequency		32	-	2000	KHz
f_{OUT}	Output frequency		48	-	96	MHz
$I_{FDPLL96M}$	Current consumption	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	500	-	µA
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	900	-	
J_p	Period jitter	f_{IN}= 32 kHz, f_{OUT}= 48 MHz	-	2.2	3.0	%
		f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	3.7	9.0	
		f_{IN}= 2 MHz, f_{OUT}= 48 MHz	-	2.2	3.0	
		f_{IN}= 2 MHz, f_{OUT}= 96 MHz	-	4.4	9.7	
t_{LOCK}	Lock Time	After start-up, time to get lock signal. f_{IN}= 32 kHz, f_{OUT}= 96 MHz	-	1.0	2	ms
		f_{IN}= 2 MHz, f_{OUT}= 96 MHz	-	22	50	µs
Duty	Duty cycle		40	50	60	%

Note:

1. All values have been characterized with FILTSEL[1/0] as default value.

38. Packaging Information

38.1 Thermal Considerations

Related Links

Junction Temperature

38.1.1 Thermal Resistance Data

The following Table summarizes the thermal resistance data depending on the package.

Table 38-1. Thermal Resistance Data

Package Type	θ_{JA}	θ_{JC}
32-pin TQFP	64.7°C/W	23.1°C/W
48-pin TQFP	63.6°C/W	12.2°C/W
64-pin TQFP	60.9°C/W	12.2°C/W
32-pin QFN	40.9°C/W	15.2°C/W
48-pin QFN	32.0°C/W	10.9°C/W
64-pin QFN	32.5°C/W	10.7°C/W
35-ball WLCSP	41.8°C/W	2.26°C/W

38.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- θ_{JC} = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- P_D = Device power consumption (W)
- T_A = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Related Links

Thermal Considerations

Table 44-15. Differential Mode (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number Of Bits	With gain compensation	-	10.5	10.9	bits
TUE	Total Unadjusted Error	1x Gainn	1.5	4.3	17.0	LSB
INLI	Integral Non Linearity	1x Gainn	1.0	1.3	6.5	LSB
DNL	Differential Non Linearity	1x Gainn	+/-0.3	+/-0.5	+/-0.95	LSB
	Gain Error	Ext. Ref 1x	-15.0	2.5	+20.0	mV
		$V_{REF}=V_{DDANA}/1.48$	-20.0	-1.5	+20.0	mV
		Bandgap	-15.0	-5.0	+15.0	mV
	Gain Accuracy(5)	Ext. Ref. 0.5x	+/-0.1	+/-0.2	+/-0.45	%
		Ext. Ref. 2x to 16x	+/-0.1	+/-0.2	+/-2.0	%
	Offset Error	Ext. Ref. 1x	-10.0	-1.5	+10.0	mV
		$V_{REF}=V_{DDANA}/1.48$	-10.0	0.5	+15.0	mV
		Bandgap	-10.0	3.0	+15.0	mV
SFDR	Spurious Free Dynamic Range	1x Gain F_{CLK_ADC} = 2.1MHz F_{IN} = 40kHz A_{IN} = 95%FSR	64.2	70.0	78.9	dB
SINAD	Signal-to-Noise and Distortion		64.1	65.0	66	dB
SNR	Signal-to-Noise Ratio		64.3	65.5	66.0	dB
THD	Total Harmonic Distortion		-74.8	-64.0	-65.0	dB
	Noise RMS	T=25°C	0.6	1.0	1.6	mV

Table 44-16. Differential Mode (Device Variant B)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number Of Bits	With gain compensation	-	10.5	10.8	bits
TUE	Total Unadjusted Error	1x Gainn	1.5	2.7	14	LSB
INLI	Integral Non Linearity	1x Gainn	0.9	1.3	4	LSB
DNL	Differential Non Linearity	1x Gainn	+/-0.3	+/-0.5	+/-0.95	LSB
	Gain Error	Ext. Ref 1x	-10.0	-1.3	+10	mV
		$V_{REF}=V_{DDANA}/1.48$	-25.0	-10.1	+10.0	mV
		Bandgap	-25.0	+2	+10.0	mV
	Gain Accuracy(5)	Ext. Ref. 0.5x	+/-0.005	+/-0.05	+/-0.15	%
		Ext. Ref. 2x to 16x	+/-0.1	+/-0.03	+/-0.5	%
	Offset Error	Ext. Ref. 1x	-8.0	-1.0	+8.0	mV
		$V_{REF}=V_{DDANA}/1.48$	-8.0	0.6	+8.0	mV
		Bandgap	-6.0	-1.0	+8.0	mV