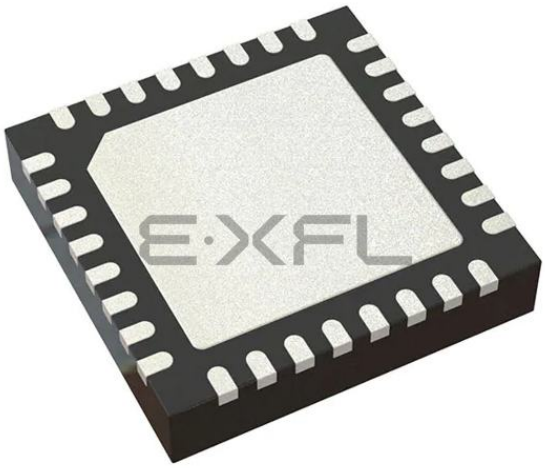

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e15b-mut

Related Links

Electrical Characteristics

8.3 Power-Up

This section summarizes the power-up sequence of the device. The behavior after power-up is controlled by the Power Manager. Refer to *PM – Power Manager* for details.

Related Links

PM – Power Manager

8.3.1 Starting of Clocks

After power-up, the device is set to its initial state and kept in reset, until the power has stabilized throughout the device. Once the power has stabilized, the device will use a 1MHz clock. This clock is derived from the 8MHz Internal Oscillator (OSC8M), which is divided by eight and used as a clock source for generic clock generator 0. Generic clock generator 0 is the main clock for the Power Manager (PM).

Some synchronous system clocks are active, allowing software execution.

Refer to the “Clock Mask Register” section in *PM – Power Manager* for the list of default peripheral clocks running. Synchronous system clocks that are running are by default not divided and receive a 1MHz clock through generic clock generator 0. Other generic clocks are disabled except GCLK_WDT, which is used by the Watchdog Timer (WDT).

Related Links

PM – Power Manager

8.3.2 I/O Pins

After power-up, the I/O pins are tri-stated.

8.3.3 Fetching of Initial Instructions

After reset has been released, the CPU starts fetching PC and SP values from the reset address, which is 0x00000000. This address points to the first executable address in the internal flash. The code read from the internal flash is free to configure the clock system and clock sources. Refer to *PM – Power Manager*, *GCLK – Generic Clock Controller* and *SYSCTRL – System Controller* for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

Related Links

PM – Power Manager

SYSCTRL – System Controller

Clock System

8.4 Power-On Reset and Brown-Out Detector

The SAM D21 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on reset on VDDANA
- BOD33: Brown-out detector on VDDANA
- BOD12: Voltage Regulator Internal Brown-out detector on VDDCORE. The Voltage Regulator Internal BOD is calibrated in production and its calibration configuration is stored in the NVM User Row. This configuration should not be changed if the user row is written to assure the correct behavior of the BOD12.

FILTER[1:0]	Name	Description
0x2	HBFILT	High bandwidth filter
0x3	HDFILT	High damping filter

17.8.20 DPLL Status

Name: DPLLSTATUS
Offset: 0x50
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					DIV	ENABLE	CLKRDY	LOCK
Access					R	R	R	R
Reset					0	0	0	0

Bit 3 – DIV: Divider Enable

Value	Description
0	The reference clock divider is disabled.
1	The reference clock divider is enabled.

Bit 2 – ENABLE: DPLL Enable

Value	Description
0	The DPLL is disabled.
1	The DPLL is enabled.

Bit 1 – CLKRDY: Output Clock Ready

Value	Description
0	The DPLL output clock is off
1	The DPLL output clock in on.

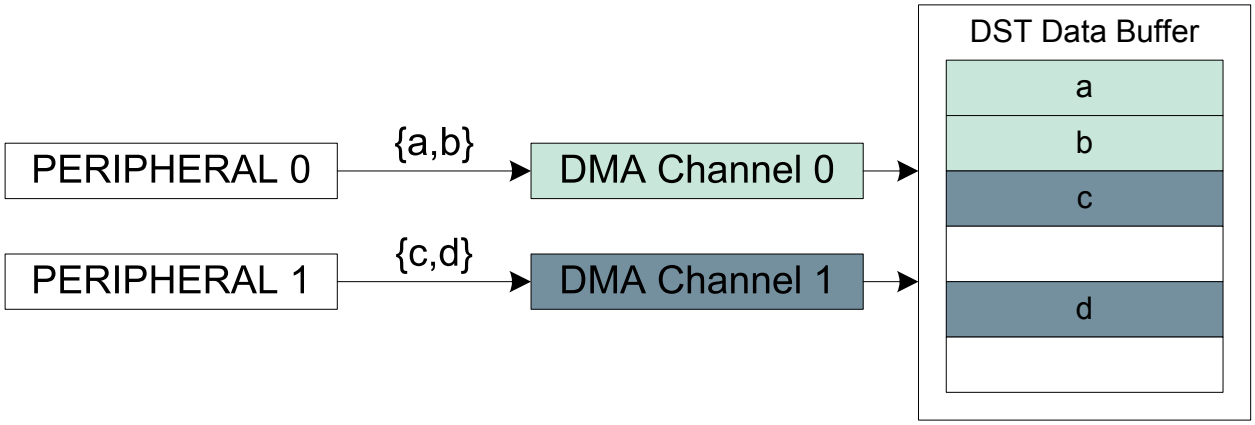
Bit 0 – LOCK: DPLL Lock Status

Value	Description
0	The DPLL Lock signal is cleared.
1	The DPLL Lock signal is asserted.

- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

Figure 20-9shows an example where DMA channel 0 is configured to increment destination address by one beat (BTCTRL.DSTINC=1) and DMA channel 1 is configured to increment destination address by two beats (BTCTRL.DSTINC=1, BTCTRL.STEPSEL=0, and BTCTRL.STEPSIZE=0x1). As the source address for both channels are peripherals, source incrementation is disabled (BTCTRL.SRCINC=0).

Figure 20-9. Destination Address Increment



20.6.2.8 Error Handling

If a bus error is received from an AHB slave during a DMA data transfer, the corresponding active channel is disabled and the corresponding Channel Transfer Error Interrupt flag in the Channel Interrupt Status and Clear register (CHINTFLAG.TERR) is set. If enabled, the optional transfer error interrupt is generated. The transfer counter will not be decremented and its current value is written-back in the write-back memory section before the channel is disabled.

When the DMAC fetches an invalid descriptor (BTCTRL.VALID=0) or when the channel is resumed and the DMA fetches the next descriptor with null address (DESCADDR=0x00000000), the corresponding channel operation is suspended, the Channel Suspend Interrupt Flag in the Channel Interrupt Flag Status and Clear register (CHINTFLAG.SUSP) is set, and the Channel Fetch Error bit in the Channel Status register (CHSTATUS.FERR) is set. If enabled, the optional suspend interrupt is generated.

20.6.3 Additional Features

20.6.3.1 Linked Descriptors

A transaction can consist of either a single block transfer or of several block transfers. When a transaction consist of several block transfers it is called linked descriptors.

Figure Figure 20-3 illustrates how linked descriptors work. When the first block transfer is completed on DMA channel 0, the DMAC fetches the next transfer descriptor which is pointed to by the value stored in the Next Descriptor Address (DESCADDR) register of the first transfer descriptor. Fetching the next transfer descriptor (DESCADDR) is continued until the last transfer descriptor. When the block transfer for the last transfer descriptor is executed and DESCADDR=0x00000000, the transaction is terminated. For further details on how the next descriptor is fetched from SRAM, refer to section Data Transmission.

Adding Descriptor to the End of a List

To add a new descriptor at the end of the descriptor list, create the descriptor in SRAM, with DESCADDR=0x00000000 indicating that it is the new last descriptor in the list, and modify the DESCADDR value of the current last descriptor to the address of the newly created descriptor.

Modifying a Descriptor in a List

In order to add descriptors to a linked list, the following actions must be performed:

Value	Name	Description
0x2E	CHN	DMA channel 14
0x2F	CHN	DMA channel 15
0x30	CHN	DMA channel 16
0x31	CHN	DMA channel 17
0x32	CHN	DMA channel 18
0x33	CHN	DMA channel 19
0x34	CHN	DMA channel 20
0x35	CHN	DMA channel 21
0x36	CHN	DMA channel 22
0x37	CHN	DMA channel 23
0x38	CHN	DMA channel 24
0x39	CHN	DMA channel 25
0x3A	CHN	DMA channel 26
0x3B	CHN	DMA channel 27
0x3C	CHN	DMA channel 28
0x3D	CHN	DMA channel 29
0x3E	CHN	DMA channel 30
0x3F	CHN	DMA channel 31

Bits 3:2 – CRCPOLY[1:0]: CRC Polynomial Type
These bits define the size of the data transfer for each bus access when the CRC is used with I/O interface, as shown in the table below.

Value	Name	Description
0x0	CRC16	CRC-16 (CRC-CCITT)
0x1	CRC32	CRC32 (IEEE 802.3)
0x2-0x3		Reserved

Bits 1:0 – CRCBEATSIZE[1:0]: CRC Beat Size
These bits define the size of the data transfer for each bus access when the CRC is used with I/O interface.

Value	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	HWORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
0x3		Reserved

20.8.3 CRC Data Input

Name: CRCDATAIN
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

23.5.9 Analog Connections

Analog functions are connected directly between the analog blocks and the I/O pads using analog buses. However, selecting an analog peripheral function for a given pin will disable the corresponding digital features of the pad.

23.5.10 CPU Local Bus

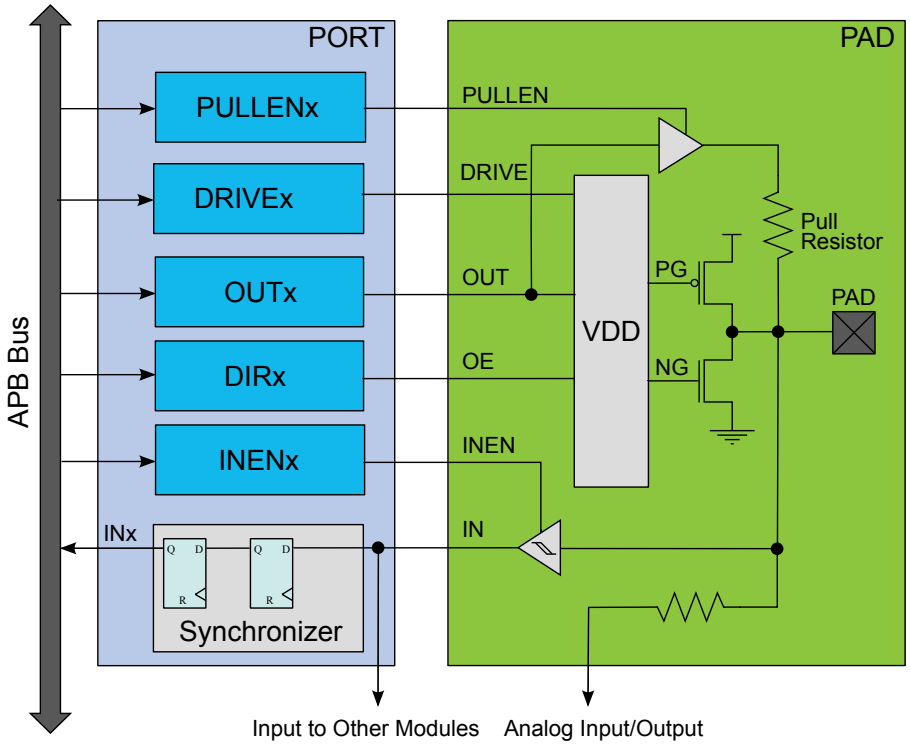
The CPU local bus (IOBUS) is an interface that connects the CPU directly to the PORT. It is a single-cycle bus interface, which does not support wait states. It supports 8-bit, 16-bit and 32-bit sizes.

This bus is generally used for low latency operation. The Data Direction (DIR) and Data Output Value (OUT) registers can be read, written, set, cleared or be toggled using this bus, and the Data Input Value (IN) registers can be read.

Since the IOBUS cannot wait for IN register resynchronization, the Control register (CTRL) must be configured to continuous sampling of all pins that need to be read via the IOBUS in order to prevent stale data from being read.

23.6 Functional Description

Figure 23-2. Overview of the PORT



0x2: SPI slave operation

0x3: SPI master operation

These bits are not synchronized.

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST: Software Reset
Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing "1' to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY. SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

27.8.2 Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RXEN	
Access							R/W	
Reset							0	

This flag is set when a Sequencer x has received a new data word, and will generate an interrupt request if INTENCLR/SET.RXRDYx is set to '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Ready x interrupt flag.

29.9.6 Synchronization Busy

Name: SYNCBUSY
Offset: 0x18
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
							DATA1	DATA0
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
			SEREN1	SEREN0	CKEN1	CKEN0	ENABLE	SWRST
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bits 8,9 – DATAx : Data x Synchronization Status [x=1..0]
Bit DATAx is cleared when the synchronization of DATA Holding register (DATAx) between the clock domains is complete.

Bit DATAx is set when the synchronization of DATA Holding register (DATAx) between the clock domains is started.

Bits 4,5 – SERENx : Serializer x Enable Synchronization Status [x=1..0]
Bit SERENx is cleared when the synchronization of CTRLA.SERENx bit between the clock domains is complete.

Bit SERENx is set when the synchronization of CTRLA.SERENx bit between the clock domains is started.

Bits 2,3 – CKENx : Clock Unit x Enable Synchronization Status [x=1..0]
Bit CKENx is cleared when the synchronization of CTRLA.CKENx bit between the clock domains is complete.

Bit CKENx is set when the synchronization of CTRLA.CKENx bit between the clock domains is started.

Bit 1 – ENABLE: Enable Synchronization Status
This bit is cleared when the synchronization of CTRLA.ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of CTRLA.ENABLE bit between the clock domains is started.

Bit 0 – SWRST: Software Reset Synchronization Status
This bit is cleared when the synchronization of CTRLA.SWRST bit between the clock domains is complete.

This bit is set when the synchronization of CTRLA.SWRST bit between the clock domains is started.

I/O Multiplexing and Considerations

30.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

30.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Pin Controller (PORT).

Related Links

PORT - I/O Pin Controller

30.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

Related Links

PM – Power Manager

30.5.3 Clocks

The TC bus clock (CLK_TCx_APB, where x represents the specific TC instance number) can be enabled and disabled in the Power Manager, and the default state of CLK_TCx_APB can be found in the *Peripheral Clock Masking* section in “PM – Power Manager”.

The different TC instances are paired, even and odd, starting from TC3, and use the same generic clock, GCLK_TCx. This means that the TC instances in a TC pair cannot be set up to use different GCLK_TCx clocks.

This generic clock is asynchronous to the user interface clock (CLK_TCx_APB). Due to this asynchronicity, accessing certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

Peripheral Clock Masking

30.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller

30.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

- Enable bit in the Control A register (CTRLA.ENABLE)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

The following registers are synchronized when written:

- Control B Clear register (CTRLBCLR)
- Control B Set register (CTRLBSET)
- Control C register (CTRLC)
- Count Value register (COUNT)
- Period Value register (PERIOD)
- Compare/Capture Value registers (CCx)

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

The following registers are synchronized when read:

- Control B Clear register (CTRLBCLR)
- Control B Set register (CTRLBSET)
- Control C register (CTRLC)
- Count Value register (COUNT)
- Period Value register (PERIOD)
- Compare/Capture Value registers (CCx)

Required read-synchronization is denoted by the "Read-Synchronized" property in the register description.

Related Links

Register Synchronization

30.7 Register Summary

Table 30-4. Register Summary – 8-bit Mode

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0		WAVEGEN[1:0]			MODE[1:0]		ENABLE	SWRST
0x01		15:8			PRESCSYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
0x02	READREQ	7:0				ADDR[4:0]				
0x03		15:8	RREQ	RCONT						
0x04	CTRLBCLR	7:0	CMD[1:0]					ONESHOT		DIR
0x05	CTRLBSET	7:0	CMD[1:0]					ONESHOT		DIR
0x06	CTRLC	7:0			CPTEN1	CPTEN0			INVEN1	INVEN0
0x07	Reserved									
0x08	DBGCTRL	7:0								DBGRUN
0x09	Reserved									
0x0A	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
0x0B		15:8			MCEO1	MCEO0				OVFEO
0x0C	INTENCLR	7:0			MC1	MC0	SYNCRDY		ERR	OVF
0x0D	INTENSET	7:0			MC1	MC0	SYNCRDY		ERR	OVF
0x0E	INTFLAG	7:0			MC1	MC0	SYNCRDY		ERR	OVF

Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – COUNT[7:0]: Counter Value
These bits contain the current counter value.

30.8.12.2 Counter Value, 16-bit Mode

Name: COUNT
Offset: 0x10
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0]: Counter Value
These bits contain the current counter value.

30.8.12.3 Counter Value, 32-bit Mode

Name: COUNT
Offset: 0x10
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

This bit is set when the synchronization of Compare/Capture Channel x register between clock domains is started.

CCx bit is available only for existing Compare/Capture Channels. For details on CC channels number, refer to each TCC feature list.

This bit is set when the synchronization of CCx register between clock domains is started.

Bit 7 – PER: PER Synchronization Busy
This bit is cleared when the synchronization of PER register between the clock domains is complete.

This bit is set when the synchronization of PER register between clock domains is started.

Bit 6 – WAVE: WAVE Synchronization Busy
This bit is cleared when the synchronization of WAVE register between the clock domains is complete.

This bit is set when the synchronization of WAVE register between clock domains is started.

Bit 5 – PATT: PATT Synchronization Busy
This bit is cleared when the synchronization of PATTERN register between the clock domains is complete.

This bit is set when the synchronization of PATTERN register between clock domains is started.

Bit 4 – COUNT: COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT register between the clock domains is complete.

This bit is set when the synchronization of COUNT register between clock domains is started.

Bit 3 – STATUS: STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS register between the clock domains is complete.

This bit is set when the synchronization of STATUS register between clock domains is started.

Bit 2 – CTRLB: CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB register between the clock domains is complete.

This bit is set when the synchronization of CTRLB register between clock domains is started.

Bit 1 – ENABLE: ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST: SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

31.8.5 Fault Control A and B

Name: FCTRLA, FCTRLB
Offset: 0x0C + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Value	Name	Description
0x0	START	Blanking applied from start of the Ramp period
0x1	RISE	Blanking applied from rising edge of the waveform output
0x2	FALL	Blanking applied from falling edge of the waveform output
0x3	BOTH	Blanking applied from each toggle of the waveform output

Bit 4 – QUAL: Recoverable Fault n Qualification
Setting this bit enables the recoverable Fault n input qualification.

Value	Description
0	The recoverable Fault n input is not disabled on CMPx value condition.
1	The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0).

Bit 3 – KEEP: Recoverable Fault n Keep
Setting this bit enables the Fault n keep action.

Value	Description
0	The Fault n state is released as soon as the recoverable Fault n is released.
1	The Fault n state is released at the end of TCC cycle.

Bits 1:0 – SRC[1:0]: Recoverable Fault n Source
These bits select the TCC event input for recoverable Fault n.

Event system channel connected to MCEx event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

Value	Name	Description
0x0	DISABLE	Fault input disabled
0x1	ENABLE	MCEx (x=0,1) event input
0x2	INVERT	Inverted MCEx (x=0,1) event input
0x3	ALTFAULT	Alternate fault (A or B) state at the end of the previous period.

31.8.6 Waveform Extension Control

Name: WEXCTRL
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	DTHS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DTLS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Offset: 0x08
Reset: 0xxxxxxxx
Property: NA

Bit	15	14	13	12	11	10	9	8
		VARIABLE[10:4]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VARIABLE[3:0]				SUBPID[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	x	0	0	0	x

Bits 14:4 – VARIABLE[10:0]: Variable field send with extended token
These bits define the VARIABLE field of a received extended token. These bits are updated when the USB has answered by an handshake token ACK to a LPM transaction. See Section 2.1.1 Protocol Extension Token in the reference document “ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum”.

To support the USB2.0 Link Power Management addition the VARIABLE field should be read as described below.

VARIABLES	Description
VARIABLE[3:0]	bLinkState (1)
VARIABLE[7:4]	BESL (2)
VARIABLE[8]	bRemoteWake (1)
VARIABLE[10:9]	Reserved

1. For a definition of LPM Token bRemoteWake and bLinkState fields, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum".
2. For a definition of LPM Token BESL field, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum" and "Table X-X1 in Errata for ECN USB 2.0 Link Power Management.

Bits 3:0 – SUBPID[3:0]: SUBPID field send with extended token
These bits define the SUBPID field of a received extended token. These bits are updated when the USB has answered by an handshake token ACK to a LPM transaction. See Section 2.1.1 Protocol Extension Token in the reference document “ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum”.

32.8.4.5 Device Status Bank

Name: STATUS_BK
Offset: 0x0A & 0x1A
Reset: 0xxxxxxxx
Property: NA

32.8.5.4 Host Frame Number

Name: FNUM
Offset: 0x10
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
			FNUM[10:5]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FNUM[4:0]							
Access	R/W	R/W	R/W	R/W	R/W			
Reset	0	0	0	0	0			

Bits 13:3 – FNUM[10:0]: Frame Number
These bits contains the current SOF number.

These bits can be written by software to initialize a new frame number value. In this case, at the next SOF, the FNUM field takes its new value.

As the FNUM register lies across two consecutive byte addresses, writing byte-wise (8-bits) to the FNUM register may produce incorrect frame number generation. It is recommended to write FNUM register word-wise (32-bits) or half-word-wise (16-bits).

32.8.5.5 Host Frame Length

Name: FLENHIGH
Offset: 0x12
Reset: 0x00
Property: Read-Only

Bit	7	6	5	4	3	2	1	0
	FLENHIGH[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – FLENHIGH[7:0]: Frame Length
These bits contains the 8 high-order bits of the internal frame counter.

Table 32-9. Counter Description vs. Speed

Host Register STATUS.SPEED	Description
Full Speed	With a USB clock running at 12MHz, counter length is 12000 to ensure a SOF generation every 1 ms.

Name	Description	Mode	VDD=1.8V			VDD=3.3V			Units
			Min.	Typ.	Max	Min.	Typ.	Max.	
t_{PDM2RS}	Data input setup time	Master mode PDM2 Right	30.5			20.9			ns
t_{PDM2RH}	Data input hold time	Master mode PDM2 Right	-6.7			-6.7			ns

Table 37-66. 2S Timing Characteristics and Requirements (Device Variant B and C)

Name	Description	Mode	VDD=1.8V			VDD=3.3V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{M_MCKOR}	I2S MCK rise time(3)	Master mode / Capacitive load CL = 15 pF			9.2			4.7	ns
t_{M_MCKOF}	I2S MCK fall time(3)	Master mode / Capacitive load CL = 15 pF			11.6			5.4	ns
d_{M_MCKO}	I2S MCK duty cycle	Master mode	47.1		50	47.3		50	%
d_{M_MCKI}	I2S MCK duty cycle	Master mode, pin is input (1b)		50			50		%
t_{M_SCKOR}	I2S SCK rise time(3)	Master mode / Capacitive load CL = 15 pF			9			4.6	ns
t_{M_SCKOF}	I2S SCK fall time(3)	Master mode / Capacitive load CL = 15 pF			9.7			4.6	ns
d_{M_SCKO}	I2S SCK duty cycle	Master mode	47		50	47.2		50	%
f_{M_SCKO}, 1/ t_{M_SCKO}	I2S SCK frequency	Master mode, Supposing external device response delay is 30ns			7.8			9.2	MHz
f_{S_SCKI}, 1/ t_{S_SCKI}	I2S SCK frequency	Slave mode, Supposing external device response delay is 30ns			12.8			13	MHz
d_{S_SCKO}	I2S SCK duty cycle	Slave mode		50			50		%
t_{M_FSOV}	FS valid time	Master mode			2.4			1.9	ns
t_{M_FSOH}	FS hold time	Master mode	-0.1			-0.1			ns
t_{S_FSIS}	FS setup time	Slave mode	6			5.3			ns
t_{S_FSIH}	FS hold time	Slave mode	0			0			ns
t_{M_SDIS}	Data input setup time	Master mode	36			25.9			ns

Table 39-1. Power Supply Connections, V_{DDCORE} From Internal Regulator

Signal Name	Recommended Pin Connection	Description
V_{DDIO}	1.62V - 3.63V Decoupling/filtering capacitors 100nF(1)(2) and 10µF(1) Decoupling/filtering inductor 10µH(1)(3)	Digital supply voltage
V_{DDANA}	1.62V - 3.63V Decoupling/filtering capacitors 100nF(1)(2) and 10µF(1) Ferrite bead(4) prevents the V_{DD} noise interfering the V_{DDANA}	Analog supply voltage
V_{DDCORE}	1.6V to 1.8V Decoupling/filtering capacitor 1µF(1)(2)	Core supply voltage / external decoupling pin
GND		Ground
GND_{ANA}		Ground for the analog power domain

Note:

1. These values are only given as typical examples.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group, low ESR caps should be used for better decoupling.
3. An inductor should be added between the external power and the V_{DD} for power filtering.
4. Ferrite bead has better filtering performance than the common inductor at high frequencies. It can be added between V_{DD} and V_{DDANA} for preventing digital noise from entering the analog power domain. The bead should provide enough impedance (e.g. 50Ω at 20MHz and 220Ω at 100MHz) for separating the digital power from the analog power domain. Make sure to select a ferrite bead designed for filtering applications with a low DC resistance to avoid a large voltage drop across the ferrite bead.

39.3 External Analog Reference Connections

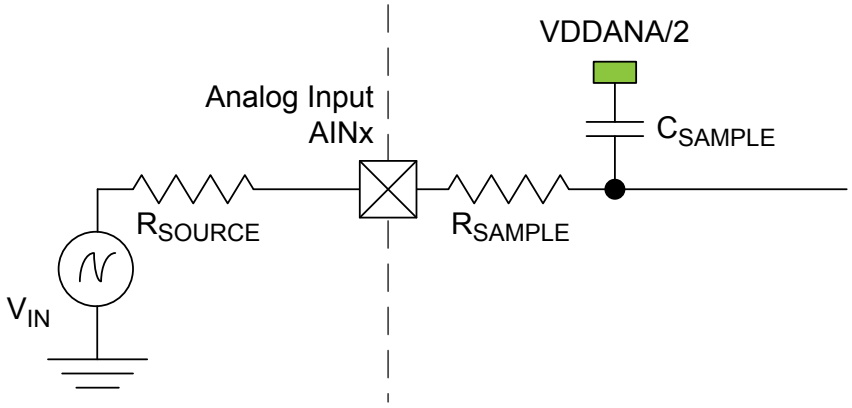
The following schematic checklist is only necessary if the application is using one or more of the external analog references. If the internal references are used instead, the following circuits are not necessary.

Errata reference: 13574
Fix/Workaround:
Write CTRLB.ACKACT to 0 using the following sequence:
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
Write CTRLB.ACKACT to 1 using the following sequence:
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
// Re-enable interrupts if applicable.
Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.
When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit position.
Code replacements examples:
Current:
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
Change to:
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
// Re-enable interrupts if applicable.
Current:
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
Change to:
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
Current:
/* ACK or NACK address */
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
Change to:
// CMD=0x3 clears all interrupts, so to keep the result similar,
// PREC is cleared if it was set.
if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;

15 – The SYSTICK calibration value is incorrect.
Errata reference: 14154
Fix/Workaround:

capacitor (C_{SAMPLE}). In addition, the source resistance (R_{SOURCE}) must be taken into account when calculating the required sample and hold time. The next figure shows the ADC input channel equivalent circuit.

Figure 44-3. ADC Input



To achieve n bits of accuracy, the C_{SAMPLE} capacitor must be charged at least to a voltage of

$$V_{CSAMPLE} \geq V_{IN} \times \left(1 + -2^{-(n+1)}\right)$$

The minimum sampling time $t_{SAMPLEHOLD}$ for a given R_{SOURCE}can be found using this formula:

$$t_{SAMPLEHOLD} \geq \left(R_{SAMPLE} + R_{SOURCE}\right) \times \left(C_{SAMPLE}\right) \times (n+1) \times \ln(2)$$

for a 12 bits accuracy: $t_{SAMPLEHOLD} \geq \left(R_{SAMPLE} + R_{SOURCE}\right) \times \left(C_{SAMPLE}\right) \times 9.02$

where

$$t_{SAMPLEHOLD} = \frac{1}{2 \times f_{ADC}}$$

44.6.5 Digital to Analog Converter (DAC) Characteristics

Table 44-19. Operating Conditions(1)(Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDANA}	Analog supply voltage		1.62	-	3.63	V
AV_{REF}	External reference voltage		1.0	-	V_{DDANA}-0.6	V
	Internal reference voltage 1		-	1	-	V
	Internal reference voltage 2		-	V_{DDANA}	-	V
	Linear output voltage range		0.05	-	V_{DDANA}-0.05	V
	Minimum resistive load		5	-	-	kΩ
	Maximum capacitance load		-	-	100	pF
I_{DD}	DC supply current(2)	Voltage pump disabled	-	160	242	µA

44.8.4 32.768kHz Internal oscillator (OSC32K) Characteristics

Table 44-42. 32kHz RC Oscillator Characteristics (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 32.768kHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	28.508	32.768	35.389	kHz
		Calibrated against a 32.768kHz reference at 25°C, at V_{DD}=3.3V	32.276	32.768	33.260	
		Calibrated against a 32.768kHz reference at 25°C, over [1.62, 3.63]V	31.457	32.768	34.079	
I_{OSC32K}	Current consumption		-	0.79	1.80	µA
$t_{STARTUP}$	Start-up time		-	1	2	cycle
Duty	Duty Cycle		-	50	-	%

Table 44-43. 32kHz RC Oscillator Characteristics (Device Variant B)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 32.768kHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	28.508	32.768	35.389	kHz
		Calibrated against a 32.768kHz reference at 25°C, at V_{DD}=3.3V	32.276	32.768	33.260	
		Calibrated against a 32.768kHz reference at 25°C, over [1.62, 3.63]V	31.457	32.768	34.079	
I_{OSC32K}	Current consumption		-	0.67	2.80	µA
$t_{STARTUP}$	Start-up time		-	1	2	cycle
Duty	Duty Cycle		-	50	-	%

44.8.5 Ultra Low Power Internal 32kHz RC Oscillator (OSCULP32K) Characteristics

Table 44-44. Ultra Low Power Internal 32kHz RC Oscillator Characteristics (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output frequency	Calibrated against a 32.768kHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	25.559	32.768	40.305	kHz
		Calibrated against a 32.768kHz reference at 25°C, at V_{DD}=3.3V	31.293	32.768	34.570	
		Calibrated against a 32.768kHz reference at 25°C, over [1.62, 3.63]V	31.293	32.768	34.570	
$i_{OSCULP32K}$(1)(2)			-	-	180	nA