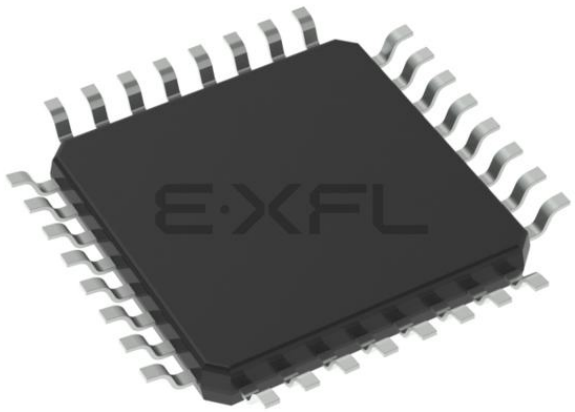

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-TQFP |
| Supplier Device Package | 32-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e16b-au |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 6 – EIC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 5 – RTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 4 – WDT:**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – GCLK**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – SYSCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

**Bits 31:0 – END[31:0]: End Marker**
Indicates the end of the CoreSight ROM table entries.

### 13.13.13 CoreSight ROM Table Memory Type

**Name:** MEMTYPE
**Offset:** 0x1FCC
**Reset:** 0x0000000X
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SMEMP |
| Access | | | | | | | | R |
| Reset | | | | | | | | x |

**Bit 0 – SMEMP: System Memory Present**
This bit indicates whether system memory is present on the bus that connects to the ROM table.

This bit is set at power-up if the device is not protected, indicating that the system memory is accessible from a debug adapter.

This bit is cleared at power-up if the device is protected, indicating that the system memory is not accessible from a debug adapter.

### 13.13.14 Peripheral Identification 4

**Name:** PID4
**Offset:** 0x1FD0
**Reset:** 0x00000000
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

**Bit 17 – AC: AC APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the AC is stopped. |
| 1 | The APBC clock for the AC is enabled. |

**Bit 16 – ADC: ADC APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the ADC is stopped. |
| 1 | The APBC clock for the ADC is enabled. |

**Bit 15 – TC7: TC7 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TC7 is stopped. |
| 1 | The APBC clock for the TC7 is enabled. |

**Bit 14 – TC6: TC6 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TC6 is stopped. |
| 1 | The APBC clock for the TC6 is enabled. |

**Bit 13 – TC5: TC5 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TC5 is stopped. |
| 1 | The APBC clock for the TC5 is enabled. |

**Bit 12 – TC4: TC4 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TC4 is stopped. |
| 1 | The APBC clock for the TC4 is enabled. |

**Bit 11 – TC3: TC3 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TC3 is stopped. |
| 1 | The APBC clock for the TC3 is enabled. |

**Bit 10 – TCC2: TCC2 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TCC2 is stopped. |
| 1 | The APBC clock for the TCC2 is enabled. |

**Bit 9 – TCC1: TCC1 APB Clock Enable**

| Value | Description |
|---|---|
| 0 | The APBC clock for the TCC1 is stopped. |
| 1 | The APBC clock for the TCC1 is enabled. |

3. Start DFLL close loop

This procedure will reduce DFLL Lock time to DFLL Fine lock time.

**Related Links**

GCLK - Generic Clock Controller

NVM Software Calibration Area Mapping

#### Frequency Locking

The locking of the frequency in closed-loop mode is divided into two stages. In the first, coarse stage, the control logic quickly finds the correct value for DFLLVAL.COARSE and sets the output frequency to a value close to the correct frequency. On coarse lock, the DFLL Locked on Coarse Value bit (PCLKSR.DFLLLOCKC) in the Power and Clocks Status register will be set.

In the second, fine stage, the control logic tunes the value in DFLLVAL.FINE so that the output frequency is very close to the desired frequency. On fine lock, the DFLL Locked on Fine Value bit (PCLKSR.DFLLLOCKF) in the Power and Clocks Status register will be set.

Interrupts are generated by both PCLKSR.DFLLLOCKC and PCLKSR.DFLLLOCKF if INTENSET.DFLLOCKC or INTENSET.DFLLOCKF are written to one.

CLK_DFLL48M is ready to be used when the DFLL Ready bit (PCLKSR.DFLLRDY) in the Power and Clocks Status register is set, but the accuracy of the output frequency depends on which locks are set. For lock times, refer to the *Electrical Characteristics*.

**Related Links**

Electrical Characteristics

#### Frequency Error Measurement

The ratio between CLK_DFLL48M_REF and CLK48M_DFLL is measured automatically when the DFLL48M is in closed-loop mode. The difference between this ratio and the value in DFLLMUL.MUL is stored in the DFLL Multiplication Ratio Difference bit group(DFLLVAL.DIFF) in the DFLL Value register. The relative error on CLK_DFLL48M compared to the target frequency is calculated as follows:

$$\mathrm{ERROR} = \frac{\mathrm{DIFF}}{\mathrm{MUL}}$$

#### Drift Compensation

If the Stable DFLL Frequency bit (DFLLCTRL.STABLE) in the DFLL Control register is zero, the frequency tuner will automatically compensate for drift in the CLK_DFLL48M without losing either of the locks. This means that DFLLVAL.FINE can change after every measurement of CLK_DFLL48M.

The DFLLVAL.FINE value overflows or underflows can occur in close loop mode when the clock source reference drifts or is unstable. This will set the DFLL Out Of Bounds bit (PCLKSR.DFLLOOB) in the Power and Clocks Status register.

To avoid this error, the reference clock in close loop mode must be stable, an external oscillator is recommended and internal oscillator forbidden. The better choice is to use an XOSC32K.

#### Reference Clock Stop Detection

If CLK_DFLL48M_REF stops or is running at a very low frequency (slower than CLK_DFLL48M/(2 * $MUL_{MAX}$)), the DFLL Reference Clock Stopped bit (PCLKSR.DFLLRCS) in the Power and Clocks Status register will be set. Detecting a stopped reference clock can take a long time, on the order of 217 CLK_DFLL48M cycles. When the reference clock is stopped, the DFLL48M will operate as if in open-loop mode. Closed-loop mode operation will automatically resume if the CLK_DFLL48M_REF is restarted. An interrupt is generated on a zero-to-one transition on PCLKSR.DFLLRCS if the DFLL Reference Clock Stopped bit (INTENSET.DFLLRCS) in the Interrupt Enable Set register is set.

**Bit 7 – DFLLLCKC: DFLL Lock Coarse**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DFLL Lock Coarse bit in the Status register (PCLKSR.DFLLLCKC) and will generate an interrupt request if INTENSET.DFLLLCKC is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the DFLL Lock Coarse interrupt flag.

**Bit 6 – DFLLLCKF: DFLL Lock Fine**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DFLL Lock Fine bit in the Status register (PCLKSR.DFLLLCKF) and will generate an interrupt request if INTENSET.DFLLLCKF is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the DFLL Lock Fine interrupt flag.

**Bit 5 – DFLLOOB: DFLL Out Of Bounds**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DFLL Out Of Bounds bit in the Status register (PCLKSR.DFLLOOB) and will generate an interrupt request if INTENSET.DFLLOOB is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the DFLL Out Of Bounds interrupt flag.

**Bit 4 – DFLLRDY: DFLL Ready**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DFLL Ready bit in the Status register (PCLKSR.DFLLRDY) and will generate an interrupt request if INTENSET.DFLLRDY is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the DFLL Ready interrupt flag.

**Bit 3 – OSC8MRDY: OSC8M Ready**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the OSC8M Ready bit in the Status register (PCLKSR.OSC8MRDY) and will generate an interrupt request if INTENSET.OSC8MRDY is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the OSC8M Ready interrupt flag.

**Bit 2 – OSC32KRDY: OSC32K Ready**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the OSC32K Ready bit in the Status register (PCLKSR.OSC32KRDY) and will generate an interrupt request if INTENSET.OSC32KRDY is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the OSC32K Ready interrupt flag.

**Bit 12 – LBYPASS: Lock Bypass**

| Value | Description |
|---|---|
| 0 | Normal Mode: the CLK_FDPLL96M is turned off when lock signal is low. |
| 1 | Lock Bypass Mode: the CLK_FDPLL96M is always running, lock is irrelevant. |

**Bits 10:8 – LTIME[2:0]: Lock Time**
These bits select Lock Timeout.

| LTIME[2:0] | Name | Description |
|---|---|---|
| 0x0 | DEFAULT | No time-out |
| 0x1-0x3 | | Reserved |
| 0x4 | 8MS | Time-out if no lock within 8 ms |
| 0x5 | 9MS | Time-out if no lock within 9 ms |
| 0x6 | 10MS | Time-out if no lock within 10 ms |
| 0x7 | 11MS | Time-out if no lock within 11 ms |

**Bits 5:4 – REFCLK[1:0]: Reference Clock Selection**
These bits select the CLK_FDPLL96M_REF source.

| REFCLK[1:0] | Name | Description |
|---|---|---|
| 0x0 | XOSC32 | XOSC32 clock reference |
| 0x1 | XOSC | XOSC clock reference |
| 0x2 | GCLK_DPLL | GCLK_DPLL clock reference |
| 0x3 | | Reserved |

**Bit 3 – WUF: Wake Up Fast**

| Value | Description |
|---|---|
| 0 | DPLL CK output is gated until complete startup time and lock time. |
| 1 | DPLL CK output is gated until startup time only. |

**Bit 2 – LPEN: Low-Power Enable**

| Value | Description |
|---|---|
| 0 | The time to digital converter is selected. |
| 1 | The time to digital converter is not selected, this will improve power consumption but increase the output jitter. |

**Bits 1:0 – FILTER[1:0]: Proportional Integral Filter Selection**
These bits select the DPLL filter type.

| FILTER[1:0] | Name | Description |
|---|---|---|
| 0x0 | DEFAULT | Default filter mode |
| 0x1 | LBFILT | Low bandwidth filter |

### 19.8.27 Alarm n Mask - MODE2

**Name:** MASK
**Offset:** 0x1C
**Reset:** 0x00
**Property:** Write-Protected, Write-Synchronized

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | SEL[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 2:0 – SEL[2:0]: Alarm Mask Selection**
These bits define which bit groups of Alarm n are valid.

| SEL[2:0] | Name | Description |
|---|---|---|
| 0x0 | OFF | Alarm Disabled |
| 0x1 | SS | Match seconds only |
| 0x2 | MMSS | Match seconds and minutes only |
| 0x3 | HHMMSS | Match seconds, minutes, and hours only |
| 0x4 | DDHHMMSS | Match seconds, minutes, hours, and days only |
| 0x5 | MMDDHHMMSS | Match seconds, minutes, hours, days, and months only |
| 0x6 | YYMMDDHHMMSS | Match seconds, minutes, hours, days, months, and years |
| 0x7 | | Reserved |

An AHB clock (CLK_DMAC_AHB) is required to clock the DMAC. This clock must be configured and enabled in the power manager before using the DMAC, and the default state of CLK_DMAC_AHB can be found in *Peripheral Clock Masking*.

This bus clock (CLK_DMAC_APB) is always synchronous to the module clock (CLK_DMAC_AHB), but can be divided by a prescaler and may run even when the module clock is turned off.

**Related Links**

Peripheral Clock Masking

### 20.5.4 DMA

Not applicable.

### 20.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using the DMAC interrupt requires the interrupt controller to be configured first.

**Related Links**

Nested Vector Interrupt Controller

### 20.5.6 Events

The events are connected to the event system.

**Related Links**

EVSYS – Event System

### 20.5.7 Debug Operation

When the CPU is halted in debug mode the DMAC will halt normal operation. The DMAC can be forced to continue operation during debugging. Refer to DBGCTRL for details.

### 20.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Pending register (INTPEND)
- Channel ID register (CHID)
- Channel Interrupt Flag Status and Clear register (CHINTFLAG)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

**Related Links**

PAC - Peripheral Access Controller

### 20.5.9 Analog Connections

Not applicable.

## 20.6 Functional Description

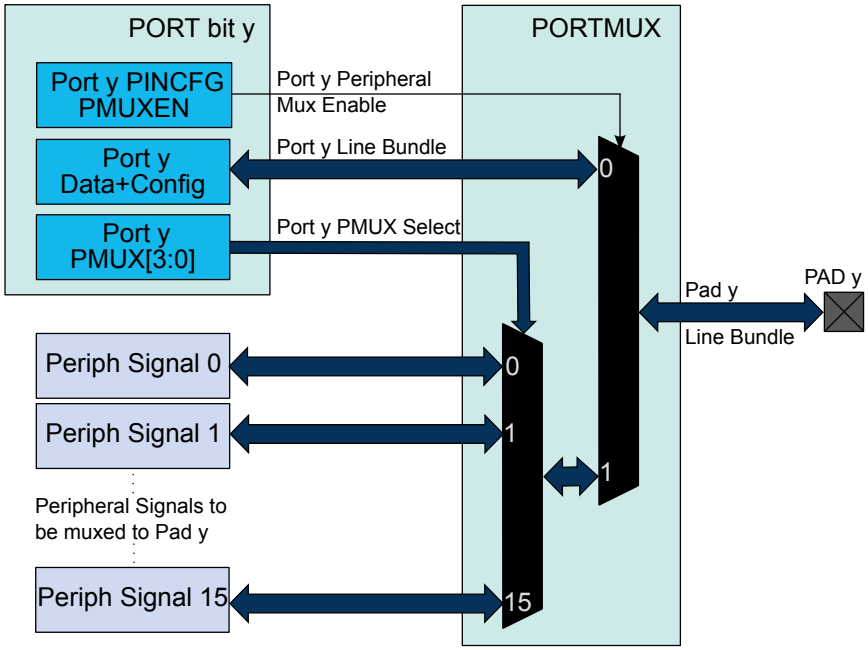
### 20.6.1 Principle of Operation

The DMAC consists of a DMA module and a CRC module.

### 23.6.1 Principle of Operation

Each PORT group of up to 32 pins is controlled by the registers in PORT, as described in the figure. These registers in PORT are duplicated for each PORT group, with increasing base addresses. The number of PORT groups may depend on the package/number of pins.

**Figure 23-3. Overview of the peripheral functions multiplexing**




The I/O pins of the device are controlled by PORT peripheral registers. Each port pin has a corresponding bit in the Data Direction (DIR) and Data Output Value (OUT) registers to enable that pin as an output and to define the output state.

The direction of each pin in a PORT group is configured by the DIR register. If a bit in DIR is set to '1', the corresponding pin is configured as an output pin. If a bit in DIR is set to '0', the corresponding pin is configured as an input pin.

When the direction is set as output, the corresponding bit in the OUT register will set the level of the pin. If bit y in OUT is written to '1', pin y is driven HIGH. If bit y in OUT is written to '0', pin y is driven LOW. Pin configuration can be set by Pin Configuration (PINCFGy) registers, with y=00, 01, ..31 representing the bit position.

The Data Input Value (IN) is set as the input value of a port pin with resynchronization to the PORT clock. To reduce power consumption, these input synchronizers are clocked only when system requires reading the input value. The value of the pin can always be read, whether the pin is configured as input or output. If the Input Enable bit in the Pin Configuration registers (PINCFGy.INEN) is '0', the input value will not be sampled.

In PORT, the Peripheral Multiplexer Enable bit in the PINCFGy register (PINCFGy.PMUXEN) can be written to '1' to enable the connection between peripheral functions and individual I/O pins. The Peripheral Multiplexing n (PMUXn) registers select the peripheral function for the corresponding pin. This will override the connection between the PORT and that I/O pin, and connect the selected peripheral signal to the particular I/O pin instead of the PORT line bundle.

**Bits 12:8 – CHANNEL[4:0]: Channel Event Selection**
These bits are used to select the channel to connect to the event user.

Note that to select channel n, the value (n+1) must be written to the USER.CHANNEL bit group.

| CHANNEL[4:0] | Channel Number |
|---|---|
| 0x0 | No Channel Output Selected |
| 0x1-0xC | Channel n-1 selected |
| 0xD-0xFF | Reserved |

**Bits 4:0 – USER[4:0]: User Multiplexer Selection**
These bits select the event user to be configured with a channel, or the event user to read the channel value from.

**Table 24-2. User Multiplexer Selection**

| USER[7:0] | User Multiplexer | Description | Path Type |
|---|---|---|---|
| 0x00 | DMAC CH0 | Channel 0 | Resynchronized path only |
| 0x01 | DMAC CH1 | Channel 1 | Resynchronized path only |
| 0x02 | DMAC CH2 | Channel 2 | Resynchronized path only |
| 0x03 | DMAC CH3 | Channel 3 | Resynchronized path only |
| 0x04 | TCC0 EV0 | | Asynchronous, synchronous and resynchronized paths |
| 0x05 | TCC0 EV1 | | Asynchronous, synchronous and resynchronized paths |
| 0x06 | TCC0 MC0 | Match/Capture 0 | Asynchronous, synchronous and resynchronized paths |
| 0x07 | TCC0 MC1 | Match/Capture 1 | Asynchronous, synchronous and resynchronized paths |
| 0x08 | TCC0 MC2 | Match/Capture 2 | Asynchronous, synchronous and resynchronized paths |
| 0x09 | TCC0 MC3 | Match/Capture 3 | Asynchronous, synchronous and resynchronized paths |
| 0x0A | TCC1 EV0 | | Asynchronous, synchronous and resynchronized paths |
| 0x0B | TCC1 EV1 | | Asynchronous, synchronous and resynchronized paths |
| 0x0C | TCC1 MC0 | Match/Capture 0 | Asynchronous, synchronous and resynchronized paths |
| 0x0D | TCC1 MC1 | Match/Capture 1 | Asynchronous, synchronous and resynchronized paths |
| 0x0E | TCC2 EV0 | | Asynchronous, synchronous and resynchronized paths |

| Value | Description |
|---|---|
| 0 | The Clock Unit x is disabled. |
| 1 | The Clock Unit x is enabled. |

**Bit 1 – ENABLE: Enable**
Writing a '0' to this bit will disable the module.

Writing a '1' to this bit will enable the module.

| Value | Description |
|---|---|
| 0 | The peripheral is disabled. |
| 1 | The peripheral is enabled. |

**Bit 0 – SWRST: Software Reset**
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers to their initial state, and the peripheral will be disabled.

Writing a '1' to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

| Value | Description |
|---|---|
| 0 | There is no reset operation ongoing. |
| 1 | The reset operation is ongoing. |

### 29.9.2 Clock Unit n Control

**Name:** CLKCTRLn
**Offset:** 0x04 + n*0x04 [n=0..1]
**Reset:** 0x00000000
**Property:** Enable-Protected, PAC Write-Protection

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | MCKOUTINV | SCKOUTINV | FSOUTINV | MCKOUTDIV[4:0] | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | MCKDIV[4:0] | | | | | MCKEN | | MCKSEL |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | SCKSEL | FSINV | | | FSSEL |
| Access | | | | R/W | R/W | | | R/W |
| Reset | | | | 0 | 0 | | | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BITDELAY | FSWIDTH[1:0] | | NBSLOTS[2:0] | | | SLOTSIZE[1:0] | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Waveform Output Generation Operations**

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a waveform generation mode in the Waveform Generation Operation bit in Waveform register (WAVE.WAVEGEN).
2. Optionally invert the waveform output WO[x] by writing the corresponding Waveform Output x Inversion bit in the Driver Control register (DRVCTRL.INVENx).
3. Configure the pins with the I/O Pin Controller. Refer to *PORT - I/O Pin Controller* for details.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TCC_COUNT (see Normal Frequency Operation). An interrupt and/or event can be generated on the same condition if Match/Capture occurs, i.e. INTENSET.MCx and/or EVCTRL.MCEOx is '1'. Both interrupt and event can be generated simultaneously. The same condition generates a DMA request.

There are seven waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

- Normal Frequency (NFRQ)
- Match Frequency (MFRQ)
- Normal Pulse-Width Modulation (NPWM)
- Dual-slope, interrupt/event at TOP (DSTOP)
- Dual-slope, interrupt/event at ZERO (DSBOTTOM)
- Dual-slope, interrupt/event at Top and ZERO (DSBOTH)
- Dual-slope, critical interrupt/event at ZERO (DSCRITICAL)

When using MFRQ configuration, the TOP value is defined by the CC0 register value. For the other waveform operations, the TOP value is defined by the Period (PER) register value.

For dual-slope waveform operations, the update time occurs when the counter reaches ZERO. For the other waveforms generation modes, the update time occurs on counter wraparound, on overflow, underflow, or re-trigger.

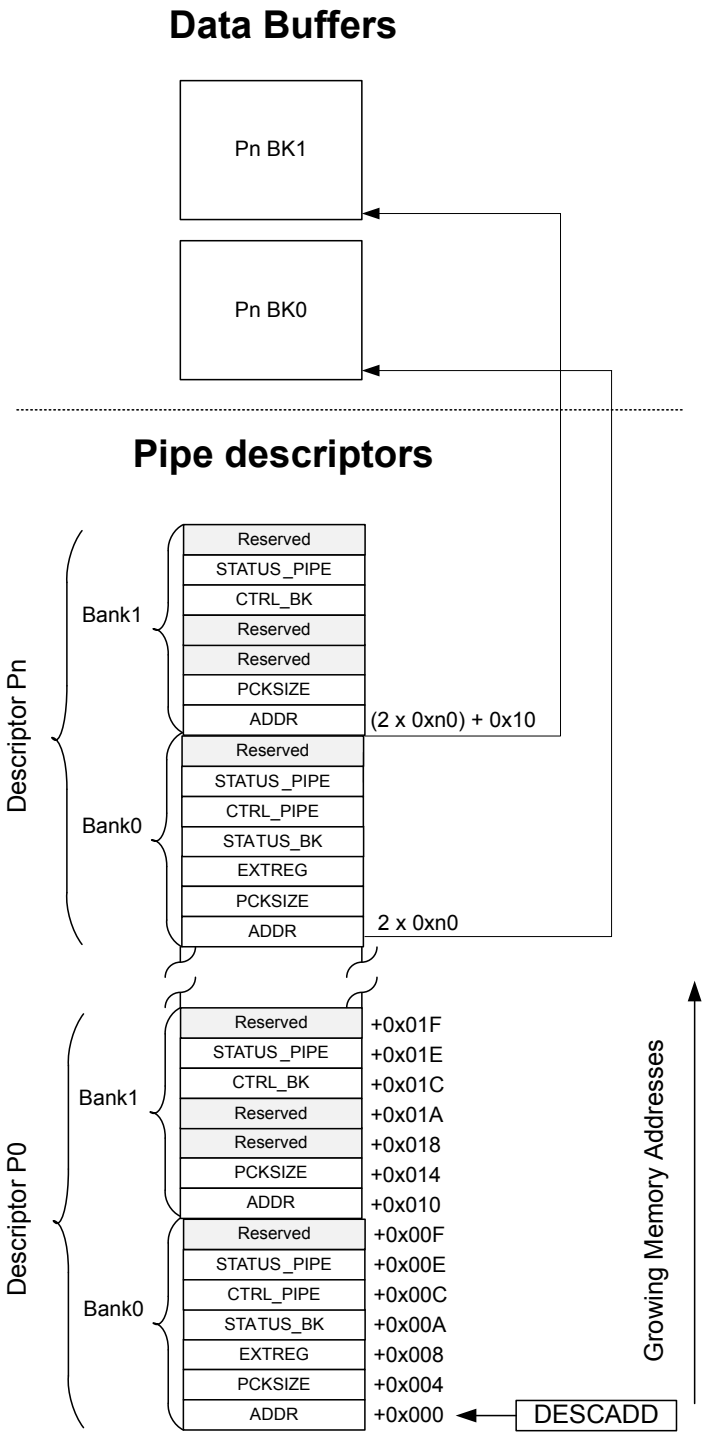
The table below shows the update counter and overflow event/interrupt generation conditions in different operation modes.

**Table 31-2. Counter Update and Overflow Event/interrupt Conditions**

| Name | Operation | TOP | Update | Output Waveform | | OVFIF/Event | |
|---|---|---|---|---|---|---|---|
| | | | | On Match | On Update | Up | Down |
| NFRQ | Normal Frequency | PER | TOP/ ZERO | Toggle | Stable | TOP | ZERO |
| MFRQ | Match Frequency | CC0 | TOP/ ZERO | Toggle | Stable | TOP | ZERO |

### 32.8.7 Host Registers - Pipe RAM

#### 32.8.7.1 Pipe Descriptor Structure



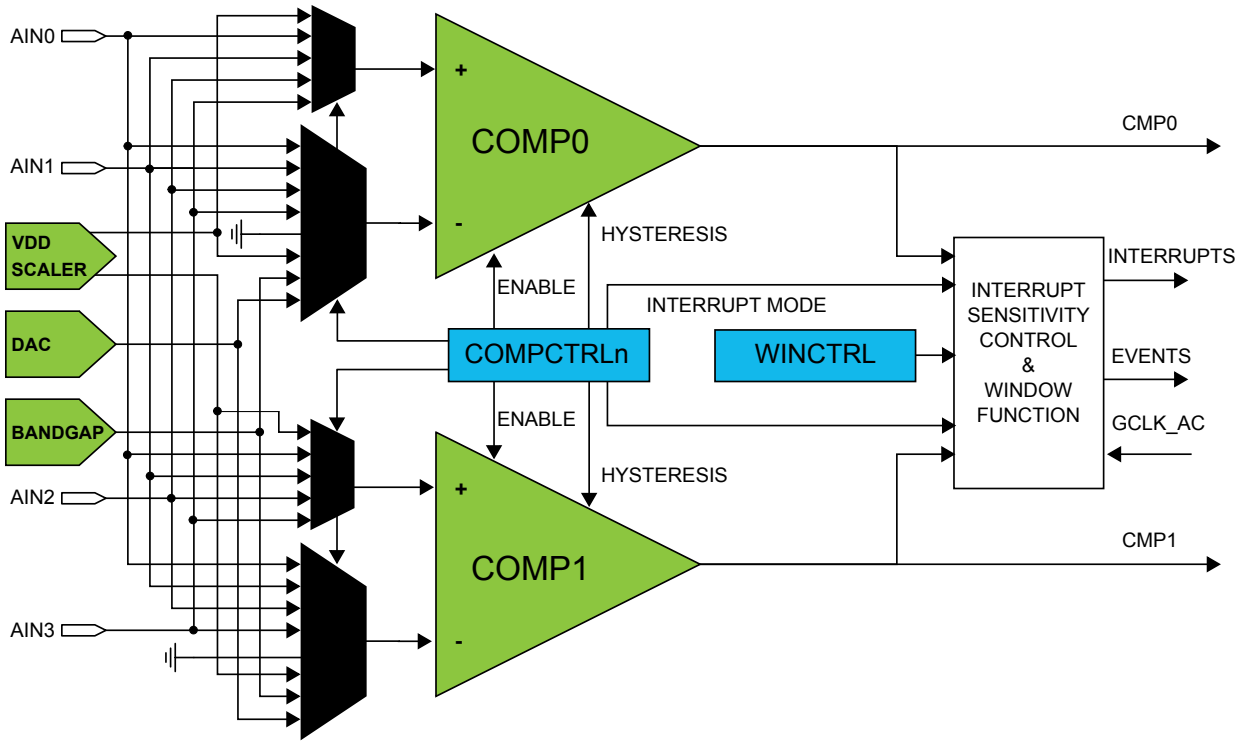

#### 32.8.7.2 Address of the Data Buffer

**Name:** ADDR
**Offset:** 0x00 & 0x10

- Optional digital filter on comparator output
- Low-power option
  - Single-shot support

## 34.3 Block Diagram

**Figure 34-1. Analog Comparator Block Diagram**




## 34.4 Signal Description

| Signal | Description | Type |
|---|---|---|
| AIN[3..0] | Analog input | Comparator inputs |
| CMP[1..0] | Digital output | Comparator outputs |

Refer to *I/O Multiplexing and Considerations* for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

**Related Links**

I/O Multiplexing and Considerations

## 34.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

### 34.5.1 I/O Lines

Using the AC's I/O lines requires the I/O pins to be configured. Refer to *PORT - I/O Pin Controller* for details.

- Control B register (CTRLB)
- Interrupt Flag register (INTFLAG)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

**Related Links**

PAC - Peripheral Access Controller

### 34.5.9 Analog Connections

Each comparator has up to four I/O pins that can be used as analog inputs. Each pair of comparators shares the same four pins. These pins must be configured for analog operation before using them as comparator inputs.

Any internal reference source, such as a bandgap voltage reference, or DAC must be configured and enabled prior to its use as a comparator input.

## 34.6 Functional Description

### 34.6.1 Principle of Operation

Each comparator has one positive input and one negative input. Each positive input may be chosen from a selection of analog input pins. Each negative input may be chosen from a selection of both analog input pins and internal inputs, such as a bandgap voltage reference.

The digital output from the comparator is '1' when the difference between the positive and the negative input voltage is positive, and '0' otherwise.

The individual comparators can be used independently (normal mode) or paired to form a window comparison (window mode).

### 34.6.2 Basic Operation

#### 34.6.2.1 Initialization

Before enabling the AC, the input and output events must be configured in the Event Control register (EVCTRL). These settings cannot be changed while the AC is enabled.

#### 34.6.2.2 Enabling, Disabling and Resetting

The AC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The AC is disabled writing a '0' to CTRLA.ENABLE.

The AC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the AC will be reset to their initial state, and the AC will be disabled. Refer to *CTRLA* for details.

The individual comparators must be also enabled by writing a '1' to the Enable bit in the Comparator x Control registers (COMPCTRLx.ENABLE). However, when the AC is disabled, this will also disable the individual comparators, but will not clear their COMPCTRLx.ENABLE bits.

**Related Links**

CTRLA

| Value | Name | Description |
|---|---|---|
| 0x0 | ABOVE | Interrupt on signal above window |
| 0x1 | INSIDE | Interrupt on signal inside window |
| 0x2 | BELOW | Interrupt on signal below window |
| 0x3 | OUTSIDE | Interrupt on signal outside window |

**Bit 0 – WEN0: Window 0 Mode Enable**

| Value | Description |
|---|---|
| 0 | Window mode is disabled for comparators 0 and 1. |
| 1 | Window mode is enabled for comparators 0 and 1. |

### 34.8.11 Comparator Control n

**Name:** COMPCTRL0, COMPCTRL1
**Offset:** 0x10 + n*0x04 [n=0..1]
**Reset:** 0x00000000
**Property:** PAC Write-Protection, Write-Synchronized

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | FLEN[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | HYST | | OUT[1:0] | |
| Access | | | | | R/W | | R/W | R/W |
| Reset | | | | | 0 | | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | SWAP | | MUXPOS[1:0] | | | MUXNEG[2:0] | | |
| Access | R/W | | R/W | R/W | | R/W | R/W | R/W |
| Reset | 0 | | 0 | 0 | | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | INTSEL[1:0] | | | SPEED[1:0] | | SINGLE | ENABLE |
| Access | | R/W | R/W | | R/W | R/W | R/W | R/W |
| Reset | | 0 | 0 | | 0 | 0 | 0 | 0 |

**Bits 26:24 – FLEN[2:0]: Filter Length**
These bits configure the filtering for comparator n. COMPCTRLn.FLEN can only be written while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

| Value | Name | Description |
|---|---|---|
| 0x0 | OFF | No filtering |
| 0x1 | MAJ3 | 3-bit majority function (2 of 3) |
| 0x2 | MAJ5 | 5-bit majority function (3 of 5) |
| 0x3-0x7 | N/A | Reserved |

**Table 37-20. BOD33 LEVEL Value**

| Symbol | BOD33.LEVEL | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{BOD+}$ | 6 | Hysteresis ON | - | 1.715 | 1.745 | V |
| | 7 | | - | 1.750 | 1.779 | |
| | 39 | | - | 2.84 | 2.92 | |
| | 48 | | - | 3.2 | 3.3 | |
| $V_{BOD-}$ or $V_{BOD}$ | 6 | Hysteresis ON or Hysteresis OFF | 1.62 | 1.64 | 1.67 | |
| | 7 | | 1.64 | 1.675 | 1.71 | |
| | 39 | | 2.72 | 2.77 | 2.81 | |
| | 48 | | 3.0 | 3.07 | 3.2 | |

**Note:** See chapter Memories table *NVM User Row Mapping* for the BOD33 default value settings.

**Table 37-21. BOD33 Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Step size, between adjacent values in BOD33.LEVEL | | - | 34 | - | mV |
| $V_{HYST}$ | $V_{BOD+}$ - $V_{BOD-}$ | Hysteresis ON | 35 | - | 170 | mV |
| $t_{DET}$ | Detection time | Time with $V_{DDANA} < V_{TH}$ necessary to generate a reset signal | - | 0.9(1) | - | µs |
| $I_{BOD33}$ | Current consumption | Continuous mode | 2.9 | 33 | 52.2 | µA |
| | | Sampling mode | - | 23 | 75.5 | |
| $t_{STARTUP}$ | Startup time | | - | 2.2(1) | - | µs |

**Note:** 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

**Related Links**

NVM User Row Mapping

### 37.10.4 Analog-to-Digital (ADC) characteristics

**Table 37-22. Operating Conditions**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| RES | Resolution | | 8 | - | 12 | bits |
| $f_{CLK\_ADC}$ | ADC Clock frequency | | 30 | - | 2100 | kHz |
| | Sample rate(1) | Single shot | 5 | - | 300 | ksps |
| | | Free running | 5 | - | 350 | ksps |
| | Sampling time(1) | | 0.5 | - | - | cycles |

**Figure 37-17. 10 Sensor / PTC_GCLK = 2MHz / FREQ_MODE_HOP**

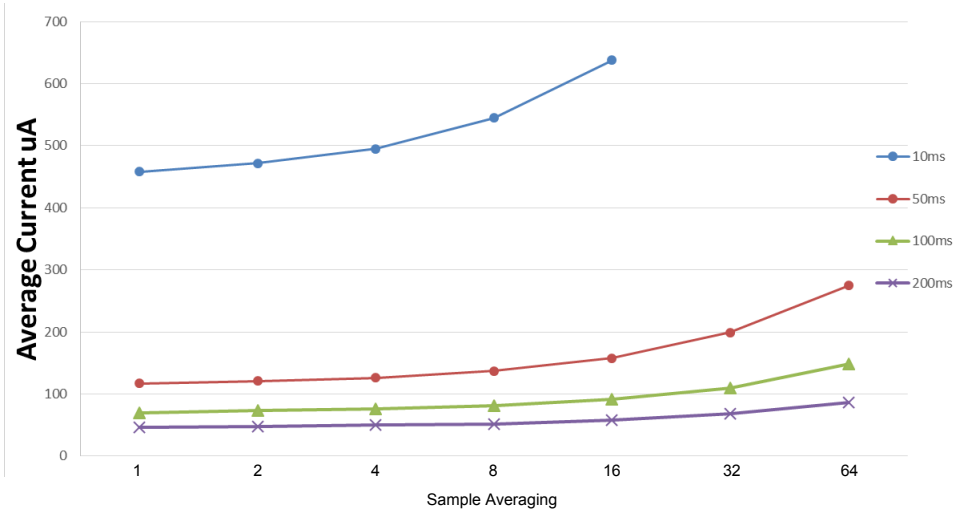
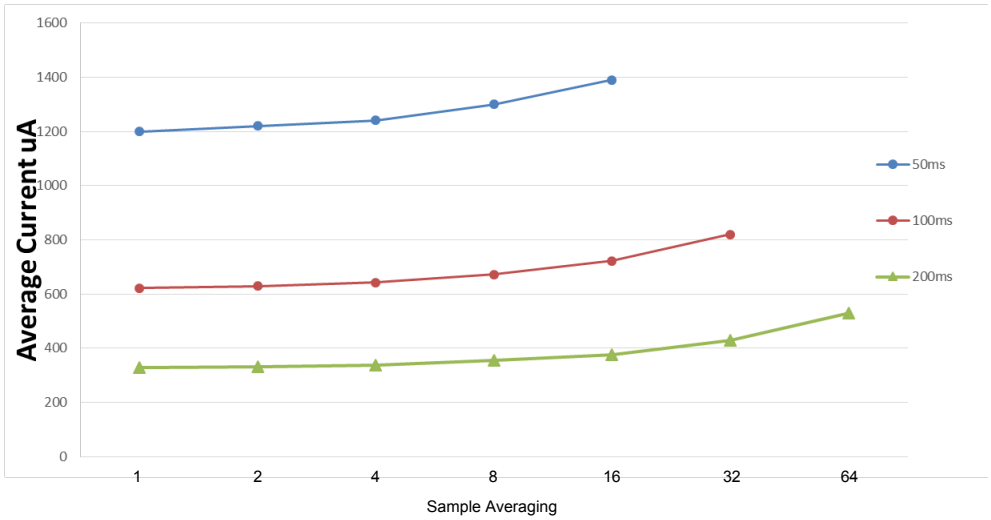



**Figure 37-18. 100 Sensor / PTC_GCLK = 4MHz / FREQ_MODE_NONE**



# 41. Conventions

## 41.1 Numerical Notation

**Table 41-1. Numerical Notation**

| Symbol | Description |
|---|---|
| 165 | Decimal number |
| 0b0101 | Binary number (example 0b0101 = 5 decimal) |
| '0101' | Binary numbers are given without prefix if unambiguous. |
| 0x3B24 | Hexadecimal number |
| X | Represents an unknown or don't care value |
| Z | Represents a high-impedance (floating) state for either a signal or a bus |

## 41.2 Memory Size and Type

**Table 41-2. Memory Size and Bit Rate**

| Symbol | Description |
|---|---|
| KB (kbyte) | kilobyte ($2^{10}$ = 1024) |
| MB (Mbyte) | megabyte ($2^{20}$ = 1024*1024) |
| GB (Gbyte) | gigabyte ($2^{30}$ = 1024*1024*1024) |
| b | bit (binary '0' or '1') |
| B | byte (8 bits) |
| 1kbit/s | 1,000 bit/s rate (not 1,024 bit/s) |
| 1Mbit/s | 1,000,000 bit/s rate |
| 1Gbit/s | 1,000,000,000 bit/s rate |
| word | 32 bit |
| half-word | 16 bit |

## 41.3 Frequency and Time

| Symbol | Description |
|---|---|
| kHz | 1kHz = $10^3$Hz = 1,000Hz |
| KHz | 1KHz = 1,024Hz, 32KHz = 32,768Hz |
| MHz | $10^6$ = 1,000,000Hz |

| I2S - Inter-IC Sound Controller |
| --- |
| Introducing Frame Synch Clock.<br>Signal Description: Added separate tables for Master-, Slave- and Controller mode.<br>Updated description in Debug Operation and Register Access Protection.<br>Updated description in Principle of Operation.<br>Updated description in sub sections of Basic Operation.<br>Updated formula in MCKn Clock Frequency.<br>Updated formulas in Relation Between MCKn, SCKn, and Sampling Frequency fs.<br>Updated description in PDM Reception.<br>Section on MONO removed and information included in Basic Operation.<br>Updated property of Control A (CTRLA) register: Added Write-Synchronized |
| TCC – Timer/Counter for Control Applications |
| Updated description in Principle of Operation.<br>Updated description in sub sections of Basic Operation.<br>Updated description in sub sections of Additional Features.<br>Updated description in Synchronization.<br>Lock Update (LUPD) bit description updated in Control B Clear (CTRLBCLR) register.<br>Compare Channel Buffer x Busy (CCBx) bit description updated in Synchronization Busy (SYNCBUSY) register.<br>Event Control (EVCTRL) register property updated: Removed Enable-Protected.<br>Interrupt Enable Clear (INTENCLR), Interrupt Enable Set (INTENSET) and Interrupt Flag Status and Clear (INTFLAG) registers: Updated bit description of FAULT0, FAULT1, FAULTA and FAULTB.<br>STATUS register bit descriptions updated.<br>Wave Control (WAVE) register property updated: Removed Read-Synchronized.<br>Pattern Buffer (PATTB) register: Updated property and bit description.<br>Waveform Control Buffer (WAVEB) register: Updated property and bit descriptions. |
| USB – Universal Serial Bus |
| Removed figures: Setup Transaction Overview, OUT Single Bank Transaction Overview, IN Single Bank Transaction Overview and USB Host Communication Flow.<br>Updated description and graphics in sub sections of USB Device Operations.<br>Updated description in sub sections of Host Operations.<br>Pad Calibration (PADCAL) register: Access updated.<br>Upgraded bit descriptions.<br>Pipe Descriptor Structure: Updated register reset values. |
| ADC – Analog-to-Digital Converter |