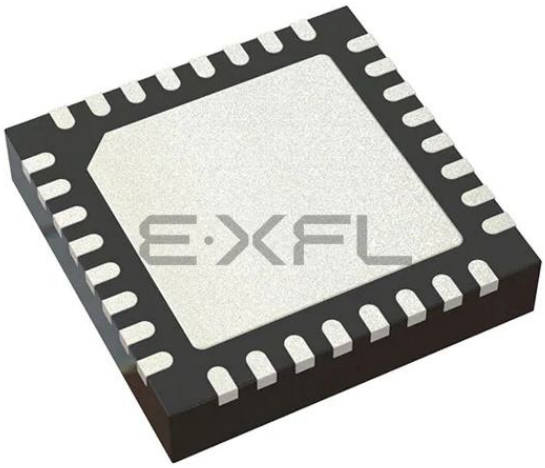

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 32-VFQFN Exposed Pad |
| Supplier Device Package | 32-VQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e16b-mut |

        - Up to four compare channels with optional complementary output
        - Generation of synchronized pulse width modulation (PWM) pattern across port pins
        - Deterministic fault protection, fast decay and configurable dead-time between complementary output
        - Dithering that increase resolution with up to 5 bit and reduce quantization error
    - 32-bit Real Time Counter (RTC) with clock/calendar function
    - Watchdog Timer (WDT)
    - CRC-32 generator
    - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
        - Embedded host and device function
        - Eight endpoints
    - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
        - USART with full-duplex and single-wire half-duplex configuration
        - I2C up to 3.4MHz
        - SPI
        - LIN slave
    - One two-channel Inter-IC Sound ($I^2S$) interface
    - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
        - Differential and single-ended input
        - 1/2x to 16x programmable gain stage
        - Automatic offset and gain error compensation
        - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
    - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
    - Two Analog Comparators (AC) with window compare function
    - Peripheral Touch Controller (PTC)
        - 256-Channel capacitive touch and proximity sensing
- I/O
    - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20
- Packages
    - 64-pin TQFP, QFN, UFBGA
    - 48-pin TQFP, QFN, WLCSP
    - 32-pin TQFP, QFN, WLCSP
- Operating Voltage
    - 1.62V – 3.63V

| Periph. Name | Base Address | IRQ Line | AHB Clock | | APB Clock | | Generic Clock | PAC | | Events | | DMA | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Index | Enabled at Reset | Index | Enabled at Reset | Index | Index | Prot. at Reset | User | Generator | Index | Sleep Walking |
| TC5 | 0x42003400 | 20 | | | 13 | N | 28 | 13 | N | 20: EV | 57: OVF<br>58-59: MC0-1 | 30: OVF<br>31-32: MC0-1 | Y |
| TC6 | 0x42003800 | 21 | | | 14 | N | 29 | 14 | N | 21: EV | 60: OVF<br>61-62: MC0-1 | 33: OVF<br>34-35: MC0-1 | Y |
| TC7 | 0x42003C00 | 22 | | | 15 | N | 29 | 15 | N | 22: EV | 63: OVF<br>64-65: MC0-1 | 36: OVF<br>37-38: MC0-1 | Y |
| ADC | 0x42004000 | 23 | | | 16 | Y | 30 | 16 | N | 23: START<br>24: SYNC | 66: RESRDY<br>67: WINMON | 39: RESRDY | Y |
| AC | 0x42004400 | 24 | | | 17 | N | 31: DIG<br>32: ANA | 17 | N | 25-26: SOC0-1 | 68-69: COMP0-1<br>70: WIN0 | | Y |
| DAC | 0x42004800 | 25 | | | 18 | N | 33 | 18 | N | 27: START | 71: EMPTY | 40: EMPTY | Y |
| PTC | 0x42004C00 | 26 | | | 19 | N | 34 | 19 | N | 28: STCONV | 72: EOC<br>73: WCOMP | | |
| I2S | 0x42005000 | 27 | | | 20 | N | 35-36 | 20 | N | | | 41:42: RX<br>43:44: TX | Y |

command is ongoing, other commands are discarded until the current operation is completed. Hence, the user must wait for the STATUSA.DONE bit to be set prior to issuing another one.

### 13.11.2 Basic Operation

#### 13.11.2.1 Initialization

The module is enabled by enabling its clocks. For more details, refer to Clocks. The DSU registers can be PAC write-protected.

**Related Links**

PAC - Peripheral Access Controller

#### 13.11.2.2 Operation From a Debug Adapter

Debug adapters should access the DSU registers in the external address range 0x100 – 0x2000. If the device is protected by the NVMCTRL security bit, accessing the first 0x100 bytes causes the system to return an error. Refer to Intellectual Property Protection.

**Related Links**

NVMCTRL – Non-Volatile Memory Controller

Security Bit

#### 13.11.2.3 Operation From the CPU

There are no restrictions when accessing DSU registers from the CPU. However, the user should access DSU registers in the internal address range (0x0 – 0x100) to avoid external security restrictions. Refer to Intellectual Property Protection.

### 13.11.3 32-bit Cyclic Redundancy Check CRC32

The DSU unit provides support for calculating a cyclic redundancy check (CRC32) value for a memory area (including Flash and AHB RAM).

When the CRC32 command is issued from:

- The internal range, the CRC32 can be operated at any memory location
- The external range, the CRC32 operation is restricted; DATA, ADDR, and LENGTH values are forced (see below)

**Table 13-3. AMOD Bit Descriptions when Operating CRC32**

| AMOD[1:0] | Short name | External range restrictions |
|---|---|---|
| 0 | ARRAY | CRC32 is restricted to the full Flash array area (EEPROM emulation area not included) DATA forced to 0xFFFFFFFF before calculation (no seed) |
| 1 | EEPROM | CRC32 of the whole EEPROM emulation area DATA forced to 0xFFFFFFFF before calculation (no seed) |
| 2-3 | Reserved | |

The algorithm employed is the industry standard CRC32 algorithm using the generator polynomial 0xEDB88320 (reversed representation).

#### 13.11.3.1 Starting CRC32 Calculation

CRC32 calculation for a memory range is started after writing the start address into the Address register (ADDR) and the size of the memory range into the Length register (LENGTH). Both must be word-aligned.

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | REVISION[3:0] | | | | JEPU | JEPIDCH[2:0] | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

**Bits 7:4 – REVISION[3:0]: Revision Number**
Revision of the peripheral. Starts at 0x0 and increments by one at both major and minor revisions.

**Bit 3 – JEPU: JEP-106 Identity Code is used**
This bit will always return one when read, indicating that JEP-106 code is used.

**Bits 2:0 – JEPIDCH[2:0]: JEP-106 Identity Code High**
These bits will always return 0x1 when read, indicating an Atmel device (Atmel JEP-106 identity code is 0x1F).

### 13.13.18 Peripheral Identification 3

**Name:** PID3
**Offset:** 0x1FEC
**Reset:** 0x00000000
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Value | Description |
|---|---|
| 0 | The XOSC32K Ready interrupt is disabled. |
| 1 | The XOSC32K Ready interrupt is enabled, and an interrupt request will be generated when the XOSC32K Ready Interrupt flag is set. |

**Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable**
Writing a zero to this bit has no effect.

Writing a one to this bit will set the XOSC Ready Interrupt Enable bit, which enables the XOSC Ready interrupt.

| Value | Description |
|---|---|
| 0 | The XOSC Ready interrupt is disabled. |
| 1 | The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the XOSC Ready Interrupt flag is set. |

### 17.8.3 Interrupt Flag Status and Clear

**Note:** Depending on the fuse settings, various bits of the INTFLAG register can be set to one at startup. Therefore the user should clear those bits before using the corresponding interrupts.

**Name:** INTFLAG
**Offset:** 0x08
**Reset:** 0x00000000
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | DPLLLTO | DPLLLCKF |
| Access | R | R | R | R | R | R | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | DPLLLCKR | | | | B33SRDY | BOD33DET | BOD33RDY | DFLLRCS |
| Access | R/W | R | R | R | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | DFLLLCKC | DFLLLCKF | DFLLOOB | DFLLRDY | OSC8MRDY | OSC32KRDY | XOSC32KRDY | XOSCRDY |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 17 – DPLLLTO: DPLL Lock Timeout**
This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DPLL Lock Timeout bit in the Status register (PCLKSR.DPLLLTO) and will generate an interrupt request if INTENSET.DPLLLTO is one.

Writing a zero to this bit has no effect.

12 – December

**Bits 21:17 – DAY[4:0]: Day**
Day starts at 1 and ends at 28, 29, 30 or 31, depending on the month and year.

**Bits 16:12 – HOUR[4:0]: Hour**
When CTRL.CLKREP is zero, the Hour bit group is in 24-hour format, with values 0-23. When CTRL.CLKREP is one, HOUR[3:0] has values 1-12 and HOUR[4] represents AM (0) or PM (1).

**Table 19-4. Hour**

| HOUR[4:0] | CLOCK.HOUR[4] | CLOCK.HOUR[3:0] | Description |
|---|---|---|---|
| 0 | 0x00 - 0x17 | | Hour (0 - 23) |
| | 0x18 - 0x1F | | Reserved |
| 1 | 0 | 0x0 | Reserved |
| | | 0x1 - 0xC | AM Hour (1 - 12) |
| | | 0xD - 0xF | Reserved |
| | 1 | 0x0 | Reserved |
| | | 0x1 - 0xC | PM Hour (1 - 12) |
| | | 0xF - 0xF | Reserved |

**Bits 11:6 – MINUTE[5:0]: Minute**
0 – 59.

**Bits 5:0 – SECOND[5:0]: Second**
0– 59.

### 19.8.23 Counter Period - MODE1

**Name:** PER
**Offset:** 0x14
**Reset:** 0x0000
**Property:** Write-Protected, Write-Synchronized

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | PER[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PER[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 15:0 – PER[15:0]: Counter Period**
These bits define the value of the 16-bit RTC period.

**Property:** PAC Write-Protection

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DBGRUN |
| Access | | | | | | | | R/W |
| Reset | | | | | | | | 0 |

**Bit 0 – DBGRUN: Debug Run**
This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

| Value | Description |
|---|---|
| 0 | The DMAC is halted when the CPU is halted by an external debugger. |
| 1 | The DMAC continues normal operation when the CPU is halted by an external debugger. |

### 20.8.7 Quality of Service Control

**Name:** QOSCTRL
**Offset:** 0x0E
**Reset:** 0x2A
**Property:** PAC Write-Protection

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | DQOS[1:0] | | FQOS[1:0] | | WRBQOS[1:0] | |
| Access | | | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | | 1 | 0 | 1 | 0 | 1 | 0 |

**Bits 5:4 – DQOS[1:0]: Data Transfer Quality of Service**
These bits define the memory priority access during the data transfer operation.

| DQOS[1:0] | Name | Description |
|---|---|---|
| 0x0 | DISABLE | Background (no sensitive operation) |
| 0x1 | LOW | Sensitive Bandwidth |
| 0x2 | MEDIUM | Sensitive Latency |
| 0x3 | HIGH | Critical Latency |

**Bits 3:2 – FQOS[1:0]: Fetch Quality of Service**
These bits define the memory priority access during the fetch operation.

| FQOS[1:0] | Name | Description |
|---|---|---|
| 0x0 | DISABLE | Background (no sensitive operation) |
| 0x1 | LOW | Sensitive Bandwidth |
| 0x2 | MEDIUM | Sensitive Latency |
| 0x3 | HIGH | Critical Latency |

with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN) will set the input pull direction to an internal pull-down.

| Value | Description |
|---|---|
| 0 | The corresponding I/O pin in the PORT group will keep its configuration. |
| 1 | The corresponding I/O pin output is driven low, or the input is connected to an internal pull-down. |

### 23.8.7 Data Output Value Set

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

**Name:** OUTSET
**Offset:** 0x18
**Reset:** 0x00000000
**Property:** PAC Write-Protection

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | OUTSET[31:24] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | OUTSET[23:16] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | OUTSET[15:8] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | OUTSET[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

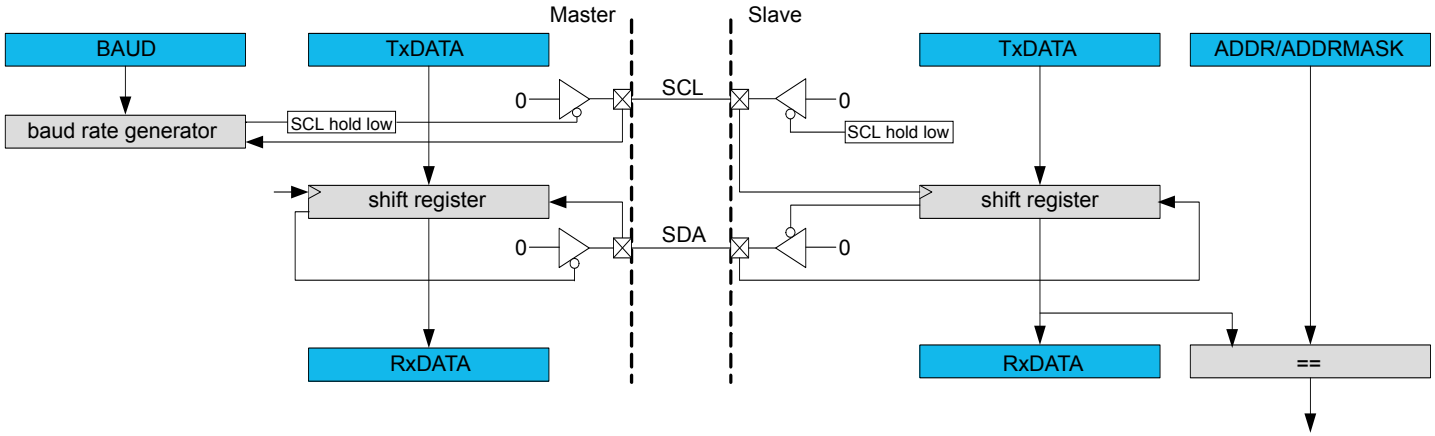
**Bits 31:0 – OUTSET[31:0]: PORT Data Output Value Set**
Writing '0' to a bit has no effect.

Writing '1' to a bit will set the corresponding bit in the OUT register, which sets the output drive level high for I/O pins configured as outputs via the Data Direction register (DIR). For pins configured as inputs via Data Direction register (DIR) with pull enabled via the Pull Enable register (PULLEN), these bits will set the input pull direction to an internal pull-up.

| Value | Description |
|---|---|
| 0 | The corresponding I/O pin in the group will keep its configuration. |
| 1 | The corresponding I/O pin output is driven high, or the input is connected to an internal pull-up. |

## 28.3 Block Diagram

**Figure 28-1. I²C Single-Master Single-Slave Interconnection**




## 28.4 Signal Description

| Signal Name | Type | Description |
|---|---|---|
| PAD[0] | Digital I/O | SDA |
| PAD[1] | Digital I/O | SCL |
| PAD[2] | Digital I/O | SDA_OUT (4-wire) |
| PAD[3] | Digital I/O | SDC_OUT (4-wire) |

One signal can be mapped on several pins.

Not all the pins are I²C pins.

**Related Links**

I/O Multiplexing and Considerations

## 28.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

### 28.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Pin Controller (PORT).

When the SERCOM is used in I²C mode, the SERCOM controls the direction and value of the I/O pins. Both PORT control bits PINCFGn.PULLEN and PINCFGn.DRVSTR are still effective. If the receiver or transmitter is disabled, these pins can be used for other purposes.

**Related Links**

PORT: IO Pin Controller

### 28.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes.

**Bit 7 – ERROR: Error**
This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status bits in the STATUS register. These status bits are LENERR, SEXTTOUT, MEXTTOUT, LOWTOUT, ARBLOST, and BUSERR.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

**Bit 1 – SB: Slave on Bus**
The Slave on Bus flag (SB) is set when a byte is successfully received in master read mode, i.e., no arbitration lost or bus error occurred during the operation. When this flag is set, the master forces the SCL line low, stretching the $I^2C$ clock period. The SCL line will be released and SB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the SB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

**Bit 0 – MB: Master on Bus**
This flag is set when a byte is transmitted in master write mode. The flag is set regardless of the occurrence of a bus error or an arbitration lost condition. MB is also set when arbitration is lost during sending of NACK in master read mode, or when issuing a start condition if the bus state is unknown. When this flag is set and arbitration is not lost, the master forces the SCL line low, stretching the $I^2C$ clock period. The SCL line will be released and MB will be cleared on one of the following actions:

- Writing to ADDR.ADDR
- Writing to DATA.DATA
- Reading DATA.DATA when smart mode is enabled (CTRLB.SMEN)
- Writing a valid command to CTRLB.CMD

Writing '1' to this bit location will clear the MB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

### 28.10.7 Status

**Name:** STATUS
**Offset:** 0x1A
**Reset:** 0x0000
**Property:** Write-Synchronized

In Controller mode, only the Clock generation unit needs to be configured by writing to the CTRLA and CLKCTRLn registers, where parameters such as clock division factors, Number of slots, Slot size, Frame Sync signal, clock enable are selected.

**MCKn Clock Frequency**

When the $I^2S$ is in Master mode, writing a '1' to CLKCTRLn.MCKEN will output GCLK_I2S_n as Master Clock to the MCKn pin. The Master Clock to MCKn pin can be divided by writing to CLKCTRLn.MCKSEL and CLKCTRLn.MCKOUTOUT. The Master Clock (MCKn) frequency is GCLK_I2S_n frequency divided by (MCLKOUTDIV+1).

$$f(\mathrm{MCKn}) = \frac{f(\mathrm{GCLK\_I2S\_}n)}{(\mathrm{MCKOUTDIV}+1)}$$

**SCKn Clock Frequency**

When the Serial Clock (SCKn) is generated from GCLK_I2S_n and both CLKCTRLn.MCKSEL and CLKCTRLn.SCKSEL are zero, the Serial Clock (SCKn) frequency is GCLK_I2S_n frequency divided by (MCKDIV+1).

i.e.

$$f(\mathrm{SCKn}) = \frac{f(\mathrm{GCLK\_I2S\_}n)}{(\mathrm{MCKDIV}+1)}$$

**Relation Between MCKn, SCKn, and Sampling Frequency *fs***

Based on sampling frequency ***fs***, the SCKn frequency requirement can be calculated:

- SCKn frequency: $f_{\mathrm{SCKn}} = fs \times \mathrm{total\_number\_of\_bits\_per\_frame}$,
- Where $\mathrm{total\_number\_of\_bits\_per\_frame} = \mathrm{number\_of\_slots} \times \mathrm{number\_of\_bits\_per\_slots}$.
- The number of slots is selected by writing to the Number of Slots in Frame bit field in the Clock Unit n Control (CLKCTRLn) register: $\mathrm{number\_of\_slots} = \mathrm{NBSLOTS} + 1$.
- The number of bits per slot (8, 16, 24, or 32 bit) is selected by writing to the Slot Size bit field in CLKCTRLn: .
- Consequently, $f_{\mathrm{SCKn}} = 8 \times fs \times (\mathrm{NBSLOTS}+1) \times (\mathrm{SLOTSIZE}+1)$.

The clock frequencies $f_{\mathrm{SCKn}}$ and $f_{\mathrm{MCKn}}$ are derived from the generic clock frequency $f_{\mathrm{GCLK\_I2S\_n}}$ :

- $f_{\mathrm{GCLK\_I2S\_n}} = f_{\mathrm{SCKn}} \times (\mathrm{CLKCTRLn.MCKDIV}+1)$
  $= 8 \times fs \times (\mathrm{NBSLOTS}+1) \times (\mathrm{SLOTSIZE}+1) \times (\mathrm{MCKDIV}+1)$
  , and
- $f_{\mathrm{GCLK\_I2S\_n}} = f_{\mathrm{MCKn}} \times (\mathrm{MCKOUTDIV}+1)$.

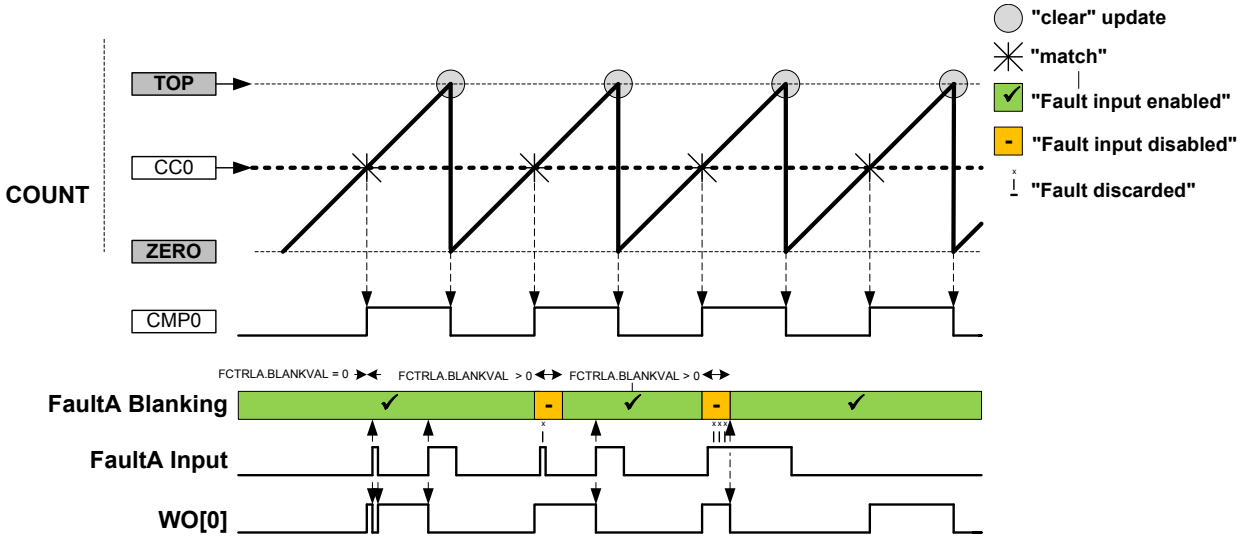
Substituting the right hand sides of the two last equations yields:

$$f_{\mathrm{MCKn}} = \frac{f_{\mathrm{GCLK\_I2S\_n}}}{\mathrm{MCKOUTDIV}+1}$$

$$f_{\mathrm{MCKn}} = \frac{8 \cdot (\mathrm{SLOTSIZE}+1) \cdot (\mathrm{NBSLOTS}+1) \cdot (\mathrm{MCKDIV}+1)}{\mathrm{MCKOUTDIV}+1}$$

If a Master Clock output is not required, the GCLK_I2S generic clock can be configured as SCKn by writing a '0'to CLKCTRLn.MCKDIV. Alternatively, if the frequency of the generic clock is a multiple of the required SCKn frequency, the MCKn-to-SCKn divider can be used with the ratio defined by writing the CLKCTRLn.MCKDIV field.

**Figure 31-20. Fault Blanking in RAMP1 Operation with Inverted Polarity**




**Fault Qualification**

This is enabled by writing a '1' to the Fault n Qualification bit in the Recoverable Fault n Configuration register (FCTRLn.QUAL). When the recoverable fault qualification is enabled (FCTRLn.QUAL=1), the fault input is disabled all the time the corresponding channel output has an inactive level, as shown in the figures below.

**Figure 31-21. Fault Qualification in RAMP1 Operation**

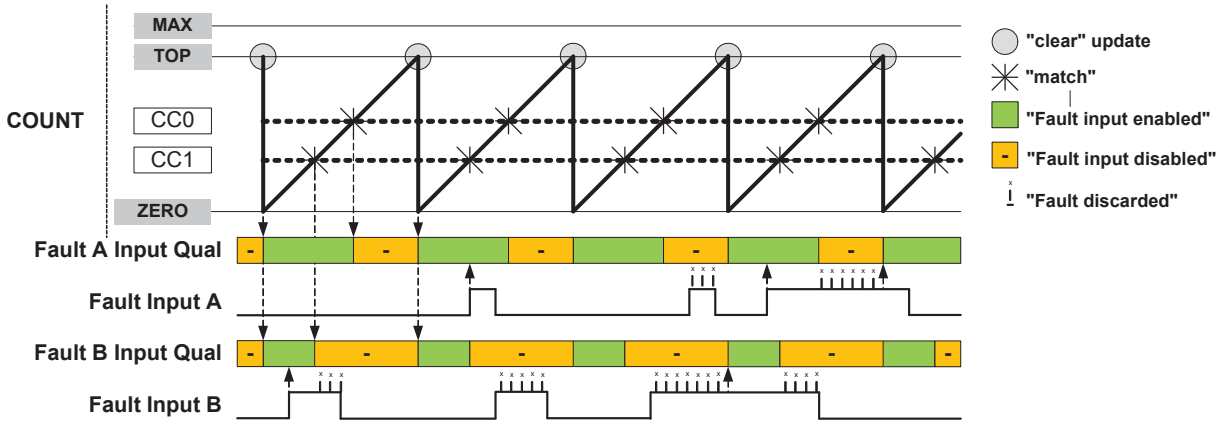



**Figure 31-22. Fault Qualification in RAMP2 Operation with Inverted Polarity**

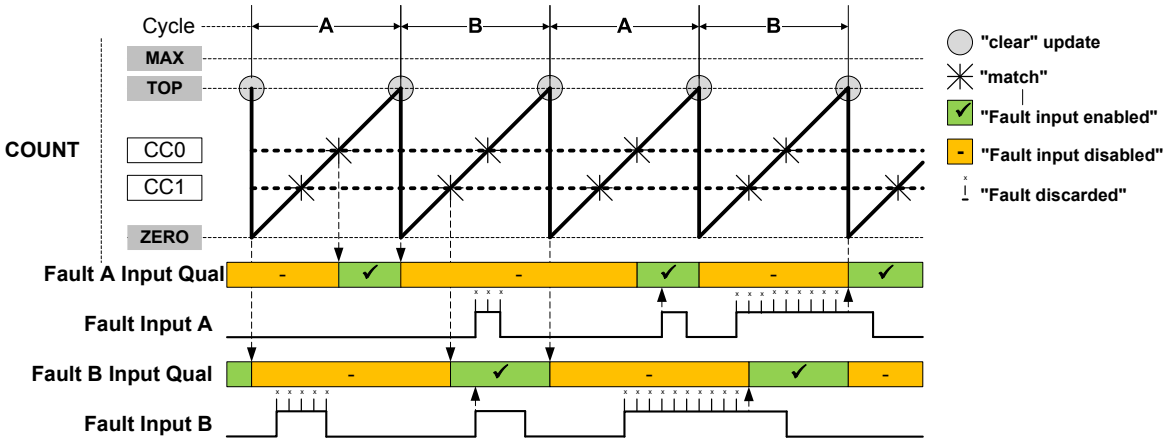
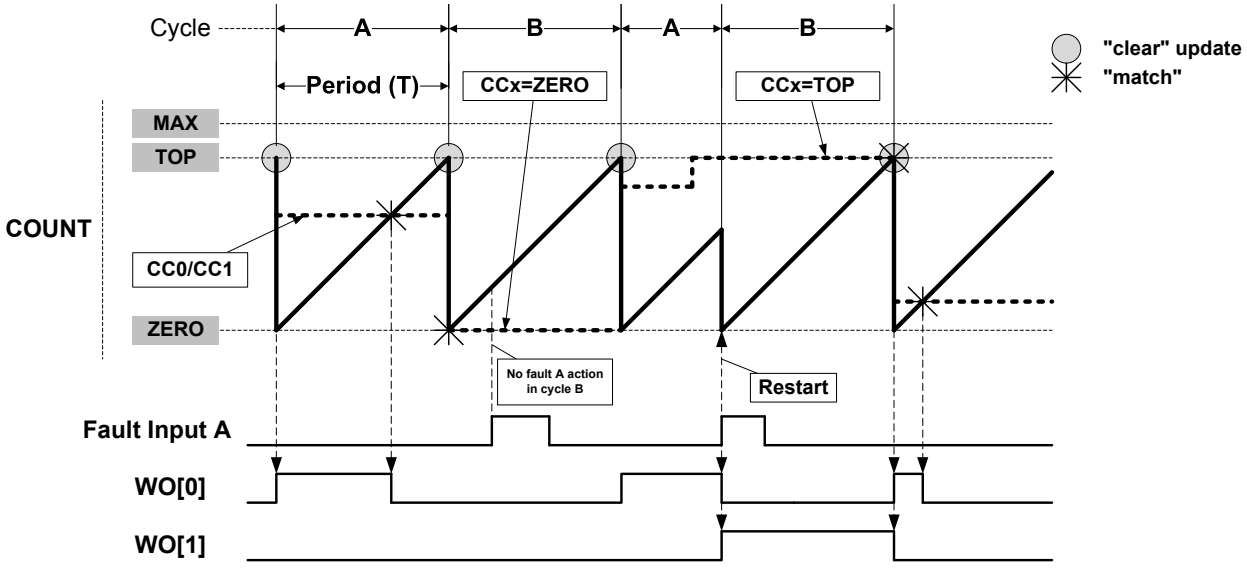


**Figure 31-25. Waveform Generation in RAMP2 mode with Restart Action**




**Capture Action**

Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT - the equivalent to a standard capture operation, for further details refer to Capture Operations
- CAPTMIN - gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued.
- CAPTMAX - gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued, see Figure 31-26.
- LOCMIN - notifies by event or interrupt when a local minimum captured value is detected.
- LOCMAX - notifies by event or interrupt when a local maximum captured value is detected.
- DERIV0 - notifies by event or interrupt when a local extreme captured value is detected, see Figure 31-27.

*CCx Content:*

In CAPTMIN and CAPTMAX operations, CCx keeps the respective extremum captured values, see Figure 31-26. In LOCMIN, LOCMAX or DERIV0 operation, CCx follows the counter value at fault time, see Figure 31-27.

Before enabling CAPTMIN or CAPTMAX mode of capture, the user must initialize the corresponding CCx register value to a value different from zero (for CAPTMIN) top (for CAPTMAX). If the CCx register initial value is zero (for CAPTMIN) top (for CAPTMAX), no captures will be performed using the corresponding channel.

*MCx Behaviour:*

In LOCMIN and LOCMAX operation, capture is performed on each capture event. The MCx interrupt flag is set only when the captured value is upper or equal (for LOCMIN) or lower or equal (for LOCMAX) to the previous captured value. So interrupt flag is set when a new

relative local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected. DERIV0 is equivalent to an OR function of (LOCMIN, LOCMAX).

In CAPT operation, capture is performed on each capture event. The MCx interrupt flag is set on each new capture.

In CAPTMIN and CAPTMAX operation, capture is performed only when on capture event time, the counter value is lower (for CAPTMIN) or upper (for CAPMAX) than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is upper or equal (for CAPTMIN) or lower or equal (for CAPTMAX) to the value captured on the previous event. So interrupt flag is set when a new absolute local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected.

*Interrupt Generation*

In CAPT mode, an interrupt is generated on each filtered Fault n and each dedicated CCx channel capture counter value. In other modes, an interrupt is only generated on an extreme captured value.

**Figure 31-26. Capture Action “CAPTMAX”**

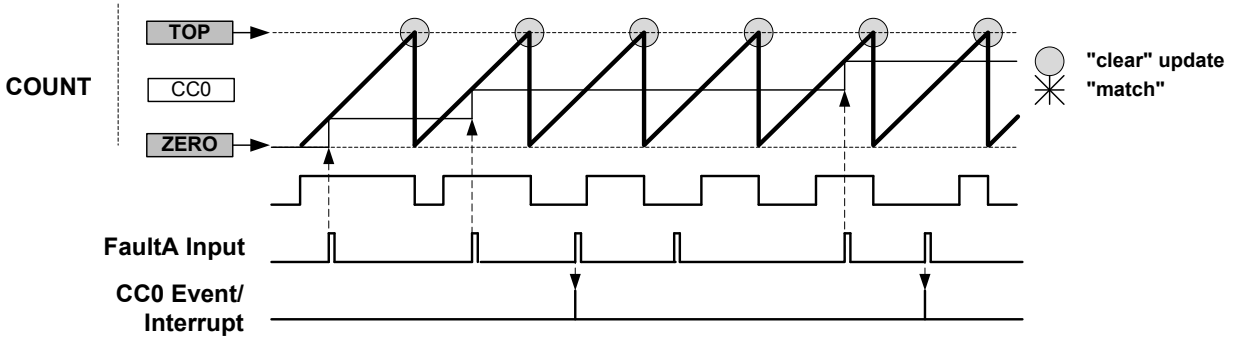
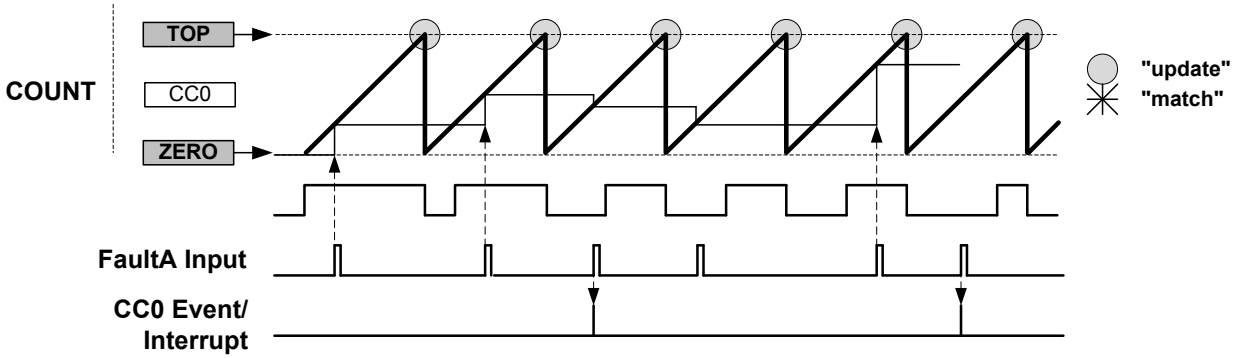



**Figure 31-27. Capture Action “DERIV0”**




**Hardware Halt Action**

This is configured by writing 0x1 to the Fault n Halt mode bits in the Recoverable Fault n Configuration register (FCTRLn.HALT). When enabled, the timer/counter is halted and the cycle is extended as long as the corresponding fault is present.

The next figure ('Waveform Generation with Halt and Restart Actions') shows an example where both restart action and hardware halt action are enabled for Fault A. The compare channel 0 output is clamped to inactive level as long as the timer/counter is halted. The timer/counter resumes the counting operation as soon as the fault condition is no longer present. As the restart action is enabled in this example, the timer/counter is restarted after the fault condition is no longer present.

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1E | Reserved | | | | | | | | | |
| 0x1F | Reserved | | | | | | | | | |
| 0x20 | EPINTSMRY | 7:0 | EPINT[7:0] | | | | | | | |
| 0x21 | | 15:8 | EPINT[15:8] | | | | | | | |
| 0x22 | Reserved | | | | | | | | | |
| 0x23 | Reserved | | | | | | | | | |

**Table 32-2. Device Endpoint Register n**

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1m0 | EPCFGn | 7:0 | | | EPTYPE1[1:0] | | | | EPTYPE0[1:0] | |
| 0x1m1 | Reserved | | | | | | | | | |
| 0x1m2 | Reserved | | | | | | | | | |
| 0x1m3 | Reserved | | | | | | | | | |
| 0x1m4 | EPSTATUSCLRn | 7:0 | BK1RDY | BK0RDY | STALLRQ1 | STALLRQ0 | | CURBK | DTGLIN | DTGLOUT |
| 0x1m5 | EPSTATUSSETn | 7:0 | BK1RDY | BK0RDY | STALLRQ1 | STALLRQ0 | | CURBK | DTGLIN | DTGLOUT |
| 0x1m6 | EPSTATUSn | 7:0 | BK1RDY | BK0RDY | STALLRQ1 | STALLRQ0 | | CURBK | DTGLIN | DTGLOUT |
| 0x1m7 | EPINTFLAGn | 7:0 | | STALL1 | STALL0 | RXSTP | TRFAIL1 | TRFAIL0 | TRCPT1 | TRCPT0 |
| 0x1m8 | EPINTENCLRn | 7:0 | | STALL1 | STALL0 | RXSTP | TRFAIL1 | TRFAIL0 | TRCPT1 | TRCPT0 |
| 0x1m9 | EPINTENSETn | 7:0 | | STALL1 | STALL0 | RXSTP | TRFAIL1 | TRFAIL0 | TRCPT1 | TRCPT0 |
| 0x1mA | Reserved | | | | | | | | | |
| 0x1mB | Reserved | | | | | | | | | |

**Table 32-3. Device Endpoint n Descriptor Bank 0**

| Offset 0x n0 + index | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | ADDR | 7:0 | ADD[7:0] | | | | | | | |
| 0x01 | | 15:8 | ADD[15:8] | | | | | | | |
| 0x02 | | 23:16 | ADD[23:16] | | | | | | | |
| 0x03 | | 31:24 | ADD[31:24] | | | | | | | |
| 0x04 | PCKSIZE | 7:0 | BYTE_COUNT[7:0] | | | | | | | |
| 0x05 | | 15:8 | MULTI_PACKET_SIZE[1:0] | | BYTE_COUNT[13:8] | | | | | |
| 0x06 | | 23:16 | MULTI_PACKET_SIZE[9:2] | | | | | | | |
| 0x07 | | 31:24 | AUTO_ZLP | SIZE[2:0] | | | MULTI_PACKET_SIZE[13:10] | | | |
| 0x08 | EXTREG | 7:0 | VARIABLE[3:0] | | | | SUBPID[3:0] | | | |
| 0x09 | | 15:8 | | VARIABLE[10:4] | | | | | | |
| 0x0A | STATUS_BK | 7:0 | | | | | | | ERRORFLOW | CRCERR |
| 0x0B | Reserved | 7:0 | | | | | | | | |
| 0x0C | Reserved | 7:0 | | | | | | | | |
| 0x0D | Reserved | 7:0 | | | | | | | | |
| 0x0E | Reserved | 7:0 | | | | | | | | |
| 0x0F | Reserved | 7:0 | | | | | | | | |

For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the Power Manager will start CLK_AC_DIG. The comparator is enabled, and after the startup time has passed, a comparison is done and appropriate peripheral events and interrupts are also generated. The comparator and CLK_AC_DIG are then disabled again automatically, unless configured to wake up the system from sleep.

**Related Links**

Electrical Characteristics

### 34.6.3 Selecting Comparator Inputs

Each comparator has one positive and one negative input. The positive input is one of the external input pins (AINx). The negative input can be fed either from an external input pin (AINx) or from one of the several internal reference voltage sources common to all comparators. The user selects the input source as follows:

- The positive input is selected by the Positive Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXPOS)
- The negative input is selected by the Negative Input MUX Select bit group in the Comparator Control register (COMPCTRLx.MUXNEG)

In the case of using an external I/O pin, the selected pin must be configured for analog use in the PORT Controller by disabling the digital input and output. The switching of the analog input multiplexers is controlled to minimize crosstalk between the channels. The input selection must be changed only while the individual comparator is disabled.

**Note:** For internal use of the comparison results by the CCL, this bit must be 0x1 or 0x2.

### 34.6.4 Window Operation

Each comparator pair can be configured to work together in window mode. In this mode, a voltage range is defined, and the comparators give information about whether an input signal is within this range or not. Window mode is enabled by the Window Enable x bit in the Window Control register (WINCTRL.WENx). Both comparators in a pair must have the same measurement mode setting in their respective Comparator Control Registers (COMPCTRLx.SINGLE).

To physically configure the pair of comparators for window mode, the same I/O pin must be chosen as positive input for each comparator, providing a shared input signal. The negative inputs define the range for the window. In Figure 34-4, COMP0 defines the upper limit and COMP1 defines the lower limit of the window, as shown but the window will also work in the opposite configuration with COMP0 lower and COMP1 higher. The current state of the window function is available in the Window x State bit group of the Status register (STATUS.WSTATEx).

Window mode can be configured to generate interrupts when the input voltage changes to below the window, when the input voltage changes to above the window, when the input voltage changes into the window or when the input voltage changes outside the window. The interrupt selections are set by the Window Interrupt Selection bit field in the Window Control register (WINCTRL.WINTSEL). Events are generated using the inside/outside state of the window, regardless of whether the interrupt is enabled or not. Note that the individual comparator outputs, interrupts and events continue to function normally during window mode.

When the comparators are configured for window mode and single-shot mode, measurements are performed simultaneously on both comparators. Writing '1' to either Start Comparison bit in the Control B register (CTRLB.STARTx) will start a measurement. Likewise either peripheral event can start a measurement.

**Table 37-2. General Operating Conditions**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | | 1.62(1) | 3.3 | 3.63 | V |
| $V_{DDANA}$ | Analog supply voltage | | 1.62(1) | 3.3 | 3.63 | V |
| $T_A$ | Temperature range | | -40 | 25 | 85 | °C |
| $T_J$ | Junction temperature | | - | - | 100 | °C |

1. With BOD33 disabled. If the BOD33 is enabled, check Table 37-20.
2.
3.

## 37.4 Supply Characteristics

The following characteristics are applicable to the operating temperature range: $T_A$ = -40°C to 85°C, unless otherwise specified and are valid for a junction temperature up to $T_J$ = 100°C. Refer to *Power Supply and Start-Up Considerations*.

**Table 37-3. Supply Characteristics**

| Symbol | Conditions | Voltage | | |
|---|---|---|---|---|
| | | Min. | Max. | Units |
| $V_{DDIO}$<br>$V_{DDIN}$<br>$V_{DDANA}$ | Full Voltage Range | 1.62 | 3.63 | V |

**Table 37-4. Supply Rise Rates**

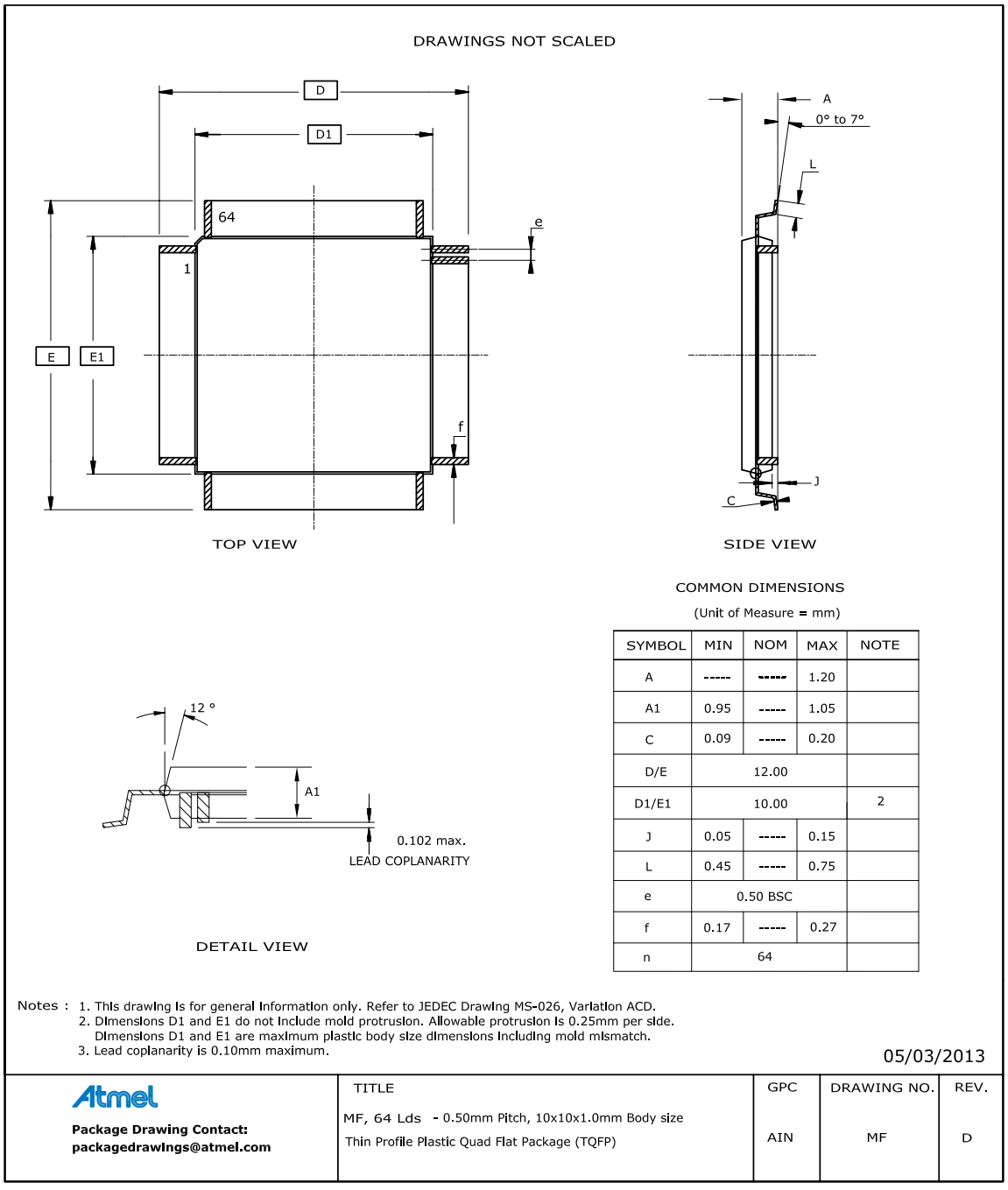
| Symbol | Parameter | Rise Rate | Units |
|---|---|---|---|
| | | Max. | |
| $V_{DDIO}$<br>$V_{DDIN}$<br>$V_{DDANA}$ | DC supply peripheral I/Os, internal regulator and analog supply voltage | 0.1 | V/µs |

**Related Links**

Power Supply and Start-Up Considerations

## 38.2 Package Drawings

### 38.2.1 64 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 1.20 | |
| A1 | 0.95 | ----- | 1.05 | |
| C | 0.09 | ----- | 0.20 | |
| D/E | | 12.00 | | |
| D1/E1 | | 10.00 | | 2 |
| J | 0.05 | ----- | 0.15 | |
| L | 0.45 | ----- | 0.75 | |
| e | | 0.50 BSC | | |
| f | 0.17 | ----- | 0.27 | |
| n | | 64 | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Atmel<br>**Package Drawing Contact:**<br>**packagedrawings@atmel.com** | MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size<br>Thin Profile Plastic Quad Flat Package (TQFP) | AIN | MF | D |

**Table 38-2. Device and Package Maximum Weight**

| | |
|---|---|
| 300 | mg |

**Table 38-3. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Fix/Workaround:**
Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

**2 – The DFLL status bits in the PCLKSR register during the USB clock recovery mode can be wrong after a USB suspend state.**
**Errata reference: 11938**
**Fix/Workaround:**
Do not monitor the DFLL status bits in the PCLKSR register during the USB clock recovery mode.

**3 – If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.**
**Errata reference: 10669**
**Fix/Workaround:**
Check that the lockbits: DFLLLCKC and DFLLLCKF in the SYSCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

#### 40.1.3.5 XOSC32K

**1 – The automatic amplitude control of the XOSC32K does not work.**
**Errata reference: 10933**
**Fix/Workaround:**
Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0)

#### 40.1.3.6 FDPLL

**1 – When changing on-the-fly the FDPLL ratio in DPLLnRATIO register, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.**
**Errata reference: 15753**
**Fix/Workaround:**
Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

#### 40.1.3.7 DMAC

**1 – When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.**
**This happens if the channel number of the channel being enabled is lower than the channel already active.**
**Errata reference: 15683**
**Fix/Workaround:**
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

**2 – If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.**
**Errata reference: 13507**

# 41. Conventions

## 41.1 Numerical Notation

**Table 41-1. Numerical Notation**

| Symbol | Description |
|---|---|
| 165 | Decimal number |
| 0b0101 | Binary number (example 0b0101 = 5 decimal) |
| '0101' | Binary numbers are given without prefix if unambiguous. |
| 0x3B24 | Hexadecimal number |
| X | Represents an unknown or don't care value |
| Z | Represents a high-impedance (floating) state for either a signal or a bus |

## 41.2 Memory Size and Type

**Table 41-2. Memory Size and Bit Rate**

| Symbol | Description |
|---|---|
| KB (kbyte) | kilobyte ($2^{10}$ = 1024) |
| MB (Mbyte) | megabyte ($2^{20}$ = 1024*1024) |
| GB (Gbyte) | gigabyte ($2^{30}$ = 1024*1024*1024) |
| b | bit (binary '0' or '1') |
| B | byte (8 bits) |
| 1kbit/s | 1,000 bit/s rate (not 1,024 bit/s) |
| 1Mbit/s | 1,000,000 bit/s rate |
| 1Gbit/s | 1,000,000,000 bit/s rate |
| word | 32 bit |
| half-word | 16 bit |

## 41.3 Frequency and Time

| Symbol | Description |
|---|---|
| kHz | 1kHz = $10^3$Hz = 1,000Hz |
| KHz | 1KHz = 1,024Hz, 32KHz = 32,768Hz |
| MHz | $10^6$ = 1,000,000Hz |