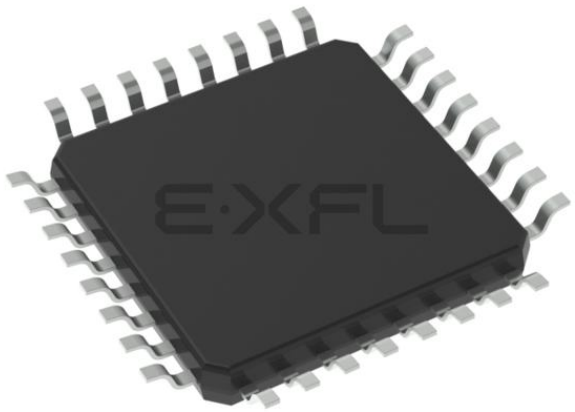


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

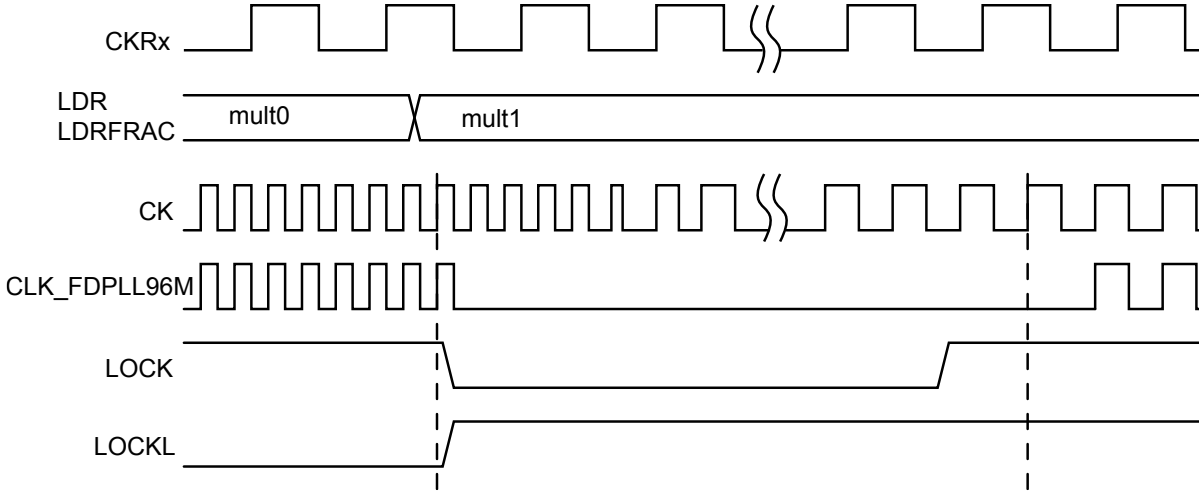
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e17a-af

is set when a falling edge has been detected. The flag is cleared when the software write a one to the interrupt flag bit location.

Figure 17-6. RATIOCTRL Register Update Operation



17.6.8.7 Digital Filter Selection

The PLL digital filter (PI controller) is automatically adjusted in order to provide a good compromise between stability and jitter. Nevertheless a software operation can override the filter setting using the DPLLCTRLB.FILTER field. The DPLLCTRLB.LPEN field can be use to bypass the TDC module.

17.6.9 3.3V Brown-Out Detector Operation

The 3.3V BOD monitors the 3.3V VDDANA supply (BOD33). It supports continuous or sampling modes.

The threshold value action (reset the device or generate an interrupt), the Hysteresis configuration, as well as the enable/disable settings are loaded from Flash User Calibration at startup, and can be overridden by writing to the corresponding BOD33 register bit groups.

17.6.9.1 3.3V Brown-Out Detector (BOD33)

The 3.3V Brown-Out Detector (BOD33) monitors the VDDANA supply and compares the voltage with the brown-out threshold level set in the BOD33 Level bit group (BOD33.LEVEL) in the BOD33 register. The BOD33 can generate either an interrupt or a reset when VDDANA crosses below the brown-out threshold level. The BOD33 detection status can be read from the BOD33 Detection bit (PCLKSR.BOD33DET) in the Power and Clocks Status register.

At start-up or at power-on reset (POR), the BOD33 register values are loaded from the Flash User Row. Refer to *NVM User Row Mapping* for more details.

Related Links

NVM User Row Mapping

17.6.9.2 Continuous Mode

When the BOD33 Mode bit (BOD33.MODE) in the BOD33 register is written to zero and the BOD33 is enabled, the BOD33 operates in continuous mode. In this mode, the BOD33 is continuously monitoring the VDDANA supply voltage.

When the BOD12 Mode bit (BOD12.MODE) in the BOD12 register is written to zero and the BOD12 is enabled(BOD12.ENABLE is written to one), the BOD12 operates in continuous mode. In this mode, the BOD12 is continuously monitoring the VDDCORE supply voltage. Continues mode is not available for BOD12 when running in standby sleep mode.

Continuous mode is the default mode for both BOD12 and BOD33.

Bit 6 – CLKREP: Clock Representation
This bit is valid only in Mode 2 and determines how the hours are represented in the Clock Value (CLOCK) register. This bit can be written only when the peripheral is disabled.

This bit is not synchronized.

Value	Description
0	24 Hour
1	12 Hour (AM/PM)

Bits 3:2 – MODE[1:0]: Operating Mode
These bits define the operating mode of the RTC.

These bits are not synchronized.

MODE[1:0]	Name	Description
0x0	COUNT32	Mode 0: 32-bit Counter
0x1	COUNT16	Mode 1: 16-bit Counter
0x2	CLOCK	Mode 2: Clock/Calendar
0x3		Reserved

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from writing CTRL.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately, and the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY) will be set. STATUS.SYNCBUSY will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST: Software Reset
Writing a zero to this bit has no effect.

Writing a one to this bit resets all registers in the RTC, except DBGCTRL, to their initial state, and the RTC will be disabled.

Writing a one to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization, there is a delay from writing CTRL.SWRST until the reset is complete. CTRL.SWRST and STATUS.SYNCBUSY will both be cleared when the reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

19.8.4 Read Request

Bit 6 – SYNCRDY: Synchronization Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Synchronization Ready Interrupt Enable bit and disable the corresponding interrupt.

Value	Description
0	The synchronization ready interrupt is disabled.
1	The synchronization ready interrupt is enabled, and an interrupt request will be generated when the Synchronization Ready interrupt flag is set.

Bit 0 – ALARM0: Alarm 0 Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit disables the Alarm 0 interrupt.

Value	Description
0	The Alarm 0 interrupt is disabled.
1	The Alarm 0 interrupt is enabled, and an interrupt request will be generated when the Alarm 0 interrupt flag is set.

19.8.11 Interrupt Enable Set - MODE0

Name: INTENSET
Offset: 0x07
Reset: 0x00
Property: Write-Protected

Bit	7	6	5	4	3	2	1	0
	OVF	SYNCRDY						CMP0
Access	R/W	R/W						R/W
Reset	0	0						0

Bit 7 – OVF: Overflow Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Overflow Interrupt Enable bit and enable the Overflow interrupt.

Value	Description
0	The overflow interrupt is disabled.
1	The overflow interrupt is enabled.

Bit 6 – SYNCRDY: Synchronization Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Synchronization Ready Interrupt Enable bit and enable the Synchronization Ready interrupt.

Value	Description
0	The synchronization ready interrupt is disabled.
1	The synchronization ready interrupt is enabled.

Offset	Name	Bit Pos.								
0x10	INTFLAG	7:0	EXTINT7	EXTINT6	EXTINT5	EXTINT4	EXTINT3	EXTINT2	EXTINT1	EXTINT0
0x11		15:8	EXTINT15	EXTINT14	EXTINT13	EXTINT12	EXTINT11	EXTINT10	EXTINT9	EXTINT8
0x12		23:16							EXTINT17	EXTINT16
0x13		31:24								
0x14	WAKEUP	7:0	WAKEUPEN7	WAKEUPEN6	WAKEUPEN5	WAKEUPEN4	WAKEUPEN3	WAKEUPEN2	WAKEUPEN1	WAKEUPEN0
0x15		15:8	WAKEUPEN15	WAKEUPEN14	WAKEUPEN13	WAKEUPEN12	WAKEUPEN11	WAKEUPEN10	WAKEUPEN9	WAKEUPEN8
0x16		23:16							WAKEUPEN17	WAKEUPEN16
0x17		31:24								
0x18	CONFIG0	7:0	FILTEN1	SENSE1[2:0]			FILTEN0	SENSE0[2:0]		
0x19		15:8	FILTEN3	SENSE3[2:0]			FILTEN2	SENSE2[2:0]		
0x1A		23:16	FILTEN5	SENSE5[2:0]			FILTEN4	SENSE4[2:0]		
0x1B		31:24	FILTEN7	SENSE7[2:0]			FILTEN6	SENSE6[2:0]		
0x1C	CONFIG1	7:0	FILTEN9	SENSE9[2:0]			FILTEN8	SENSE8[2:0]		
0x1D		15:8	FILTEN11	SENSE11[2:0]			FILTEN10	SENSE10[2:0]		
0x1E		23:16	FILTEN13	SENSE13[2:0]			FILTEN12	SENSE12[2:0]		
0x1F		31:24	FILTEN15	SENSE15[2:0]			FILTEN14	SENSE14[2:0]		
0x20	CONFIG2	7:0	FILTEN25	SENSE25[2:0]			FILTEN24	SENSE24[2:0]		
0x21		15:8	FILTEN27	SENSE27[2:0]			FILTEN26	SENSE26[2:0]		
0x22		23:16	FILTEN29	SENSE29[2:0]			FILTEN28	SENSE28[2:0]		
0x23		31:24	FILTEN31	SENSE31[2:0]			FILTEN30	SENSE30[2:0]		

21.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

21.8.1 Control

Name: CTRL
Offset: 0x00
Reset: 0x00
Property: Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R/W	R/W
Reset							0	0

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							WAKEUPEN17	WAKEUPEN16
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	WAKEUPEN15	WAKEUPEN14	WAKEUPEN13	WAKEUPEN12	WAKEUPEN11	WAKEUPEN10	WAKEUPEN9	WAKEUPEN8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WAKEUPEN7	WAKEUPEN6	WAKEUPEN5	WAKEUPEN4	WAKEUPEN3	WAKEUPEN2	WAKEUPEN1	WAKEUPEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – WAKEUPENx : External Interrupt x Wake-up Enable [x=17..0]

This bit enables or disables wake-up from sleep modes when the EXTINTx pin matches the external interrupt sense configuration.

Value	Description
0	Wake-up from the EXTINTx pin is disabled.
1	Wake-up from the EXTINTx pin is enabled.

21.8.10 Configuration n

Name: CONFIGn
Offset: 0x18 + n*0x04 [n=0..2]
Reset: 0x00000000
Property: Write-Protected

Bit	31	30	29	28	27	26	25	24
	FILTEN7	SENSE7[2:0]			FILTEN6	SENSE6[2:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FILTEN5	SENSE5[2:0]			FILTEN4	SENSE4[2:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FILTEN3	SENSE3[2:0]			FILTEN2	SENSE2[2:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

USER[7:0]	User Multiplexer	Description	Path Type
0x0F	TCC2 EV1		Asynchronous, synchronous and resynchronized paths
0x10	TCC2 MC0	Match/Capture 0	Asynchronous, synchronous and resynchronized paths
0x11	TCC2 MC1	Match/Capture 1	Asynchronous, synchronous and resynchronized paths
0x12	TC0		Asynchronous, synchronous and resynchronized paths
0x13	TC1		Asynchronous, synchronous and resynchronized paths
0x14	TC2		Asynchronous, synchronous and resynchronized paths
0x15	TC3		Asynchronous, synchronous and resynchronized paths
0x16	TC4		Asynchronous, synchronous and resynchronized paths
0x17	ADC START	ADC start conversion	Asynchronous path only
0x18	ADC SYNC	Flush ADC	Asynchronous path only
0x19	AC COMP0	Start comparator 0	Asynchronous path only
0x1A	AC COMP1	Start comparator 1	Asynchronous path only
0x1B	DAC START	DAC start conversion	Asynchronous path only
0x1C	PTC STCONV	PTC start conversion	Asynchronous path only
0x1D-0x1F	Reserved		Reserved

24.8.4 Channel Status

Name: CHSTATUS
Offset: 0x0C
Reset: 0x000F00FF
Property: -

Bit	31	30	29	28	27	26	25	24
					CHBUSY11	CHBUSY10	CHBUSY9	CHBUSY8
Access					R	R	R	R
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					USRRDY11	USRRDY10	USRRDY9	USRRDY8
Access					R	R	R	R
Reset					0	0	0	0

RXPO[1:0]	Name	Description
0x2	PAD[2]	SERCOM PAD[2] is used for data reception
0x3	PAD[3]	SERCOM PAD[3] is used for data reception

Bits 17:16 – TXPO[1:0]: Transmit Data Pinout
These bits define the transmit data (TxD) and XCK pin configurations.

This bit is not synchronized.

TXPO	TxD Pin Location	XCK Pin Location (When Applicable)	RTS	CTS
0x0	SERCOM PAD[0]	SERCOM PAD[1]	N/A	N/A
0x1	SERCOM PAD[2]	SERCOM PAD[3]	N/A	N/A
0x2	SERCOM PAD[0]	N/A	SERCOM PAD[2]	SERCOM PAD[3]
0x3	Reserved			

Bits 15:13 – SAMPR[2:0]: Sample Rate
These bits select the sample rate.

These bits are not synchronized.

SAMPR[2:0]	Description
0x0	16x over-sampling using arithmetic baud rate generation.
0x1	16x over-sampling using fractional baud rate generation.
0x2	8x over-sampling using arithmetic baud rate generation.
0x3	8x over-sampling using fractional baud rate generation.
0x4	3x over-sampling using arithmetic baud rate generation.
0x5-0x7	Reserved

Bit 8 – IBON: Immediate Buffer Overflow Notification
This bit controls when the buffer overflow status bit (STATUS.BUFOVF) is asserted when a buffer overflow occurs.

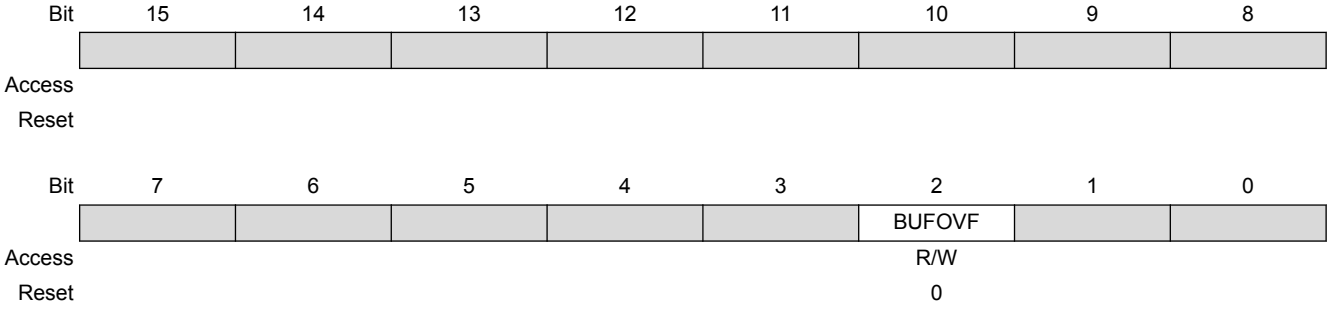
Value	Description
0	STATUS.BUFOVF is asserted when it occurs in the data stream.
1	STATUS.BUFOVF is asserted immediately upon buffer overflow.

Bit 7 – RUNSTDBY: Run In Standby
This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

27.8.7 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: –



Bit 2 – BUFOVF: Buffer Overflow
Reading this bit before reading DATA will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when a buffer overflow condition is detected. See also CTRLA.IBON for overflow handling.

When set, the corresponding RxDATA will be zero.

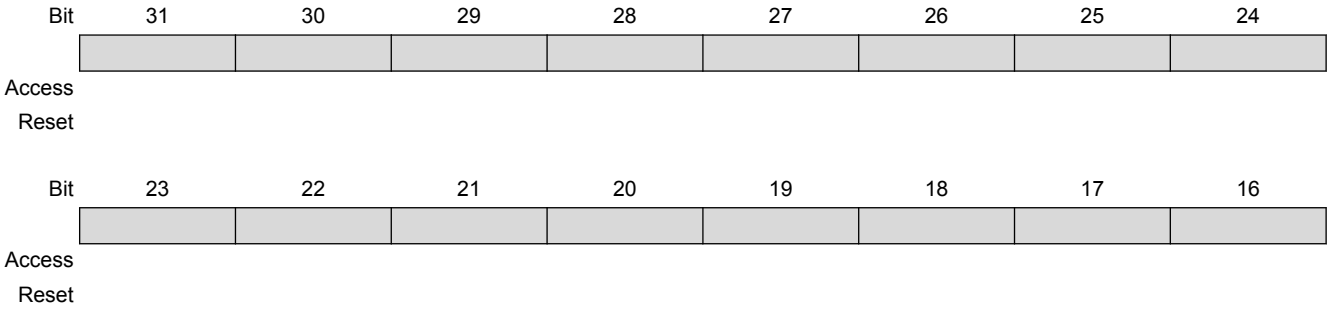
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Value	Description
0	No Buffer Overflow has occurred.
1	A Buffer Overflow has occurred.

27.8.8 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -



Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

28.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		LOWTOUT			SCLSM		SPEED[1:0]	
Access		R/W			R/W		R/W	R/W
Reset		0			0		0	0

Bit	23	22	21	20	19	18	17	16
	SEXTTOEN		SDAHOLD[1:0]					PINOUT
Access	R/W		R/W	R/W				R/W
Reset	0		0	0				0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – LOWTOUT: SCL Low Time-Out
This bit enables the SCL low time-out. If SCL is held low for 25ms-35ms, the slave will release its clock hold, if enabled, and reset the internal state machine. Any interrupt flags set at the time of time-out will remain set.

Value	Description
0	Time-out disabled.
1	Time-out enabled.

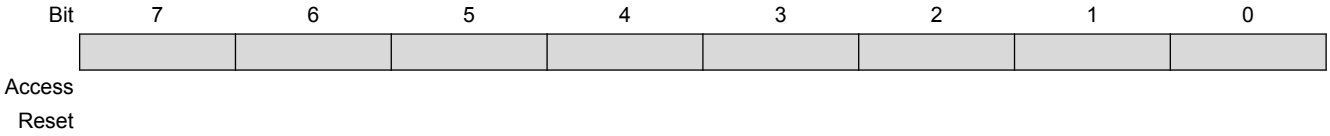
Bit 27 – SCLSM: SCL Clock Stretch Mode
This bit controls when SCL will be stretched for software interaction.

This bit is not synchronized.

Value	Description
0	SCL stretch according to Figure 28-9
1	SCL stretch only after ACK bit according to Figure 28-10

Bits 25:24 – SPEED[1:0]: Transfer Speed
These bits define bus speed.

These bits are not synchronized.



Bit 18 – ACKACT: Acknowledge Action
This bit defines the slave's acknowledge behavior after an address or data byte is received from the master. The acknowledge action is executed when a command is written to the CMD bits. If smart mode is enabled (CTRLB.SMEN=1), the acknowledge action is performed when the DATA register is read.

This bit is not enable-protected.

Value	Description
0	Send ACK
1	Send NACK

Bits 17:16 – CMD[1:0]: Command
This bit field triggers the slave operation as the below. The CMD bits are strobe bits, and always read as zero. The operation is dependent on the slave interrupt flags, INTFLAG.DRDY and INTFLAG.AMATCH, in addition to STATUS.DIR.

All interrupt flags (INTFLAG.DRDY, INTFLAG.AMATCH and INTFLAG.PREC) are automatically cleared when a command is given.

This bit is not enable-protected.

Table 28-3. Command Description

CMD[1:0]	DIR	Action
0x0	X	(No action)
0x1	X	(Reserved)
0x2	Used to complete a transaction in response to a data interrupt (DRDY)	
	0 (Master write)	Execute acknowledge action succeeded by waiting for any start (S/Sr) condition
	1 (Master read)	Wait for any start (S/Sr) condition
0x3	Used in response to an address interrupt (AMATCH)	
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute acknowledge action succeeded by slave data interrupt
	Used in response to a data interrupt (DRDY)	
	0 (Master write)	Execute acknowledge action succeeded by reception of next byte
	1 (Master read)	Execute a byte read operation followed by ACK/NACK reception

Bits 15:14 – AMODE[1:0]: Address Mode
These bits set the addressing mode.

These bits are not write-synchronized.

28.8.8 Address

Name: ADDR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
						ADDRMASK[9:7]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDRMASK[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit	15	14	13	12	11	10	9	8
	TENBITEN					ADDR[9:7]		
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[6:0]							GENCEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 26:17 – ADDRMASK[9:0]: Address Mask
These bits act as a second address match register, an address mask register or the lower limit of an address range, depending on the CTRLB.AMODE setting.

Bit 15 – TENBITEN: Ten Bit Addressing Enable

Value	Description
0	10-bit address recognition disabled.
1	10-bit address recognition enabled.

Bits 10:1 – ADDR[9:0]: Address
These bits contain the I^2C slave address used by the slave address match logic to determine if a master has addressed the slave.

When using 7-bit addressing, the slave address is represented by ADDR[6:0].

When using 10-bit addressing (ADDR.TENBITEN=1), the slave address is represented by ADDR[9:0]

When the address match logic detects a match, INTFLAG.AMATCH is set and STATUS.DIR is updated to indicate whether it is a read or a write transaction.

Bit 0 – GENCEN: General Call Address Enable
A general call address is an address consisting of all-zeroes, including the direction bit (master write).

Bit 0 – SWRST: Software Reset Synchronization Busy
Resetting the SERCOM (CTRLA.SWRST) requires synchronization. When written, the SYNCBUSY.SWRST bit will be set until synchronization is complete.

Writes to any register while synchronization is on-going will be discarded and an APB error will be generated.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

28.10.9 Address

Name: ADDR
Offset: 0x24
Reset: 0x0000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TENBITEN	HS	LENEN			ADDR[2:0]		
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 23:16 – LEN[7:0]: Transaction Length
These bits define the transaction length of a DMA transaction from 0 to 255 bytes. The Transfer Length Enable (LENEN) bit must be written to '1' in order to use DMA.

Bit 15 – TENBITEN: Ten Bit Addressing Enable
This bit enables 10-bit addressing. This bit can be written simultaneously with ADDR to indicate a 10-bit or 7-bit address transmission.

Value	Description
0	10-bit addressing disabled.
1	10-bit addressing enabled.

The FSn pin is used as Word Select in I²S format and as Frame Synchronization in TDM format, as described in I2S Format - Reception and Transmission Sequence with Word Select and TDM Format - Reception and Transmission Sequence, respectively.

29.6.2.2 Data Holding Registers

For each Serializer m, the I²S user interface includes a Data m register (DATAm). They are used to access data samples for all data slots.

Data Reception Mode

In receiver mode, the DATAm registers store the received data.

When a new data word is available in the DATAm register, the Receive Ready bit (RXRDYm) in the Interrupt Flag Status and Clear register (INTFLAG) is set. Reading the DATAm register will clear this bit.

A receive overrun condition occurs if a new data word becomes available before the previous data word has been read from the DATAm register. Then, the Receive Overrun bit in INTFLAG will be set (INTFLAG.RXORm). This interrupt can be cleared by writing a '1' to it.

Data Transmission Mode

In Transmitter mode, the DATAm registers contain the data to be transmitted.

when DATAm is empty, the Transmit Ready bit in the Interrupt Flag Status and Clear register is set (INTFLAG.TXRDYm). Writing to DATAm will clear this bit.

A transmit underrun condition occurs if a new data word needs to be transmitted before it has been written to DATAm. Then, the Transmit Underrun bit in INTFLAG will be set (INTFLAG.TXURm). This interrupt can be cleared by writing a '1' to it. The Transmit Data when Underrun bit in the Serializer n Control register (SERCTRLm.TXSAME) configures whether a zero data word is transmitted in case of underrun (SERCTRLm.TXSAME=0), or the previous data word for the current transmit slot number is transmitted again (SERCTRLm.TXSAME=1).

29.6.3 Master, Controller, and Slave Modes

In Master and Controller modes, the I²S provides the Serial Clock, a Word Select/Frame Sync signal and optionally a Master Clock.

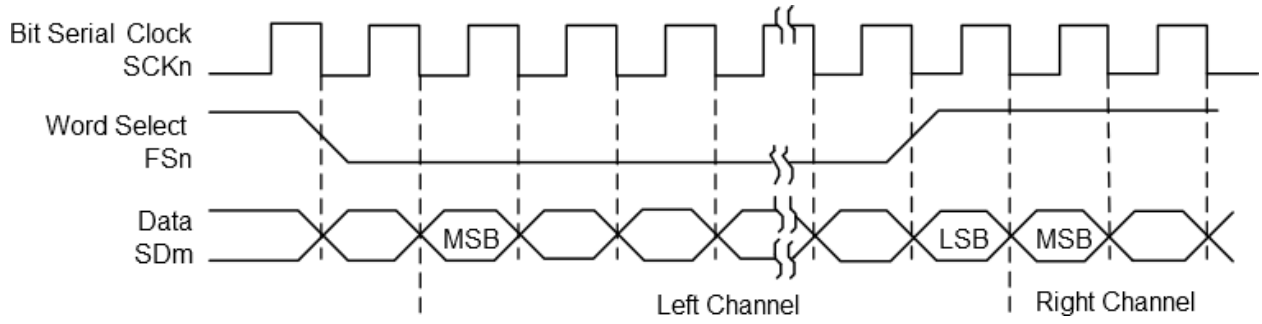
In Controller mode, the I²S Serializers are disabled. Only the clocks are enabled and output for external receivers and/or transmitters.

In Slave mode, the I²S receives the Serial Clock and the Word Select/Frame Sync Signal from an external master. SCKn and FSn pins are inputs.

29.6.4 I²S Format - Reception and Transmission Sequence with Word Select

As specified in the I²S protocol, data bits are left-adjusted in the Word Select slot, with the MSB transmitted first, starting one clock period after the transition on the Word Select line.

Figure 29-5. I²S Reception and Transmission Sequence



data is also received. For instance, writing SERCTRL0.RXLOOP=1 will connect SD1 output to SD0 input, or writing SERCTRL1.RXLOOP=1 will connect SD0 output to SD1 input.

RXLOOP=1 will connect the Transmitter output of the other Serializer to the Receiver input of the current Serializer. For the Loop-back Mode to work, the current Serializer must be configured as receiver and the other Serializer as transmitter.

Writing SERCTRLm.RXLOOP=0 will restore normal behavior and connection between Serializer m and SDm pin input.

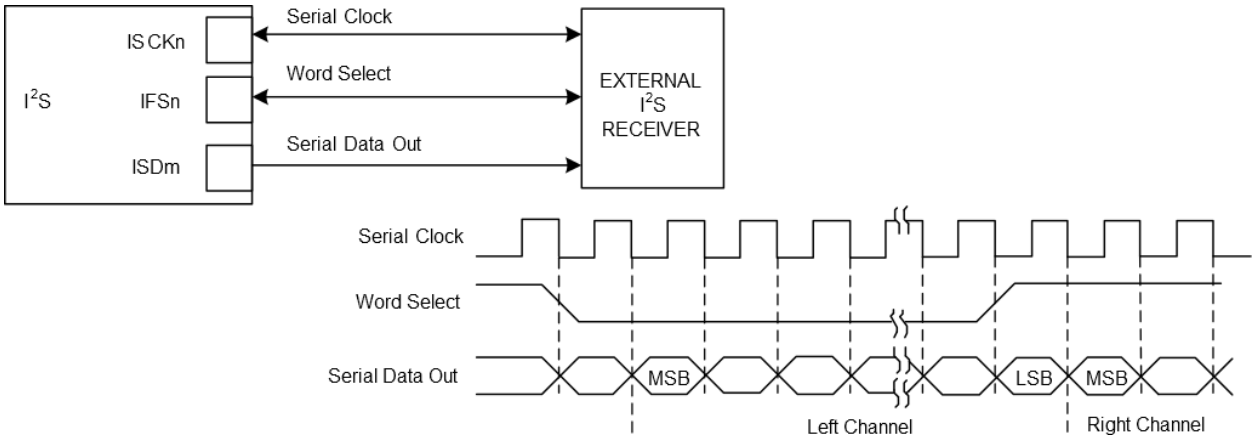
As for other changes to the Serializer configuration, Serializer m must be disabled before writing the SERCTRLm register to update SERCTRLm.RXLOOP.

29.7 I²S Application Examples

The I²S can support several serial communication modes used in audio or high-speed serial links. Some standard applications are shown in the following figures.

Note: The following examples are not a complete list of serial link applications supported by the I²S.

Figure 29-7. Audio Application Block Diagram



inverted high side (HS) of the waveform output with optional dead-time insertion between LS and HS switching. The SWAP unit can swap the LS and HS pin outputs, and can be used for fast decay motor control.

The pattern generation unit can be used to generate synchronized waveforms with constant logic level on TCC UPDATE conditions. This is useful for easy stepper motor and full bridge control.

The non-recoverable fault module enables event controlled fault protection by acting directly on the generated waveforms of the timer/counter compare channel outputs. When a non-recoverable fault condition is detected, the output waveforms are forced to a safe and pre-configured value that is safe for the application. This is typically used for instant and predictable shut down and disabling high current or voltage drives.

The count event sources (TCE0 and TCE1) are shared with the non-recoverable fault extension. The events can be optionally filtered. If the filter options are not used, the non-recoverable faults provide an immediate asynchronous action on waveform output, even for cases where the clock is not present. For further details on how to configure asynchronous events routing, refer to section *EVSYS – Event System*.

Related Links

EVSYS – Event System

31.6.2 Basic Operation

31.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TCC is disabled(CTRLA.ENABLE=0):

- Control A (CTRLA) register, except Run Standby (RUNSTDBY), Enable (ENABLE) and Software Reset (SWRST) bits
- Recoverable Fault n Control registers (FCTRLA and FCTRLB)
- Waveform Extension Control register (WEXCTRL)
- Drive Control register (DRVCTRL)
- Event Control register (EVCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'. Enable-protection is denoted by the “Enable-Protected” property in the register description.

Before the TCC is enabled, it must be configured as outlined by the following steps:

1. Enable the TCC bus clock (CLK_TCCx_APB).
2. If Capture mode is required, enable the channel in capture mode by writing a '1' to the Capture Enable bit in the Control A register (CTRLA.CPTEN).

Optionally, the following configurations can be set before enabling TCC:

1. Select PRESCALER setting in the Control A register (CTRLA.PRESCALER).
2. Select Prescaler Synchronization setting in Control A register (CTRLA.PRESCSYNC).
3. If down-counting operation is desired, write the Counter Direction bit in the Control B Set register (CTRLBSET.DIR) to '1'.
4. Select the Waveform Generation operation in the WAVE register (WAVE.WAVEGEN).
5. Select the Waveform Output Polarity in the WAVE register (WAVE.POL).
6. The waveform output can be inverted for the individual channels using the Waveform Output Invert Enable bit group in the Driver register (DRVCTRL.INVEN).

Bit	7	6	5	4	3	2	1	0
			WINMONEO	RESRDYEO			SYNCEI	STARTEI
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 5 – WINMONEO: Window Monitor Event Out
This bit indicates whether the Window Monitor event output is enabled or not and an output event will be generated when the window monitor detects something.

Value	Description
0	Window Monitor event output is disabled and an event will not be generated.
1	Window Monitor event output is enabled and an event will be generated.

Bit 4 – RESRDYEO: Result Ready Event Out
This bit indicates whether the Result Ready event output is enabled or not and an output event will be generated when the conversion result is available.

Value	Description
0	Result Ready event output is disabled and an event will not be generated.
1	Result Ready event output is enabled and an event will be generated.

Bit 1 – SYNCEI: Synchronization Event In

Value	Description
0	A flush and new conversion will not be triggered on any incoming event.
1	A flush and new conversion will be triggered on any incoming event.

Bit 0 – STARTEI: Start Conversion Event In

Value	Description
0	A new conversion will not be triggered on any incoming event.
1	A new conversion will be triggered on any incoming event.

33.8.10 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x16
Reset: 0x00
Property: Write-Protected

Bit	7	6	5	4	3	2	1	0
					SYNCRDY	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SYNCRDY: Synchronization Ready Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Synchronization Ready Interrupt Enable bit and the corresponding interrupt request.

Figure 34-6. Continuous Mode Filtering

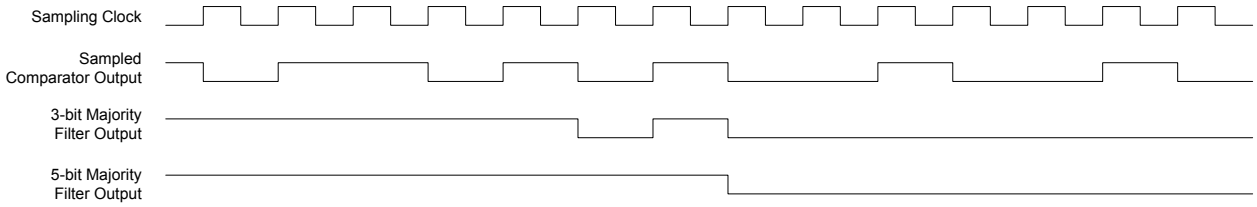
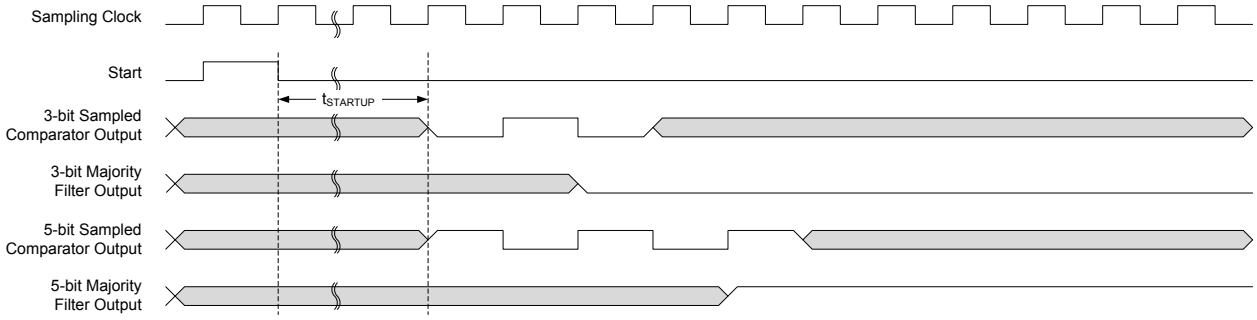


Figure 34-7. Single-Shot Filtering



During sleep modes, filtering is supported only for single-shot measurements. Filtering must be disabled if continuous measurements will be done during sleep modes, or the resulting interrupt/event may be generated incorrectly.

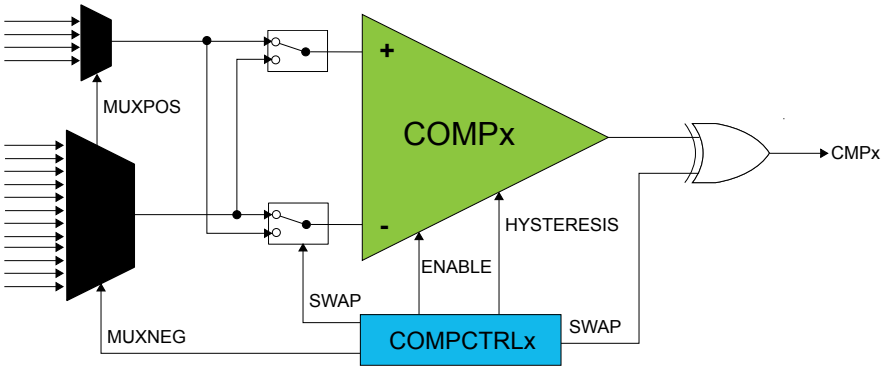
34.6.10 Comparator Output

The output of each comparator can be routed to an I/O pin by setting the Output bit group in the Comparator Control x register (COMPCTRLx.OUT). This allows the comparator to be used by external circuitry. Either the raw, non-synchronized output of the comparator or the CLK_AC-synchronized version, including filtering, can be used as the I/O signal source. The output appears on the corresponding CMP[x] pin.

34.6.11 Offset Compensation

The Swap bit in the Comparator Control registers (COMPCTRLx.SWAP) controls switching of the input signals to a comparator's positive and negative terminals. When the comparator terminals are swapped, the output signal from the comparator is also inverted, as shown in Figure 34-8. This allows the user to measure or compensate for the comparator input offset voltage. As part of the input selection, COMPCTRLx.SWAP can be changed only while the comparator is disabled.

Figure 34-8. Input Swapping for Offset Compensation



34.6.12 Interrupts

The AC has the following interrupt sources:

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Conversion time(1)	1x Gain	6	-	-	cycles
V_{REF}	Voltage reference range		1.0	-	V_{DDANA}-0.6	V
$V_{REFINT1V}$	Internal 1V reference (2)		-	1.0	-	V
$V_{REFINTVCC0}$	Internal ratiometric reference 0(2)		-	V_{DDANA}/ 1.48	-	V
$V_{REFINTVCC0}$ Voltage Error	Internal ratiometric reference 0(2) error	2.0V < V_{DDANA}<3.63V	-1.0	-	+1.0	%
$V_{REFINTVCC1}$	Internal ratiometric reference 1(2)	V_{DDANA}>2.0V	-	V_{DDANA}/2	-	V
$V_{REFINTVCC1}$ Voltage Error	Internal ratiometric reference 1(2) error	2.0V < V_{DDANA}<3.63V	-1.0	-	+1.0	%
	Conversion range(1)	Differential mode	-V_{REF}/ GAIN	-	+V_{REF}/GAIN	V
		Single-ended mode	0.0	-	+V_{REF}/GAIN	V
C_{SAMPLE}	Sampling capacitance(2)		-	3.5	-	pF
R_{SAMPLE}	Input channel source resistance(2)		-	-	3.5	kΩ
I_{DD}	DC supply current(1)	f_{CLK_ADC} = 2.1MHz(3)	-	1.25	1.79	mA

Note:

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.
3. In this condition and for a sample rate of 350ksps, 1 Conversion at gain 1x takes 6 clock cycles of the ADC clock.

Table 37-23. Differential Mode (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number Of Bits	With gain compensation	-	10.5	11.1	bits
TUE	Total Unadjusted Error	1x gain	1.5	4.3	15.0	LSB
INLI	Integral Non Linearity	1x gain	1.0	1.3	4.5	LSB
DNL	Differential Non Linearity	1x gain	+/-0.3	+/-0.5	+/-0.95	LSB

Note:

1. Maximum numbers are based on characterization and not tested in production, and valid for 5% to 95% of the input voltage range.
2. Dynamic parameter numbers are based on characterization and not tested in production.
3. Respect the input common mode voltage through the following equations (where VCM_IN is the Input channel common mode voltage):
   - 1.1. If |VIN| > VREF/4
     - VCM_IN < 0.95*VDDANA + VREF/4 – 0.75V
     - VCM_IN > VREF/4 -0.05*VDDANA -0.1V
   - 1.2. If |VIN| < VREF/4
     - VCM_IN < 1.2*VDDANA - 0.75V
     - VCM_IN > 0.2*VDDANA - 0.1V
4. The ADC channels on pins PA08, PA09, PA10, PA11 are powered from the VDDIO power supply. The ADC performance of these pins will not be the same as all the other ADC channels on pins powered from the VDDANA power supply.
5. The gain accuracy represents the gain error expressed in percent. Gain accuracy (%) = (Gain Error in V x 100) / (2*Vref/GAIN)

Table 37-25. Single-Ended Mode (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number of Bits	With gain compensation	-	9.5	9.8	Bits
TUE	Total Unadjusted Error	1x gain	-	10.5	14.0	LSB
INL	Integral Non-Linearity	1x gain	1.0	1.6	3.5	LSB
DNL	Differential Non-Linearity	1x gain	+/-0.5	+/-0.6	+/-0.95	LSB
	Gain Error	Ext. Ref. 1x	-5.0	0.7	+5.0	mV
	Gain Accuracy(4)	Ext. Ref. 0.5x	+/-0.2	+/-0.34	+/-0.4	%
		Ext. Ref. 2x to 16X	+/-0.01	+/-0.1	+/-0.2	%
	Offset Error	Ext. Ref. 1x	-5.0	1.5	+5.0	mV
SFDR	Spurious Free Dynamic Range	1x gain F_{CLK_ADC} = 2.1MHz F_{IN} = 40kHz A_{IN} = 95%FSR	63.1	65.0	67.0	dB
SINAD	Signal-to-Noise and Distortion		47.5	59.5	61.0	dB
SNR	Signal-to-Noise Ratio		48.0	60.0	64.0	dB
THD	Total Harmonic Distortion		-65.4	-63.0	-62.1	dB
	Noise RMS	T = 25°C	-	1.0	-	mV

Table 37-26. Single-Ended Mode (Device Variant B and C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number of Bits	With gain compensation	-	9.7	10.1	Bits
TUE	Total Unadjusted Error	1x gain	-	7.9	15.0	LSB
INL	Integral Non-Linearity	1x gain	1.4	2.6	4.5	LSB

If a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.
Errata reference: 13262
Fix/Workaround:
Avoid faults few cycles before the end or the beginning of a ramp.

4 – With blanking enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.
Errata reference: 12519
Fix/Workaround:
None

5 – In Dual slope mode a Retrigger Event does not clear the TCC counter.
Errata reference: 12354
Fix/Workaround:
None

6 – In two ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.
Errata reference: 12224
Fix/Workaround:
None

7 – If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.
Errata reference: 12107
Fix/Workaround:
None

8 – When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.
Errata reference: 12477
Fix/Workaround:
None.

9 – TCC fault filtering on inverted fault is not working.
Errata reference: 12512
Fix/Workaround:
Use only non-inverted faults.

10 – When waking up from the STANDBY power save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to 1.
Errata reference: 12227
Fix/Workaround:
After waking up from STANDBY power save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits