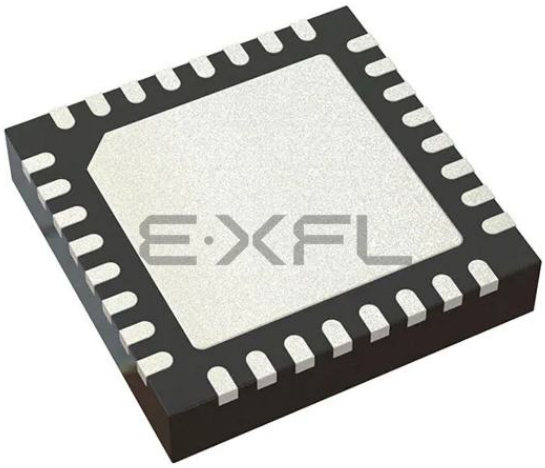

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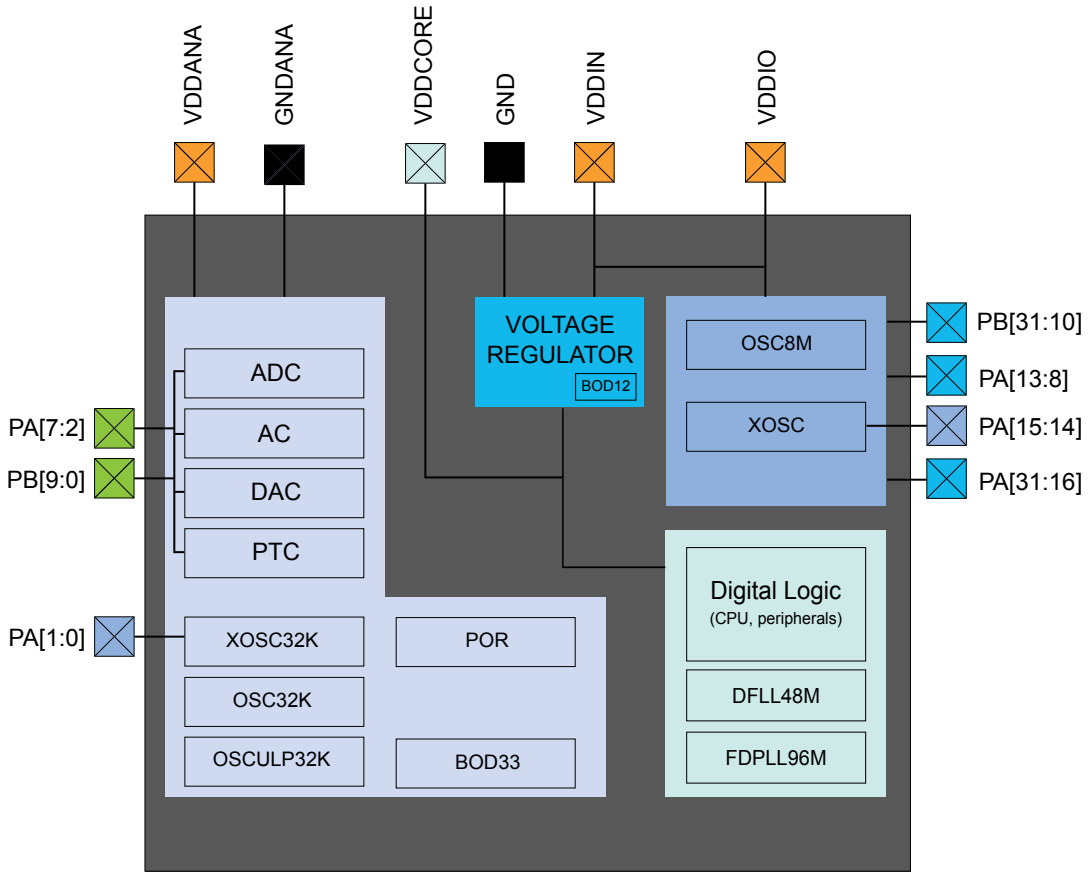
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e17a-mf

8. Power Supply and Start-Up Considerations

8.1 Power Domain Overview



8.2 Power Supply Considerations

8.2.1 Power Supplies

The device has several different power supply pins:

- VDDIO: Powers I/O lines, OSC8M and XOSC. Voltage is 1.62V to 3.63V.
- VDDIN: Powers I/O lines and the internal regulator. Voltage is 1.62V to 3.63V.
- VDDANA: Powers I/O lines and the ADC, AC, DAC, PTC, OSCULP32K, OSC32K, XOSC32K. Voltage is 1.62V to 3.63V.
- VDDCORE: Internal regulated voltage output. Powers the core, memories, peripherals, FDPLL96M, and DFLL48M. Voltage is 1.2V.

The same voltage must be applied to both VDDIN, VDDIO and VDDANA. This common voltage is referred to as V_{DD} in the datasheet.

The ground pins, GND, are common to VDDCORE, VDDIO and VDDIN. The ground pin for VDDANA is GNDANA.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

11.6.2.3 PAC2 Register Description

Write Protect Clear

Name: WPCLR
Offset: 0x00
Reset: 0x00800000
Property: –

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

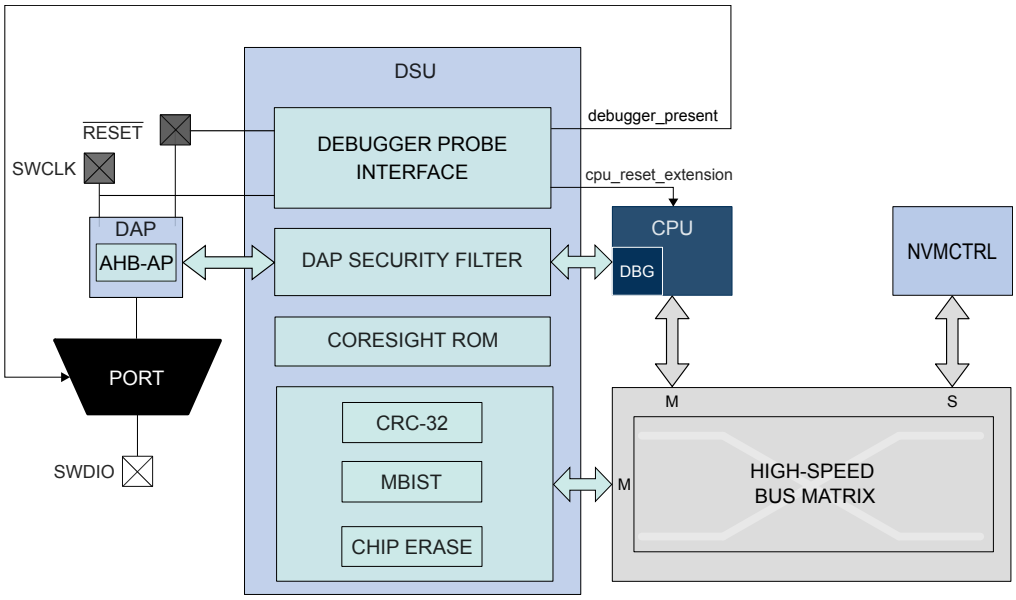
Bit	23	22	21	20	19	18	17	16
				I2S	PTC	DAC	AC	ADC
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TC7	TC4	TC5	TC4	TC3	TCC2	TCC1	TCC0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							EVSYS	
Access							R/W	
Reset							0	

13.3 Block Diagram

Figure 13-1. DSU Block Diagram



13.4 Signal Description

The DSU uses three signals to function.

Signal Name	Type	Description
$\overline{\text{RESET}}$	Digital Input	External reset
SWCLK	Digital Input	SW clock
SWDIO	Digital I/O	SW bidirectional data pin

Related Links

I/O Multiplexing and Considerations

13.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

13.5.1 IO Lines

The SWCLK pin is by default assigned to the DSU module to allow debugger probe detection and to stretch the CPU reset phase. For more information, refer to Debugger Probe Detection. The Hot-Plugging feature depends on the PORT configuration. If the SWCLK pin function is changed in the PORT or if the PORT_MUX is disabled, the Hot-Plugging feature is disabled until a power-reset or an external reset.

13.5.2 Power Management

The DSU will continue to operate in any sleep mode where the selected source clock is running.

Related Links

PM – Power Manager

1. Enable the Suspend interrupt for the DMA channel.
2. Enable the DMA channel.
3. Reserve memory space in SRAM to configure a new descriptor.
4. Configure the new descriptor:
   – Set the next descriptor address (DESCADDR)
   – Set the destination address (DSTADDR)
   – Set the source address (SRCADDR)
   – Configure the block transfer control (BTCTRL) including
      • Optionally enable the Suspend block action
      • Set the descriptor VALID bit
5. Clear the VALID bit for the existing list and for the descriptor which has to be updated.
6. Read DESCADDR from the Write-Back memory.
   – If the DMA has not already fetched the descriptor which requires changes (i.e., DESCADDR is wrong):
      • Update the DESCADDR location of the descriptor from the List
      • Optionally clear the Suspend block action
      • Set the descriptor VALID bit to '1'
      • Optionally enable the Resume software command
   – If the DMA is executing the same descriptor as the one which requires changes:
      • Set the Channel Suspend software command and wait for the Suspend interrupt
      • Update the next descriptor address (DESCRADDR) in the write-back memory
      • Clear the interrupt sources and set the Resume software command
      • Update the DESCADDR location of the descriptor from the List
      • Optionally clear the Suspend block action
      • Set the descriptor VALID bit to '1'
7. Go to step 4 if needed.

Adding a Descriptor Between Existing Descriptors

To insert a new descriptor 'C' between two existing descriptors ('A' and 'B'), the descriptor currently executed by the DMA must be identified.

1. If DMA is executing descriptor B, descriptor C cannot be inserted.
2. If DMA has not started to execute descriptor A, follow the steps:
   2.1. Set the descriptor A VALID bit to '0'.
   2.2. Set the DESCADDR value of descriptor A to point to descriptor C instead of descriptor B.
   2.3. Set the DESCADDR value of descriptor C to point to descriptor B.
   2.4. Set the descriptor A VALID bit to '1'.
3. If DMA is executing descriptor A:
   3.1. Apply the software suspend command to the channel and
   3.2. Perform steps 2.1 through 2.4.
   3.3. Apply the software resume command to the channel.

20.6.3.2 Channel Suspend

The channel operation can be suspended at any time by software by writing a '1' to the Suspend command in the Command bit field of Channel Control B register (CHCTRLB.CMD). After the ongoing burst transfer is completed, the channel operation is suspended and the suspend command is automatically cleared.

Value	Name	Description
0x2E	CHN	DMA channel 14
0x2F	CHN	DMA channel 15
0x30	CHN	DMA channel 16
0x31	CHN	DMA channel 17
0x32	CHN	DMA channel 18
0x33	CHN	DMA channel 19
0x34	CHN	DMA channel 20
0x35	CHN	DMA channel 21
0x36	CHN	DMA channel 22
0x37	CHN	DMA channel 23
0x38	CHN	DMA channel 24
0x39	CHN	DMA channel 25
0x3A	CHN	DMA channel 26
0x3B	CHN	DMA channel 27
0x3C	CHN	DMA channel 28
0x3D	CHN	DMA channel 29
0x3E	CHN	DMA channel 30
0x3F	CHN	DMA channel 31

Bits 3:2 – CRCPOLY[1:0]: CRC Polynomial Type
These bits define the size of the data transfer for each bus access when the CRC is used with I/O interface, as shown in the table below.

Value	Name	Description
0x0	CRC16	CRC-16 (CRC-CCITT)
0x1	CRC32	CRC32 (IEEE 802.3)
0x2-0x3		Reserved

Bits 1:0 – CRCBEATSIZE[1:0]: CRC Beat Size
These bits define the size of the data transfer for each bus access when the CRC is used with I/O interface.

Value	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	HWORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
0x3		Reserved

20.8.3 CRC Data Input

Name: CRCDATAIN
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	WRBADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – WRBADDR[31:0]: Write-Back Memory Base Address
These bits store the Write-Back memory base address. The value must be 128-bit aligned.

20.8.17 Channel ID

Name: CHID
Offset: 0x3F
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					ID[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – ID[3:0]: Channel ID
These bits define the channel number that will be affected by the channel registers (CH*). Before reading or writing a channel register, the channel ID bit group must be written first.

20.8.18 Channel Control A

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name: CHCTRLA
Offset: 0x40
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access	R		R	R	R	R	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 1 – ENABLE: Channel Enable
Writing a '0' to this bit during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

Writing a '1' to this bit will enable the DMA channel.

This bit is not enable-protected.

Value	Description
0	DMA channel is disabled.
1	DMA channel is enabled.

22. NVMCTRL – Non-Volatile Memory Controller

22.1 Overview

Non-Volatile Memory (NVM) is a reprogrammable Flash memory that retains program and data storage even with power off. It embeds a main array and a separate smaller array intended for EEPROM emulation (RWWEE) that can be programmed while reading the main array. The NVM Controller (NVMCTRL) connects to the AHB and APB bus interfaces for system access to the NVM block. The AHB interface is used for reads and writes to the NVM block, while the APB interface is used for commands and configuration.

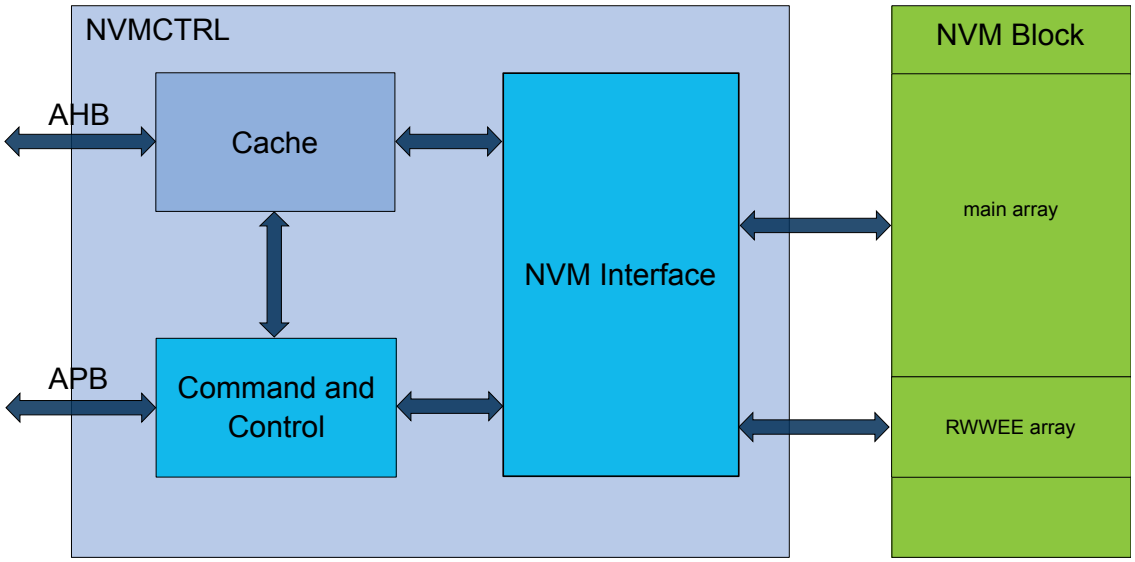
22.2 Features

- 32-bit AHB interface for reads and writes
- Read While Write EEPROM emulation area
- All NVM sections are memory mapped to the AHB, including calibration and system configuration
- 32-bit APB interface for commands and control
- Programmable wait states for read optimization
- 16 regions can be individually protected or unprotected
- Additional protection for boot loader
- Supports device protection through a security bit
- Interface to Power Manager for power-down of Flash blocks in sleep modes
- Can optionally wake up on exit from sleep or on first access
- Direct-mapped cache

Note: A register with property "Enable-Protected" may contain bits that are *not* enable-protected.

22.3 Block Diagram

Figure 22-1. Block Diagram



Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Refer to Register Access Protection.

24.8.1 Control

Name: CTRL
Offset: 0x00
Reset: 0x00
Property: Write-Protected

Bit	7	6	5	4	3	2	1	0
				GCLKREQ				SWRST
Access				R/W				W
Reset				0				0

Bit 4 – GCLKREQ: Generic Clock Requests
This bit is used to determine whether the generic clocks used for the different channels should be on all the time or only when an event needs the generic clock. Events propagated through asynchronous paths will not need a generic clock.

Value	Description
0	Generic clock is requested and turned on only if an event is detected.
1	Generic clock for a channel is always on.

Bit 0 – SWRST: Software Reset
Writing a zero to this bit has no effect.

Writing a one to this bit resets all registers in the EVSYS to their initial state.

Writing a one to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Note: Before applying a Software Reset it is recommended to disable the event generators.

24.8.2 Channel

Name: CHANNEL
Offset: 0x04
Reset: 0x00000000
Property: Write-Protected

Bit	31	30	29	28	27	26	25	24
					EDGSEL[1:0]		PATH[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

USER[7:0]	User Multiplexer	Description	Path Type
0x0F	TCC2 EV1		Asynchronous, synchronous and resynchronized paths
0x10	TCC2 MC0	Match/Capture 0	Asynchronous, synchronous and resynchronized paths
0x11	TCC2 MC1	Match/Capture 1	Asynchronous, synchronous and resynchronized paths
0x12	TC0		Asynchronous, synchronous and resynchronized paths
0x13	TC1		Asynchronous, synchronous and resynchronized paths
0x14	TC2		Asynchronous, synchronous and resynchronized paths
0x15	TC3		Asynchronous, synchronous and resynchronized paths
0x16	TC4		Asynchronous, synchronous and resynchronized paths
0x17	ADC START	ADC start conversion	Asynchronous path only
0x18	ADC SYNC	Flush ADC	Asynchronous path only
0x19	AC COMP0	Start comparator 0	Asynchronous path only
0x1A	AC COMP1	Start comparator 1	Asynchronous path only
0x1B	DAC START	DAC start conversion	Asynchronous path only
0x1C	PTC STCONV	PTC start conversion	Asynchronous path only
0x1D-0x1F	Reserved		Reserved

24.8.4 Channel Status

Name: CHSTATUS
Offset: 0x0C
Reset: 0x000F00FF
Property: -

Bit	31	30	29	28	27	26	25	24
					CHBUSY11	CHBUSY10	CHBUSY9	CHBUSY8
Access					R	R	R	R
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					USRRDY11	USRRDY10	USRRDY9	USRRDY8
Access					R	R	R	R
Reset					0	0	0	0

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

26.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		DORD	CPOL	CMODE	FORM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SAMPA[1:0]		RXPO[1:0]				TXPO[1:0]	
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0

Bit	15	14	13	12	11	10	9	8
	SAMPR[2:0]							IBON
Access	R/W	R/W	R/W					R
Reset	0	0	0					0

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – DORD: Data Order
This bit selects the data order when a character is shifted out from the Data register.

This bit is not synchronized.

Value	Description
0	MSB is transmitted first.
1	LSB is transmitted first.

Bit 29 – CPOL: Clock Polarity
This bit selects the relationship between data output change and data input sampling in synchronous mode.

This bit is not synchronized.

When paired, the TC peripherals are configured using the registers of the even-numbered TC (TC4 or TC6 respectively). The odd-numbered partner (TC3 or TC5 respectively) will act as slave, and the Slave bit in the Status register (STATUS.SLAVE) will be set. The register values of a slave will not reflect the registers of the 32-bit counter. Writing to any of the slave registers will not affect the 32-bit counter. Normal access to the slave COUNT and CCx registers is not allowed.

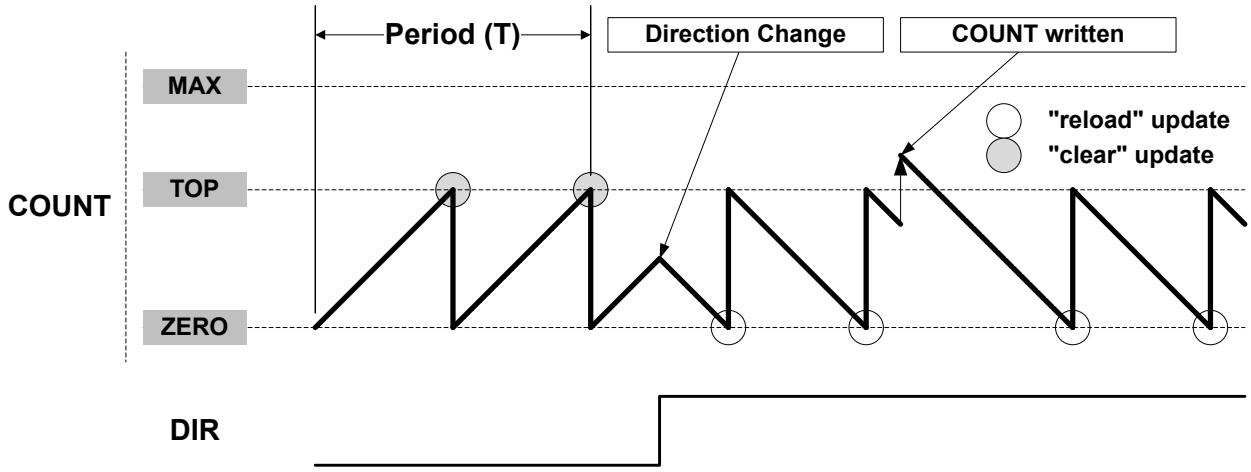
30.6.2.5 Counter Operations

The counter can be set to count up or down. When the counter is counting up and the top value is reached, the counter will wrap around to zero on the next clock cycle. When counting down, the counter will wrap around to the top value when zero is reached. In one-shot mode, the counter will stop counting after a wraparound occurs.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If this bit is zero the counter is counting up, and counting down if CTRLB.DIR=1. The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it is counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. It is also possible to generate an event on overflow or underflow when the Overflow/Underflow Event Output Enable bit in the Event Control register (EVCTRL.OVFEO) is one.

It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. When starting the TC, the COUNT value will be either ZERO or TOP (depending on the counting direction set by CTRLBSET.DIR or CTRLBCLR.DIR), unless a different value has been written to it, or the TC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed during normal operation. See also the figure below.

Figure 30-3. Counter Operation



Stop Command and Event Action

A Stop command can be issued from software by using Command bits in the Control B Set register (CTRLBSET.CMD = 0x2, STOP). When a Stop is detected while the counter is running, the counter will be loaded with the starting value (ZERO or TOP, depending on direction set by CTRLBSET.DIR or CTRLBCLR.DIR). All waveforms are cleared and the Stop bit in the Status register is set (STATUS.STOP).

Re-Trigger Command and Event Action

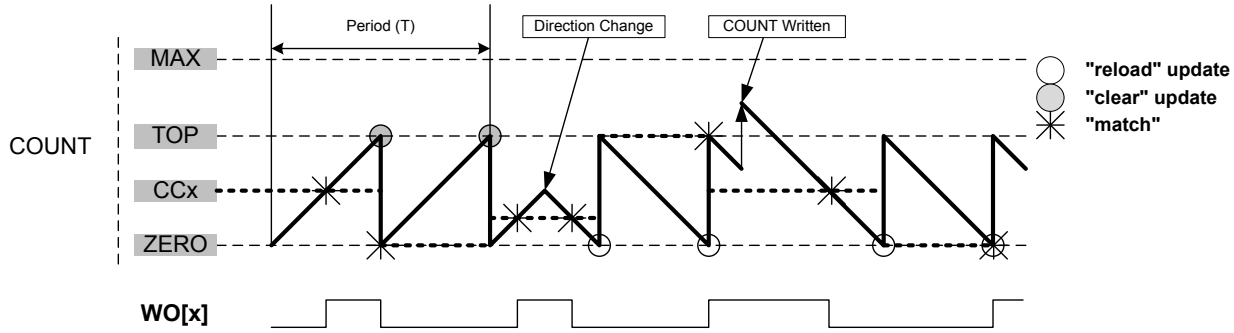
A re-trigger command can be issued from software by writing the Command bits in the Control B Set register (CTRLBSET.CMD = 0x1, RETRIGGER), or from event when a re-trigger event action is configured in the Event Control register (EVCTRL.EVACT = 0x1, RETRIGGER).

Frequency Operation

Normal Frequency Generation (NFRQ)

For Normal Frequency Generation, the period time (T) is controlled by the period register (PER) for 8-bit counter mode and MAX for 16- and 32-bit mode. The waveform generation output (WO[x]) is toggled on each compare match between COUNT and CCx, and the corresponding Match or Capture Channel x Interrupt Flag (INTFLAG.MCx) will be set.

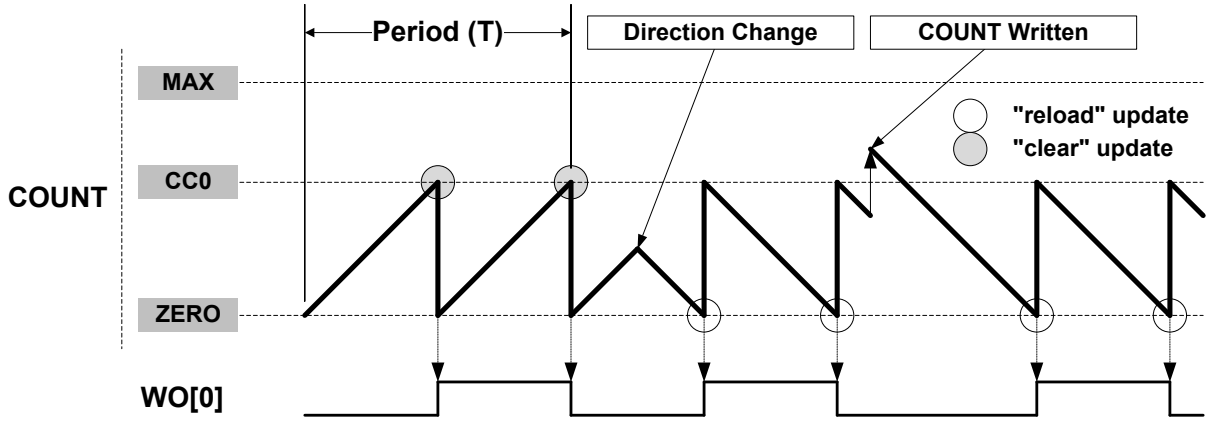
Figure 30-4. Normal Frequency Operation



Match Frequency Generation (MFRQ)

For Match Frequency Generation, the period time (T) is controlled by the CC0 register instead of PER or MAX. WO[0] toggles on each update condition.

Figure 30-5. Match Frequency Operation



PWM Operation

Normal Pulse-Width Modulation Operation (NPWM)

NPWM uses single-slope PWM generation.

For single-slope PWM generation, the period time (T) is controlled by the TOP value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

The following equation calculates the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{PWM\_SS} = \frac{\log(TOP+1)}{\log(2)}$$

Bit 4 – TXSTP: Transmitted Setup Interrupt Flag
This flag is cleared by writing a one to the flag.

This flag is set when a Transfer Complete occurs and will generate an interrupt if PINTENCLR/SET.TXSTP is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the TXSTP Interrupt Flag.

Bit 3 – PERR: Pipe Error Interrupt Flag
This flag is cleared by writing a one to the flag.

This flag is set when a pipe error occurs and will generate an interrupt if PINTENCLR/SET.PERR is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the PERR Interrupt Flag.

Bit 2 – TRFAIL: Transfer Fail Interrupt Flag
This flag is cleared by writing a one to the flag.

This flag is set when a Transfer Fail occurs and will generate an interrupt if PINTENCLR/SET.TRFAIL is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the TRFAIL Interrupt Flag.

Bit 0 – TRCPT: Transfer Complete x interrupt Flag
This flag is cleared by writing a one to the flag.

This flag is set when a Transfer complete occurs and will generate an interrupt if PINTENCLR/SET.TRCPT is one. PINTFLAG.TRCPT is set for a single bank IN/OUT pipe or a double bank IN/OUT pipe when current bank is 0.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the TRCPT Interrupt Flag.

32.8.6.7 Host Pipe Interrupt Clear Register

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Pipe Interrupt Enable Set (PINTENSET) register.

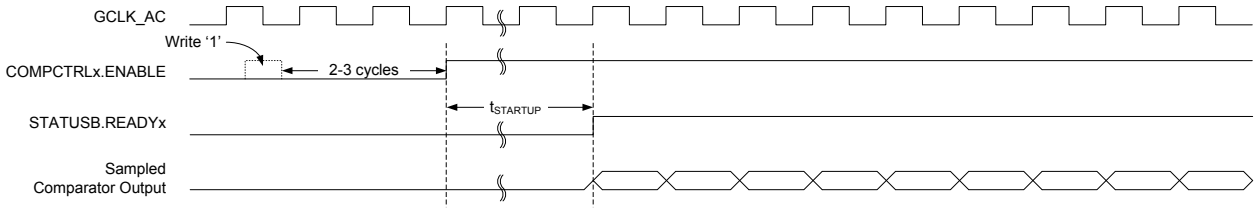
This register is cleared by USB reset or when PEN[n] is zero.

Name: PINTENCLR
Offset: 0x108 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
			STALL	TXSTP	PERR	TRFAIL		TRCPT
Access			R/W	R/W	R/W	R/W		R/W
Reset			0	0	0	0		0

In continuous operation, edge detection of the comparator output for interrupts is done by comparing the current and previous sample. The sampling rate is the CLK_AC_DIG frequency. An example of continuous measurement is shown in the next figure.

Figure 34-2. Continuous Measurement Example



For low-power operation, comparisons can be performed during sleep modes without a clock. The comparator is enabled continuously, and changes of the comparator state are detected asynchronously. When a toggle occurs, the Power Manager will start CLK_AC_DIG to register the appropriate peripheral events and interrupts. The CLK_AC_DIG clock is then disabled again automatically, unless configured to wake up the system from sleep.

Related Links

Electrical Characteristics

Single-Shot

Single-shot operation is selected by writing COMPCTRLx.SINGLE to '1'. During single-shot operation, the comparator is normally idle. The user starts a single comparison by writing '1' to the respective Start Comparison bit in the write-only Control B register (CTRLB.STARTx). The comparator is enabled, and after the start-up time has passed, a single comparison is done and STATUSA is updated. Appropriate peripheral events and interrupts are also generated. No new comparisons will be performed.

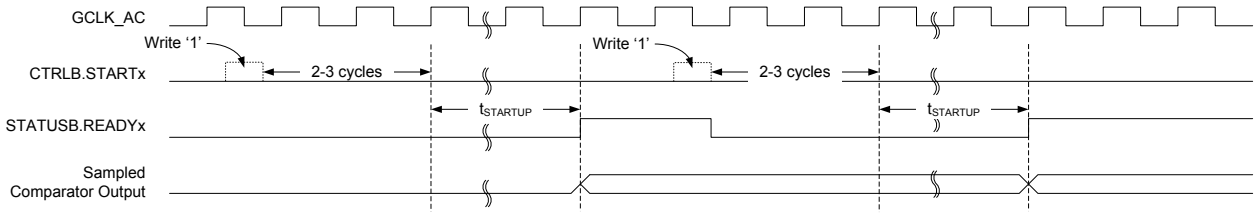
Writing '1' to CTRLB.STARTx also clears the Comparator x Ready bit in the Status B register (STATUSB.READYx). STATUSB.READYx is set automatically by hardware when the single comparison has completed.

To remove the need for polling, an additional means of starting the comparison is also available. A read of the Status C register (STATUSC) will start a comparison on all comparators currently configured for single-shot operation. The read will stall the bus until all enabled comparators are ready. If a comparator is already busy with a comparison, the read will stall until the current comparison is compete, and a new comparison will not be started.

A single-shot measurement can also be triggered by the Event System. Setting the Comparator x Event Input bit in the Event Control Register (EVCTRL.COMPEIx) enables triggering on incoming peripheral events. Each comparator can be triggered independently by separate events. Event-triggered operation is similar to user-triggered operation; the difference is that a peripheral event from another hardware module causes the hardware to automatically start the comparison and clear STATUSB.READYx.

To detect an edge of the comparator output in single-shot operation for the purpose of interrupts, the result of the current measurement is compared with the result of the previous measurement (one sampling period earlier). An example of single-shot operation is shown in the figure below.

Figure 34-3. Single-Shot Example



- Comparator (COMP0, COMP1): Indicates a change in comparator status.
- Window (WIN0): Indicates a change in the window status.

Comparator interrupts are generated based on the conditions selected by the Interrupt Selection bit group in the Comparator Control registers (COMPCTRLx.INTSEL). Window interrupts are generated based on the conditions selected by the Window Interrupt Selection bit group in the Window Control register (WINCTRL.WINTSEL[1:0]).

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the AC is reset. See INFLAG register for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated.

Related Links

Nested Vector Interrupt Controller

34.6.13 Events

The AC can generate the following output events:

- Comparator (COMP0, COMP1): Generated as a copy of the comparator status
- Window (WIN0): Generated as a copy of the window inside/outside status

Output events must be enabled to be generated. Writing a one to an Event Output bit in the Event Control register (EVCTRL.COMPEOx) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. The events must be correctly routed in the Event System.

The AC can take the following action on an input event:

- Single-shot measurement
- Single-shot measurement in window mode

Writing a one to an Event Input bit into the Event Control register (EVCTRL.COMPEIx) enables the corresponding action on input event. Writing a zero to this bit disables the corresponding action on input event. Note that if several events are connected to the AC, the enabled action will be taken on any of the incoming events. Refer to the Event System chapter for details on configuring the event system.

When EVCTRL.COMPEIx is one, the event will start a comparison on COMPx after the start-up time delay. In normal mode, each comparator responds to its corresponding input event independently. For a pair of comparators in window mode, either comparator event will trigger a comparison on both comparators simultaneously.

34.6.14 Sleep Mode Operation

The Run in Standby bits in the Comparator x Control registers (COMPCTRLx.RUNSTDBY) control the behavior of the AC during standby sleep mode. Each RUNSTDBY bit controls one comparator. When the bit is zero, the comparator is disabled during sleep, but maintains its current configuration. When the bit is one, the comparator continues to operate during sleep. Note that when RUNSTDBY is zero, the analog blocks are powered off for the lowest power consumption. This necessitates a start-up time delay when the system returns from sleep.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Variation over V_{DDANA} voltage	V_{DDANA}=1.62V to 3.6V	-1.7	1	3.7	mV/V
	Temperature Sensor accuracy	Using the method described in the Software-based Refinement of the Actual Temperature	-10	-	10	°C

Table 37-38. Temperature Sensor Characteristics(1) (Device Variant B and C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Temperature sensor output voltage	T= 25°C, V_{DDANA} = 3.3V	-	0.688	-	V
	Temperature sensor slope		2.06	2.16	2.26	mV/°C
	Variation over V_{DDANA} voltage	V_{DDANA}=1.62V to 3.6V	-0.4	1.4	3	mV/V
	Temperature Sensor accuracy	Using the method described in the Software-based Refinement of the Actual Temperature	-10	-	10	°C

Note: 1. These values are based on characterization. These values are not covered by test limits in production.

37.10.8.2 Software-based Refinement of the Actual Temperature

The temperature sensor behavior is linear but depends on several parameters such as the internal voltage reference, which itself depends on the temperature. To take this into account, each device contains a Temperature Log row with data measured and written during the production tests. These calibration values should be read by software to infer the most accurate temperature readings possible.

This Software Temperature Log row can be read at address 0x00806030

This section specifies the Temperature Log row content and explains how to refine the temperature sensor output using the values in the Temperature Log row.

Temperature Log Row

All values in this row were measured in the following conditions:

- V_{DDIN} = V_{DDIO} = V_{DDANA} = 3.3V
- ADC Clock speed = 1MHz
- ADC mode: Free running mode, ADC averaging mode with 4 averaged samples
- ADC voltage reference = 1.0V internal reference (INT1V)
- ADC input = Temperature sensor

Table 37-39. Temperature Log Row Content

Bit position	Name	Description
7:0	ROOM_TEMP_VAL_INT	Integer part of room temperature in °C
11:8	ROOM_TEMP_VAL_DEC	Decimal part of room temperature
19:12	HOT_TEMP_VAL_INT	Integer part of hot temperature in °C

Do not use the TCC interrupts FAULT1, FAULT0, FAULTB, FAULTA, DFS, ERR, or CNT to wake up the chip from standby mode.

3 – If the OVF flag in the INTFLAG register is already set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.
Errata reference: 12127
Fix/Workaround:
None

4 – Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these mode. Example: when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX won't work.
Errata reference: 14817
Fix/Workaround:
Basic capture mode must be set in lower channel and advance capture mode in upper channel.
Example: CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX
All capture will be done as expected.

5 – In RAMP 2 mode with Fault keep, qualified and restart:
If a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.
Errata reference: 13262
Fix/Workaround:
Avoid faults few cycles before the end or the beginning of a ramp.

6 – With blanking enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.
Errata reference: 12519
Fix/Workaround:
None

7 – In Dual slope mode a Retrigger Event does not clear the TCC counter.
Errata reference: 12354
Fix/Workaround:
None

8 – In two ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.
Errata reference: 12224
Fix/Workaround:
None

9 – If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.
Errata reference: 12107
Fix/Workaround:
None

This can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to NVM area.
Errata reference: 13134
Fix/Workaround:
Set MANW in the NVM.CTRLB to 1 at startup

2 – When external reset is active it causes a high leakage current on VDDIO.
Errata reference: 13446
Fix/Workaround:
Minimize the time external reset is active.

3 – When the part is secured and EEPROM emulation area configured to none, the CRC32 is not executed on the entire flash area but up to the on-chip flash size minus half a row.
Errata reference: 11988
Fix/Workaround:
When using CRC32 on a protected device with EEPROM emulation area configured to none, compute the reference CRC32 value to the full chip flash size minus half row.

40.1.4.10 I2S

1 – I2S RX serializer in LSBIT mode (SERCTRL.BITREV set) only works when the slot size is 32 bits.
Errata reference: 13320
Fix/Workaround:
In SERCTRL.SERMODE RX, SERCTRL.BITREV LSBIT must be used with CLKCTRL.SLOTSIZE 32.

40.1.4.11 SERCOM

1 – The I2C Slave SCL Low Extend Time-out (CTRLA.SEXTTOEN) and Master SCL Low Extend Time-out (CTRLA.MEXTTOEN) cannot be used if SCL Low Time-out (CTRLA.LOWTOUT) is disabled. When SCTRLA.LOWTOUT=0, the GCLK_SERCOM_SLOW is not requested.
Errata reference: 12003
Fix/Workaround:
To use the Master or Slave SCL low extend time-outs, enable the SCL Low Time-out (CTRLA.LOWTOUT=1).

2 – In USART autobaud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.
Errata reference: 13852
Fix/Workaround:
None

3 – If the SERCOM is enabled in SPI mode with SSL detection enabled (CTRLB.SSDE) and CTRLB.RXEN=1, an erroneous slave select low interrupt (INTFLAG.SSL) can be generated.
Errata reference: 13369
Fix/Workaround:
Enable the SERCOM first with CTRLB.RXEN=0. In a subsequent write, set CTRLB.RXEN=1.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.9	+/-1.2	+/-2.0	LSB
			V_{DD} = 3.6V	+/-0.9	+/-1.1	+/-1.5	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-1.1	+/-1.7	+/-3.0	
			V_{DD} = 3.6V	+/-1.0	+/-1.1	+/-1.6	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-1.1	+/-1.4	+/-2.5	
			V_{DD} = 3.6V	+/-1.0	+/-1.5	+/-1.8	
	Gain error	Ext. V_{REF}		+/-1.0	+/-5	+/-10	mV
	Offset error	Ext. V_{REF}		+/-2	+/-3	+/-8	mV

Table 44-23. Accuracy Characteristics(1)(Device Variant B)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
RES	Input resolution			-	-	10	Bits
INL	Integral non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	0.7	0.75	2.0	LSB
			V_{DD} = 3.6V	0.6	0.65	1.5	
		V_{REF} = V_{DDANA}	V_{DD} = 1.6V	0.6	0.85	2.0	
			V_{DD} = 3.6V	0.5	0.8	1.5	
		V_{REF}= INT1V	V_{DD} = 1.6V	0.5	0.75	1.5	
			V_{DD} = 3.6V	0.7	0.8	1.5	
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.3	+/-0.4	+/-1.0	LSB
			V_{DD} = 3.6V	+/-0.25	+/-0.4	+/-0.75	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-0.4	+/-0.55	+/-1.5	
			V_{DD} = 3.6V	+/-0.2	+/-0.3	+/-0.75	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-0.5	+/-0.7	+/-1.5	
			V_{DD} = 3.6V	+/-0.4	+/-0.7	+/-1.5	
	Gain error	Ext. V_{REF}		+/-0.5	+/-5	+/-12	mV
	Offset error	Ext. V_{REF}		+/-2	+/-1.5	+/-8	mV

1. All values measured using a conversion rate of 350ksps.