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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21e18a-au

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- Up to four compare channels with optional complementary output
- · Generation of synchronized pulse width modulation (PWM) pattern across port pins
- Deterministic fault protection, fast decay and configurable dead-time between complementary output
- Dithering that increase resolution with up to 5 bit and reduce quantization error
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Watchdog Timer (WDT)
- CRC-32 generator
- One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
 - Embedded host and device function
 - Eight endpoints
- Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
 - USART with full-duplex and single-wire half-duplex configuration
 - I2C up to 3.4MHz
 - SPI
 - LIN slave
- One two-channel Inter-IC Sound (I²S) interface
- One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
 - Differential and single-ended input
 - 1/2x to 16x programmable gain stage
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- 10-bit, 350ksps Digital-to-Analog Converter (DAC)
- Two Analog Comparators (AC) with window compare function
- Peripheral Touch Controller (PTC)
 - 256-Channel capacitive touch and proximity sensing
- I/O
 - Up to 52 programmable I/O pins
- Drop in compatible with SAM D20
- Packages
 - 64-pin TQFP, QFN, UFBGA
 - 48-pin TQFP, QFN, WLCSP
 - 32-pin TQFP, QFN, WLCSP
- Operating Voltage
 - 1.62V 3.63V

3.3 SAM D21J

Table 3-6. Device Variant A

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMD21J15A-AU	32K	4K	TQFP64	Tray
ATSAMD21J15A-AUT	-			Tape & Reel
ATSAMD21J15A-AF	-			Tray
ATSAMD21J15A-AFT	-			Tape & Reel
ATSAMD21J15A-MU	-		QFN64	Tray
ATSAMD21J15A-MUT	-			Tape & Reel
ATSAMD21J15A-MF	-			Tray
ATSAMD21J15A-MFT	-			Tape & Reel
ATSAMD21J16A-AU	64K	8K	TQFP64	Tray
ATSAMD21J16A-AUT	-			Tape & Reel
ATSAMD21J16A-AF				Tray
ATSAMD21J16A-AFT	-			Tape & Reel
ATSAMD21J16A-MU			QFN64	Tray
ATSAMD21J16A-MUT				Tape & Reel
ATSAMD21J16A-MF				Tray
ATSAMD21J16A-MFT				Tape & Reel
ATSAMD21J16A-CU			UFBGA64	Tray
ATSAMD21J16A-CUT				Tape & Reel
ATSAMD21J17A-AU	128K	16K	TQFP64	Tray
ATSAMD21J17A-AUT				Tape & Reel
ATSAMD21J17A-AF	-			Tray
ATSAMD21J17A-AFT	-			Tape & Reel
ATSAMD21J17A-MU	-		QFN64	Tray
ATSAMD21J17A-MUT	-			Tape & Reel
ATSAMD21J17A-MF	-			Tray
ATSAMD21J17A-MFT	-			Tape & Reel
ATSAMD21J17A-CU			UFBGA64	Tray
ATSAMD21J17A-CUT				Tape & Reel

Value	Description
0	The XOSC32K Ready interrupt is disabled.
1	The XOSC32K Ready interrupt is enabled, and an interrupt request will be generated when
	the XOSC32K Ready Interrupt flag is set.

Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the XOSC Ready Interrupt Enable bit, which enables the XOSC Ready interrupt.

Value	Description
0	The XOSC Ready interrupt is disabled.
1	The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the
	XOSC Ready Interrupt flag is set.

17.8.3 Interrupt Flag Status and Clear

Note: Depending on the fuse settings, various bits of the INTFLAG register can be set to one at startup. Therefore the user should clear those bits before using the corresponding interrupts.

 Name:
 INTFLAG

 Offset:
 0x08

 Reset:
 0x00000000

 Property:

Bit	31	30	29	28	27	26	25	24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
							DPLLLTO	DPLLLCKF
Access	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	DPLLLCKR				B33SRDY	BOD33DET	BOD33RDY	DFLLRCS
Access	R/W	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	DFLLLCKC	DFLLLCKF	DFLLOOB	DFLLRDY	OSC8MRDY	OSC32KRDY	XOSC32KRDY	XOSCRDY
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 17 – DPLLLTO: DPLL Lock Timeout

This flag is cleared by writing a one to it.

This flag is set on a zero-to-one transition of the DPLL Lock Timeout bit in the Status register (PCLKSR.DPLLLTO) and will generate an interrupt request if INTENSET.DPLLLTO is one.

Writing a zero to this bit has no effect.

Bit 12 – LBYPASS: Lock Bypass

Value	Description
0	Normal Mode: the CLK_FDPLL96M is turned off when lock signal is low.
1	Lock Bypass Mode: the CLK_FDPLL96M is always running, lock is irrelevant.

Bits 10:8 – LTIME[2:0]: Lock Time

These bits select Lock Timeout.

LTIME[2:0]	Name	Description
0x0	DEFAULT	No time-out
0x1-0x3		Reserved
0x4	8MS	Time-out if no lock within 8 ms
0x5	9MS	Time-out if no lock within 9 ms
0x6	10MS	Time-out if no lock within 10 ms
0x7	11MS	Time-out if no lock within 11 ms

Bits 5:4 – REFCLK[1:0]: Reference Clock Selection

These bits select the CLK_FDPLL96M_REF source.

REFCLK[1:0]	Name	Description
0x0	XOSC32	XOSC32 clock reference
0x1	XOSC	XOSC clock reference
0x2	GCLK_DPLL	GCLK_DPLL clock reference
0x3		Reserved

Bit 3 – WUF: Wake Up Fast

Value	Description
0	DPLL CK output is gated until complete startup time and lock time.
1	DPLL CK output is gated until startup time only.

Bit 2 – LPEN: Low-Power Enable

Value	Description
0	The time to digital converter is selected.
1	The time to digital converter is not selected, this will improve power consumption but increase the output jitter.

Bits 1:0 – FILTER[1:0]: Proportional Integral Filter Selection

These bits select the DPLL filter type.

FILTER[1:0]	Name	Description
0x0	DEFAULT	Default filter mode
0x1	LBFILT	Low bandwidth filter



Conditional Transfer

The event input is used to trigger a conditional transfer on peripherals with pending transfer requests. As example, this type of event can be used for peripheral-to-peripheral transfers, where one peripheral is the source of event and the second peripheral is the source of the trigger.

Each peripheral trigger is stored internally when the event is received. When the peripheral trigger is stored internally, the Channel Pending status bit is set (CHSTATUS.PEND), the respective Pending Channel n Bit in the Pending Channels register is set (PENDCH.PENDCHn), and the event is acknowledged. A software trigger will now trigger a transfer.

The figure below shows an example where conditional event is enabled with peripheral beat trigger requests.





Conditional Block Transfer

The event input is used to trigger a conditional block transfer on peripherals.

Before starting transfers within a block, an event must be received. When received, the event is acknowledged when the block transfer is completed. A software trigger will trigger a transfer.

The figure below shows an example where conditional event block transfer is started with peripheral beat trigger requests.

and 16x sample rate (CTRLA.SAMPR[0]=0).

During transmission, each low bit is transmitted as a high pulse. The pulse width is 3/16 of the baud rate period, as illustrated in the figure below.

Figure 26-10. IrDA Transmit Encoding



The reception decoder has two main functions.

The first is to synchronize the incoming data to the IrDA baud rate counter. Synchronization is performed at the start of each zero pulse.

The second main function is to decode incoming Rx data. If a pulse width meets the minimum length set by configuration (RXPL.RXPL), it is accepted. When the baud rate counter reaches its middle value (1/2 bit length), it is transferred to the receiver.

Note: Note that the polarity of the transmitter and receiver are opposite: During transmission, a '0' bit is transmitted as a '1' pulse. During reception, an accepted '0' pulse is received as a '0' bit.



26.6.3.4 Break Character Detection and Auto-Baud

Break character detection and auto-baud are available in this configuration:

- Auto-baud frame format (CTRLA.FORM = 0x04 or 0x05),
- Asynchronous mode (CTRLA.CMODE = 0),
- and 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1).

The auto-baud follows the LIN format. All LIN Frames start with a Break Field followed by a Sync Field. The USART uses a break detection threshold of greater than 11 nominal bit times at the configured baud rate. At any time, if more than 11 consecutive dominant bits are detected on the bus, the USART detects a Break Field. When a Break Field has been detected, the Receive Break interrupt flag (INTFLAG.RXBRK) is set and the USART expects the Sync Field character to be 0x55. This field is used to update the actual baud rate in order to stay synchronized. If the received Sync character is not 0x55, then the Inconsistent Sync Field error flag (STATUS.ISF) is set along with the Error interrupt flag (INTFLAG.ERROR), and the baud rate is unchanged.

Bit 31 30 29 28 27 26 25 24 Access Reset Bit 23 22 21 20 19 18 17 16 RXEN TXEN R/W R/W Access 0 Reset 0 Bit 15 13 12 11 10 9 8 14 PMODE ENC SFDE COLDEN R/W R/W R/W R/W Access Reset 0 0 0 0 Bit 7 6 5 4 3 2 0 1 SBMODE CHSIZE[2:0] R/W R/W R/W R/W Access 0 0 0 Reset 0

Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit 17 – RXEN: Receiver Enable

Writing '0' to this bit will disable the USART receiver. Disabling the receiver will flush the receive buffer and clear the FERR, PERR and BUFOVF bits in the STATUS register.

Writing '1' to CTRLB.RXEN when the USART is disabled will set CTRLB.RXEN immediately. When the USART is enabled, CTRLB.RXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the receiver is enabled. When the receiver is enabled, CTRLB.RXEN will read back as '1'.

Writing '1' to CTRLB.RXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.RXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The receiver is disabled or being enabled.
1	The receiver is enabled or will be enabled when the USART is enabled.

Bit 16 – TXEN: Transmitter Enable

Writing '0' to this bit will disable the USART transmitter. Disabling the transmitter will not become effective until ongoing and pending transmissions are completed.

Writing '1' to CTRLB.TXEN when the USART is disabled will set CTRLB.TXEN immediately. When the USART is enabled, CTRLB.TXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the transmitter is enabled. When the transmitter is enabled, CTRLB.TXEN will read back as '1'.

Writing '1' to CTRLB.TXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.TXEN will read back as '1'.

This bit is not enable-protected.

Bit	23	22	21	20	19	18	17	16
				ADDRM	ASK[7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
Access		•			•		•	
Reset								
Bit	7	6	5	4	3	2	1	0
				ADD	R[7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – ADDRMASK[7:0]: Address Mask

These bits hold the address mask when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

Bits 7:0 - ADDR[7:0]: Address

These bits hold the address when the transaction format with address is used (CTRLA.FORM, CTRLB.AMODE).

27.8.10 Data

 Name:
 DATA

 Offset:
 0x28

 Reset:
 0x0000

 Property:

Bit	15	14	13	12	11	10	9	8
								DATA[8:8]
Access								R/W
Reset								0
Bit	7	6	5	4	3	2	1	0
				DAT	A[7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 - DATA[8:0]: Data

Reading these bits will return the contents of the receive data buffer. The register should be read only when the Receive Complete Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set.

Writing these bits will write the transmit data buffer. This register should be written only when the Data Register Empty Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is set.

27.8.11 Debug Control

Name:DBGCTRLOffset:0x30Reset:0x00Property:PAC Write-Protection



Bit 0 – DBGSTOP: Debug Stop Mode

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external
	debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.



28.6.2 Basic Operation

28.6.2.1 Initialization

The following registers are enable-protected, meaning they can be written only when the I²C interface is disabled (CTRLA.ENABLE is '0'):

- Control A register (CTRLA), except Enable (CTRLA.ENABLE) and Software Reset (CTRLA.SWRST) bits
- Control B register (CTRLB), except Acknowledge Action (CTRLB.ACKACT) and Command (CTRLB.CMD) bits
- Baud register (BAUD)
- Address register (ADDR) in slave operation.

When the I²C is enabled or is being enabled (CTRLA.ENABLE=1), writing to these registers will be discarded. If the I²C is being disabled, writing to these registers will be completed after the disabling.

Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the I^2C is enabled it must be configured as outlined by the following steps:

- 1. Select I²C Master or Slave mode by writing 0x4 or 0x5 to the Operating Mode bits in the CTRLA register (CTRLA.MODE).
- 2. If desired, select the SDA Hold Time value in the CTRLA register (CTRLA.SDAHOLD).
- 3. If desired, enable smart operation by setting the Smart Mode Enable bit in the CTRLB register (CTRLB.SMEN).
- 4. If desired, enable SCL low time-out by setting the SCL Low Time-Out bit in the Control A register (CTRLA.LOWTOUT).
- 5. In Master mode:
 - 5.1. Select the inactive bus time-out in the Inactive Time-Out bit group in the CTRLA register (CTRLA.INACTOUT).
 - 5.2. Write the Baud Rate register (BAUD) to generate the desired baud rate.

In Slave mode:

31. TCC – Timer/Counter for Control Applications

31.1 Overview

The device provides three instances of the Timer/Counter for Control applications (TCC) peripheral, TCC[2:0].

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation such as frequency generation and pulse-width modulation.

Waveform extensions are intended for motor control, ballast, LED, H-bridge, power converters, and other types of power control applications. They allow for low- and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut down of external drivers.

Figure 31-1 shows all features in TCC.

Related Links

TCC Configurations

31.2 Features

- Up to four compare/capture channels (CC) with:
 - Double buffered period setting
 - Double buffered compare or capture channel
 - Circular buffer on period and compare channel registers
- Waveform generation:
 - Frequency generation
 - Single-slope pulse-width modulation (PWM)
 - Dual-slope pulse-width modulation with half-cycle reload capability
- Input capture:
 - Event capture
 - Frequency capture
 - Pulse-width capture
- Waveform extensions:
 - Configurable distribution of compare channels outputs across port pins
 - Low- and high-side output with programmable dead-time insertion
 - Waveform swap option with double buffer support
 - Pattern generation with double buffer support
 - Dithering support
- Fault protection for safe disabling of drivers:
 - Two recoverable fault sources
 - Two non-recoverable fault sources
 - Debugger can be source of non-recoverable fault

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

31.8.22 Channel x Compare/Capture Buffer Value

CCBx is copied into CCx at TCC update time

Name: CCBn

Offset: 0x70 + n*0x04 [n=0..3]

Reset: 0x0000000

Property: Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
ſ								
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Γ				CCB	17:10]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				CCB	[9:2]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Γ	CCB[1:0]				DITHE	RB[5:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CCB[17:0]: Channel x Compare/Capture Buffer Value

These bits hold the value of the Channel x Compare/Capture Buffer Value register. The register serves as the buffer for the associated compare or capture registers (CCx). Accessing this register using the CPU or DMA will affect the corresponding CCBVx status bit.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4

Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
			STALL	RXSTP		TRFAIL		TRCPT
Access			R/W	R/W		R/W		R/W
Reset			0	0		0		0

Bit 5 – STALL: Transmit STALL x Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Transmit Stall x Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Transmit Stall x interrupt is disabled.
1	The Transmit Stall x interrupt is enabled and an interrupt request will be generated when the
	Transmit Stall x Interrupt Flag is set.

Bit 4 – RXSTP: Received Setup Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Received Setup Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Received Setup interrupt is disabled.
1	The Received Setup interrupt is enabled and an interrupt request will be generated when the
	Received Setup Interrupt Flag is set.

Bit 2 – TRFAIL: Transfer Fail x Interrupt Enable

The user should look into the descriptor table status located in ram to be informed about the error condition : ERRORFLOW, CRC.

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Transfer Fail x Interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Transfer Fail bank x interrupt is disabled.
1	The Transfer Fail bank x interrupt is enabled and an interrupt request will be generated when
	the Transfer Fail x Interrupt Flag is set.

Bit 0 – TRCPT: Transfer Complete x interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Transfer Complete x interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Transfer Complete bank x interrupt is disabled.
1	The Transfer Complete bank x interrupt is enabled and an interrupt request will be generated
	when the Transfer Complete x Interrupt Flag is set.

33.8.6 Window Monitor Control

Name:WINCTRLOffset:0x08Reset:0x00Property:Write-Protected, Write-Synchronized



Bits 2:0 – WINMODE[2:0]: Window Monitor Mode

These bits enable and define the window monitor mode.

WINMODE[2:0]	Name	Description
0x0	DISABLE	No window mode (default)
0x1	MODE1	Mode 1: RESULT > WINLT
0x2	MODE2	Mode 2: RESULT < WINUT
0x3	MODE3	Mode 3: WINLT < RESULT < WINUT
0x4	MODE4	Mode 4: !(WINLT < RESULT < WINUT)
0x5-0x7		Reserved

33.8.7 Software Trigger

Name:SWTRIGOffset:0x0CReset:0x00Property:Write-Protected, Write-Synchronized



Bit 1 – START: ADC Start Conversion

Writing this bit to zero will have no effect.

Value	Description
0	The ADC will not start a conversion.
1	The ADC will start a conversion. The bit is cleared by hardware when the conversion has
	started. Setting this bit when it is already set has no effect.

Bit 0 – FLUSH: ADC Conversion Flush

After the flush, the ADC will resume where it left off; i.e., if a conversion was pending, the ADC will start a new conversion.

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Value	Description
0	The Synchronization Ready interrupt is disabled.
1	The Synchronization Ready interrupt is enabled, and an interrupt request will be generated
	when the Synchronization Ready interrupt flag is set.

Bit 2 – WINMON: Window Monitor Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Window Monitor Interrupt Enable bit and the corresponding interrupt request.

Value	Description
0	The window monitor interrupt is disabled.
1	The window monitor interrupt is enabled, and an interrupt request will be generated when the
	Window Monitor interrupt flag is set.

Bit 1 – OVERRUN: Overrun Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Overrun Interrupt Enable bit and the corresponding interrupt request.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled, and an interrupt request will be generated when the
	Overrun interrupt flag is set.

Bit 0 – RESRDY: Result Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Result Ready Interrupt Enable bit and the corresponding interrupt request.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled, and an interrupt request will be generated when the
	Result Ready interrupt flag is set.

33.8.11 Interrupt Enable Set

Name:INTENSETOffset:0x17Reset:0x00Property:Write-Protected

Bit	7	6	5	4	3	2	1	0
					SYNCRDY	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SYNCRDY: Synchronization Ready Interrupt Enable

Writing a zero to this bit has no effect.

Symbol	Description	Max.	Units
f _{GCLK_EVSYS_CHANNEL_7}	EVSYS channel 7 input clock frequency	48	MHz
f _{GCLK_EVSYS_CHANNEL_8}	EVSYS channel 8 input clock frequency	48	MHz
f _{GCLK_EVSYS_CHANNEL_9}	EVSYS channel 9 input clock frequency	48	MHz
f _{GCLK_EVSYS_CHANNEL_10}	EVSYS channel 10 input clock frequency	48	MHz
f _{GCLK_EVSYS_CHANNEL_11}	EVSYS channel 11 input clock frequency	48	MHz
f _{GCLK_SERCOMx_SLOW}	Common SERCOM slow input clock frequency	48	MHz
f _{GCLK_SERCOM0_CORE}	SERCOM0 input clock frequency	48	MHz
f _{GCLK_SERCOM1_CORE}	SERCOM1 input clock frequency	48	MHz
f _{GCLK_SERCOM2_CORE}	SERCOM2 input clock frequency	48	MHz
f _{GCLK_SERCOM3_CORE}	SERCOM3 input clock frequency	48	MHz
f _{GCLK_SERCOM4_CORE}	SERCOM4 input clock frequency	48	MHz
f _{GCLK_SERCOM5_CORE}	SERCOM5 input clock frequency	48	MHz
fGCLK_TCC0, GCLK_TCC1	TCC0,TCC1 input clock frequency	96	MHz
fGCLK_TCC2, GCLK_TC3	TCC2,TC3 input clock frequency	96	MHz
fGCLK_TC4, GCLK_TC5	TC4,TC5 input clock frequency	48	MHz
fGCLK_TC6, GCLK_TC7	TC6,TC7 input clock frequency	48	MHz
f _{GCLK_ADC}	ADC input clock frequency	48	MHz
f _{GCLK_AC_DIG}	AC digital input clock frequency	48	MHz
f _{GCLK_AC_ANA}	AC analog input clock frequency	64	KHz
f _{GCLK_DAC}	DAC input clock frequency	350	KHz
f _{GCLK_PTC}	PTC input clock frequency	48	MHz
f _{GCLK_I2S_0}	I2S serializer 0 input clock frequency	13	MHz
f _{GCLK_I2S_1}	I2S serializer 1 input clock frequency	13	MHz

37.6 Power Consumption

The values in this section are measured values of power consumption under the following conditions, except where noted:

- Operating conditions
 - V_{VDDIN} = 3.3 V
 - VDDIN = 1.8V, CPU is running on Flash with three wait states
- Wake up time from sleep mode is measured from the edge of the wakeup signal to the execution of the first instruction fetched in flash.
- Oscillators
 - XOSC (crystal oscillator) stopped
 - XOSC32K (32 kHz crystal oscillator) running with external 32kHz crystal

	10 – When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected. Errata reference: 12477 Fix/Workaround: None.
	 11 – TCC fault filtering on inverted fault is not working. Errata reference: 12512 Fix/Workaround: Use only non-inverted faults.
	12 – When waking up from the STANDBY power save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to 1. Errata reference: 12227 Fix/Workaround: After waking up from STANDBY power save mode, perform a software reset
	of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits
	13 – When the Peripheral Access Controller (PAC) protection is enabled, writing to WAVE or WAVEB registers will not cause a hardware exception. Errata reference: 11468 Fix/Workaround: None
	14 – If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register. Errata reference: 12155 Fix/Workaround: None
40.1.1.13 USB	
	1 – The FLENC register negative sign management is not correct. Errata reference: 11472 Fix/Workaround:
	The following rule must be used for negative values: - FLENC 8h is equal to 0 decimal.
	- FLENC 9h to Fh are equal to -1 to -7 decimal instead of -7 to -1.
40.1.1.14 PIC	1 – WCOMP interrupt flag is not stable. The WCOMP interrupt flag will
	not always be set as described in the datasheet. Errata reference: 12860
	Fix/Workaround: Do not use the WCOMP interrupt. Use the WCOMP event.

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

5 – In I2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

Errata reference: 13574

Fix/Workaround:

Write CTRLB.ACKACT to 0 using the following sequence: // If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = 0;

// Re-enable interrupts if applicable.

Write CTRLB.ACKACT to 1 using the following sequence:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit position.

Code replacements examples:

Current:

SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;

Change to:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Current:

SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT; Change to:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = 0;

// Re-enable interrupts if applicable.

Current:

/* ACK or NACK address */

SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);

Change to:

// CMD=0x3 clears all interrupts, so to keep the result similar,

// PREC is cleared if it was set.

if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg =
SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM I2CS INTFLAG AMATCH;

6 – PA24 and PA25 cannot be used as input when configured as GPIO with continuous sampling (cannot be read by PORT). Errata reference: 12005

Fix/Workaround:

- Use PA24 and PA25 for peripherals or only as output pins.

- Or configure PA31 to PA24 for on-demand sampling (CTRL[31:24] all zeroes) and access the IN register through the APB (not the IOBUS), to allow waiting for on-demand sampling.

7 – Rx serializer in the RIGHT Data Slot Formatting Adjust mode (SERCTRL.SLOTADJ clear) does not work when the slot size is not 32 bits.

Errata reference: 13411

Fix/Workaround:

In SERCTRL.SERMODE RX, SERCTRL.SLOTADJ RIGHT must be used with CLKCTRL.SLOTSIZE 32.

8 – The SYSTICK calibration value is incorrect.

Errata reference: 14154

Fix/Workaround:

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

9 – While the internal startup is not completed, PA07 pin is driven low by the chip. Then as all the other pins it is configured as an High Impedance pin.

Errata reference: 12118 Fix/Workaround:

None

10 – Pulldown functionality is not available on GPIO pin PA24 and PA25 Errata reference: 13883

Fix/Workaround:

None

11 – The voltage regulator in low power mode is not functional at temperatures above 85C.

Errata reference: 12291

Fix/Workaround:

Enable normal mode on the voltage regulator in standby sleep mode. Example code:

// Set the voltage regulator in normal mode configuration in standby sleep mode

SYSCTRL->VREG.bit.RUNSTDBY = 1;

12 – If the external XOSC32K is broken, neither the external pin RST nor the GCLK software reset can reset the GCLK generators using XOSC32K as source clock.

	I/O Pin Configuration: Removed reference to "open-drain". Access for DRVSTR bit in Pin Configuration n register (PINCFGn.DRVCTR) updated from W to R/W.		
SYSCTRL – System Controller:			
	Removed references to XOSC32K and OSC32 1kHz clock output option: - XOSC32K: 32kHz External Crystal Oscillator (XOSC32K) Operation		
	- OSC32K: 32kHz Internal Oscillator (OSC32K) Operation		
	1kHz Output Enable (EN1K) bit set as reserved bit:		
	- Bit 4 in XOSC32K		
	- Bit 3 in OSC32K		
Electrical Ch	aracteristics:		
	Brown-Out Detectors Characteristics: Added Figure 37-3 and Figure 37-4 and updated conditions in Table 37-20 and Table 37-21.		
Packaging Ir	iformation:		
	Added 64-ball UFBGA and 45-ball WLCSP package drawings.		
Schematic C	hecklist		
	Updated description in Unused or Unconnected Pins.		
Errata:			
	Device Variant A: - Updated errata for revision A: Added Errata Reference 12291, 13507, 13574.		
	- Updated errata for revision B: Added Errata Reference 12291, 13507, 13574.		
	- Updated errata for revision C: Added Errata Reference 12291, 13507, 13574, 13951.		
	- Added errata for revision D.		
	Device Variant B:		
	- Added errata for revision E (Only available for SAMD21x15/16).		
Appendix A.	Electrical Characteristics at 125°C:		
	Electrical characteristics for 125°C added.		

43.13 Rev. D - 09/2014

Block Diagra	Block Diagram		
	NVM Controller bus connection changed from Master to Slave.		
Clock System			
	Register Synchronization updated by splitting the section into Common Synchronizer Register Synchronization and Distributed Synchronizer Register Synchronization.		
Electrical Characteristics			