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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

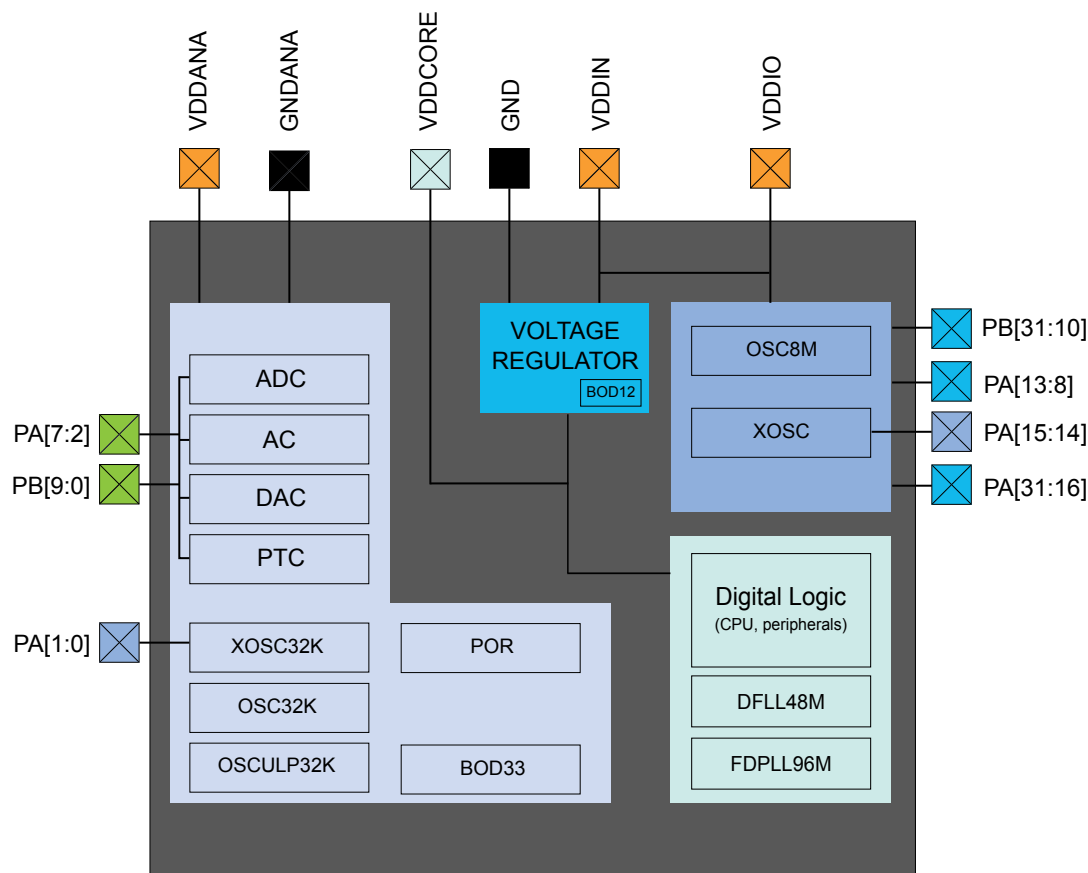
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g15b-mf">https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g15b-mf</a>

## 8. Power Supply and Start-Up Considerations

### 8.1 Power Domain Overview



### 8.2 Power Supply Considerations

#### 8.2.1 Power Supplies

The device has several different power supply pins:

- VDDIO: Powers I/O lines, OSC8M and XOSC. Voltage is 1.62V to 3.63V.
- VDDIN: Powers I/O lines and the internal regulator. Voltage is 1.62V to 3.63V.
- VDDANA: Powers I/O lines and the ADC, AC, DAC, PTC, OSCULP32K, OSC32K, XOSC32K. Voltage is 1.62V to 3.63V.
- VDDCORE: Internal regulated voltage output. Powers the core, memories, peripherals, FDPLL96M, and DFLL48M. Voltage is 1.2V.

The same voltage must be applied to both VDDIN, VDDIO and VDDANA. This common voltage is referred to as  $V_{DD}$  in the datasheet.

The ground pins, GND, are common to VDDCORE, VDDIO and VDDIN. The ground pin for VDDANA is GNDANA.

command is ongoing, other commands are discarded until the current operation is completed. Hence, the user must wait for the STATUSA.DONE bit to be set prior to issuing another one.

## 13.11.2 Basic Operation

### 13.11.2.1 Initialization

The module is enabled by enabling its clocks. For more details, refer to [Clocks](#). The DSU registers can be PAC write-protected.

#### Related Links

[PAC - Peripheral Access Controller](#)

### 13.11.2.2 Operation From a Debug Adapter

Debug adapters should access the DSU registers in the external address range 0x100 – 0x2000. If the device is protected by the NVMCTRL security bit, accessing the first 0x100 bytes causes the system to return an error. Refer to [Intellectual Property Protection](#).

#### Related Links

[NVMCTRL – Non-Volatile Memory Controller Security Bit](#)

### 13.11.2.3 Operation From the CPU

There are no restrictions when accessing DSU registers from the CPU. However, the user should access DSU registers in the internal address range (0x0 – 0x100) to avoid external security restrictions. Refer to [Intellectual Property Protection](#).

## 13.11.3 32-bit Cyclic Redundancy Check CRC32

The DSU unit provides support for calculating a cyclic redundancy check (CRC32) value for a memory area (including Flash and AHB RAM).

When the CRC32 command is issued from:

- The internal range, the CRC32 can be operated at any memory location
- The external range, the CRC32 operation is restricted; DATA, ADDR, and LENGTH values are forced (see below)

**Table 13-3. AMOD Bit Descriptions when Operating CRC32**

AMOD[1:0]	Short name	External range restrictions
0	ARRAY	CRC32 is restricted to the full Flash array area (EEPROM emulation area not included) DATA forced to 0xFFFFFFFF before calculation (no seed)
1	EEPROM	CRC32 of the whole EEPROM emulation area DATA forced to 0xFFFFFFFF before calculation (no seed)
2-3	Reserved	

The algorithm employed is the industry standard CRC32 algorithm using the generator polynomial 0xEDB88320 (reversed representation).

### 13.11.3.1 Starting CRC32 Calculation

CRC32 calculation for a memory range is started after writing the start address into the Address register (ADDR) and the size of the memory range into the Length register (LENGTH). Both must be word-aligned.

- 32KHz to 2MHz input reference clock frequency range
  - Three possible sources for the reference clock
  - Adjustable proportional integral controller
  - Fractional part used to achieve 1/16th of reference clock step
- 3.3V Brown-Out Detector (BOD33)
  - Programmable threshold
  - Threshold value loaded from Flash User Calibration at startup
  - Triggers resets or interrupts
  - Operating modes:
    - Continuous mode
    - Sampled mode for low power applications (programmable refresh frequency)
  - Hysteresis
- Internal Voltage Regulator system (VREG)
  - Operating modes:
    - Normal mode
    - Low-power mode
  - With an internal non-configurable Brown-out detector (BOD12)
- 1.2V Brown-Out Detector (BOD12)
  - Programmable threshold
  - Threshold value loaded from Flash User Calibration at start-up
  - Triggers resets or interrupts
  - Operating modes:
    - Continuous mode
    - Sampled mode for low power applications (programmable refresh frequency)
  - Hysteresis
- Voltage Reference System (VREF)
  - Bandgap voltage generator with programmable calibration value
  - Temperature sensor
  - Bandgap calibration value loaded from Flash Factory Calibration at start-up

## 19. RTC – Real-Time Counter

### 19.1 Overview

The Real-Time Counter (RTC) is a 32-bit counter with a 10-bit programmable prescaler that typically runs continuously to keep track of time. The RTC can wake up the device from sleep modes using the alarm/compare wake up, periodic wake up, or overflow wake up mechanisms

The RTC is typically clocked by the 1.024kHz output from the 32.768kHz High-Accuracy Internal Crystal Oscillator (OSC32K) and this is the configuration optimized for the lowest power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from other sources, selectable through the Generic Clock module (GCLK).

The RTC can generate periodic peripheral events from outputs of the prescaler, as well as alarm/compare interrupts and peripheral events, which can trigger at any counter value. Additionally, the timer can trigger an overflow interrupt and peripheral event, and can be reset on the occurrence of an alarm/compare match. This allows periodic interrupts and peripheral events at very long and accurate intervals.

The 10-bit programmable prescaler can scale down the clock source. By this, a wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the minimum counter tick interval is 30.5 $\mu$ s, and time-out periods can range up to 36 hours. For a counter tick interval of 1s, the maximum time-out period is more than 136 years.

### 19.2 Features

- 32-bit counter with 10-bit prescaler
- Multiple clock sources
- 32-bit or 16-bit Counter mode
  - One 32-bit or two 16-bit compare values
- Clock/Calendar mode
  - Time in seconds, minutes and hours (12/24)
  - Date in day of month, month and year
  - Leap year correction
- Digital prescaler correction/tuning for increased accuracy
- Overflow, alarm/compare match and prescaler interrupts and events
  - Optional clear on alarm/compare match

- Read Request register (READREQ)
- Status register (STATUS)
- Debug register (DBGCTRL)

**Note:** Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

### 19.5.9 Analog Connections

A 32.768kHz crystal can be connected to the XIN32 and XOUT32 pins, along with any required load capacitors. For details on recommended crystal characteristics and load capacitors, refer to *Electrical Characteristics* for details.

#### Related Links

[Electrical Characteristics](#)

## 19.6 Functional Description

### 19.6.1 Principle of Operation

The RTC keeps track of time in the system and enables periodic events, as well as interrupts and events at a specified time. The RTC consists of a 10-bit prescaler that feeds a 32-bit counter. The actual format of the 32-bit counter depends on the RTC operating mode.

The RTC can function in one of these modes:

- Mode 0 - COUNT32: RTC serves as 32-bit counter
- Mode 1 - COUNT16: RTC serves as 16-bit counter
- Mode 2 - CLOCK: RTC serves as clock/calendar with alarm functionality

### 19.6.2 Basic Operation

#### 19.6.2.1 Initialization

The following bits are enable-protected, meaning that they can only be written when the RTC is disabled (CTRL.ENABLE=0):

- Operating Mode bits in the Control register (CTRL.MODE)
- Prescaler bits in the Control register (CTRL.PRESCALER)
- Clear on Match bit in the Control register (CTRL.MATCHCLR)
- Clock Representation bit in the Control register (CTRL.CLKREP)

The following register is enable-protected:

- Event Control register (EVCTRL)

Any writes to these bits or registers when the RTC is enabled or being enabled (CTRL.ENABLE=1) will be discarded. Writes to these bits or registers while the RTC is being disabled will be completed after the disabling is complete.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

Before the RTC is enabled, it must be configured, as outlined by the following steps:

1. RTC operation mode must be selected by writing the Operating Mode bit group in the Control register (CTRL.MODE)

Action	CHCTRLB.EVACT	CHCTRLB.TRGSRC
Conditional Transfer on Strobe	TRIG	any peripheral
Conditional Transfer	CTRIG	
Conditional Block Transfer	CBLOCK	
Channel Suspend	SUSPEND	
Channel Resume	RESUME	
Skip Next Block Suspend	SSKIP	

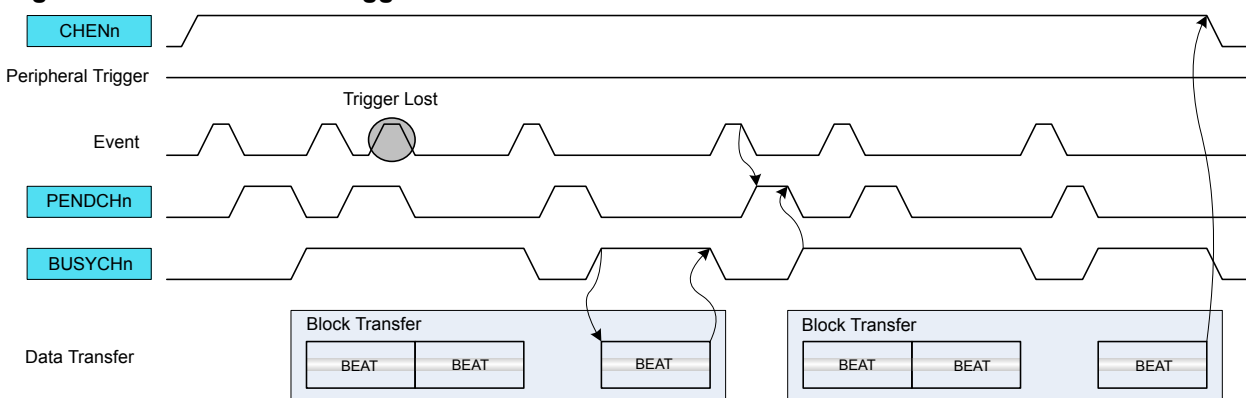
## Normal Transfer

The event input is used to trigger a beat or burst transfer on peripherals.

The event is acknowledged as soon as the event is received. When received, both the Channel Pending status bit in the Channel Status register ([CHSTATUS.PEND](#)) and the corresponding Channel n bit in the Pending Channels register ([PENDCH.PENDCHn](#)) are set. If the event is received while the channel is pending, the event trigger is lost.

The figure below shows an example where beat transfers are enabled by internal events.

**Figure 20-11. Beat Event Trigger Action**



## Conditional Transfer on Strobe

The event input is used to trigger a transfer on peripherals with pending transfer requests. This event action is intended to be used with peripheral triggers, e.g. for timed communication protocols or periodic transfers between peripherals: only when the peripheral trigger coincides with the occurrence of a (possibly cyclic) event the transfer is issued.

The event is acknowledged as soon as the event is received. The peripheral trigger request is stored internally when the previous trigger action is completed (i.e. the channel is not pending) and when an active event is received. If the peripheral trigger is active, the DMA will wait for an event before the peripheral trigger is internally registered. When both event and peripheral transfer trigger are active, both [CHSTATUS.PEND](#) and [PENDCH.PENDCHn](#) are set. A software trigger will now trigger a transfer.

The figure below shows an example where the peripheral beat transfer is started by a conditional strobe event action.

## 22.5.6 Analog Connections

Not applicable.

## 22.6 Functional Description

### 22.6.1 Principle of Operation

The NVM Controller is a slave on the AHB and APB buses. It responds to commands, read requests and write requests, based on user configuration.

#### 22.6.1.1 Initialization

After power up, the NVM Controller goes through a power-up sequence. During this time, access to the NVM Controller from the AHB bus is halted. Upon power-up completion, the NVM Controller is operational without any need for user configuration.

### 22.6.2 Memory Organization

Refer to the Physical Memory Map for memory sizes and addresses for each device.

The NVM is organized into rows, where each row contains four pages, as shown in the NVM Row Organization figure. The NVM has a row-erase granularity, while the write granularity is by page. In other words, a single row erase will erase all four pages in the row, while four write operations are used to write the complete row.

**Figure 22-2. NVM Row Organization**

Row n	Page (n*4) + 3	Page (n*4) + 2	Page (n*4) + 1	Page (n*4) + 0
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The NVM block contains a calibration and auxiliary space plus a dedicated EEPROM emulation space that are memory mapped. Refer to the NVM Organization figure below for details.

The calibration and auxiliary space contains factory calibration and system configuration information. These spaces can be read from the AHB bus in the same way as the main NVM main address space.

In addition, a boot loader section can be allocated at the beginning of the main array, and an EEPROM section can be allocated at the end of the NVM main address space.



## 28.8.8 Address

**Name:** ADDR

**Offset:** 0x24

**Reset:** 0x00000000

**Property:** PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
						ADDRMASK[9:7]		
Access						R/W	R/W	R/W
Reset						0	0	0
Bit	23	22	21	20	19	18	17	16
	ADDRMASK[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8
	TENBITEN					ADDR[9:7]		
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0
Bit	7	6	5	4	3	2	1	0
	ADDR[6:0]							GENCEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

### Bits 26:17 – ADDRMASK[9:0]: Address Mask

These bits act as a second address match register, an address mask register or the lower limit of an address range, depending on the CTRLB.AMODE setting.

### Bit 15 – TENBITEN: Ten Bit Addressing Enable

Value	Description
0	10-bit address recognition disabled.
1	10-bit address recognition enabled.

### Bits 10:1 – ADDR[9:0]: Address

These bits contain the I<sup>2</sup>C slave address used by the slave address match logic to determine if a master has addressed the slave.

When using 7-bit addressing, the slave address is represented by ADDR[6:0].

When using 10-bit addressing (ADDR.TENBITEN=1), the slave address is represented by ADDR[9:0].

When the address match logic detects a match, INTFLAG.AMATCH is set and STATUS.DIR is updated to indicate whether it is a read or a write transaction.

### Bit 0 – GENCEN: General Call Address Enable

A general call address is an address consisting of all-zeroes, including the direction bit (master write).

## 32-bit ARM-Based Microcontrollers

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

### Bit 0 – DIR: Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

### 30.8.5 Control C

**Name:** CTRLC

**Offset:** 0x06

**Reset:** 0x00

**Property:** PAC Write-Protection, Read-synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
			CPTEN1	CPTEN0			INVEN1	INVEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

### Bits 5,4 – CPTENx: Capture Channel x Enable

These bits are used to select the capture or compare operation on channel x.

Writing a '1' to CPTENx enables capture on channel x.

Writing a '0' to CPTENx disables capture on channel x.

### Bits 1,0 – INVENx: Waveform Output x Inversion Enable

These bits are used to select inversion on the output of channel x.

Writing a '1' to INVENx inverts output from WO[x].

Writing a '0' to INVENx disables inversion of output from WO[x].

### 30.8.6 Debug Control

**Name:** DBGCTRL

**Offset:** 0x08

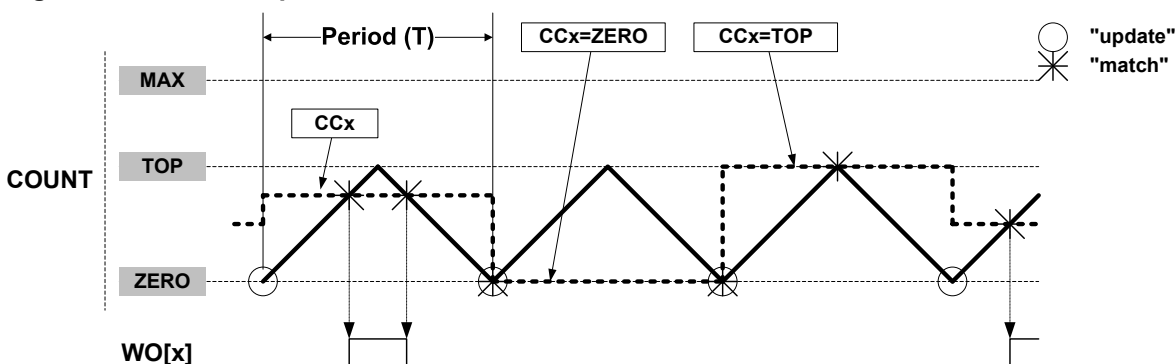
**Reset:** 0x00

**Property:** PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

In DSBOTH operation, a second update time occurs on TOP when circular buffer is enabled.

**Figure 31-7. Dual-Slope Pulse Width Modulation**



Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM ( $R_{PWM\_DS}$ ):

$$R_{PWM\_DS} = \frac{\log(PER+1)}{\log(2)}.$$

The PWM frequency  $f_{PWM\_DS}$  depends on the period setting (TOP) and the peripheral clock frequency  $f_{GCLK\_TCC}$ , and can be calculated by the following equation:

$$f_{PWM\_DS} = \frac{f_{GCLK\_TCC}}{2N \cdot PER}$$

$N$  represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency ( $f_{GCLK\_TCC}$ ) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width ( $P_{PWM\_DS}$ ) depends on the compare channel (CCx) register value and the peripheral clock frequency ( $f_{GCLK\_TCC}$ ), and can be calculated by the following equation:

$$P_{PWM\_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK\_TCC}}$$

$N$  represents the prescaler divider used.

**Note:** In DSTOP, DSBOTTOM and DSBOTH operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB]=0, falling if CCx[MSB]=1.)

## Related Links

[Circular Buffer](#)

## Dual-Slope Critical PWM Generation

### Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC\_NUM/2) control the generated waveform output edge during down-counting.

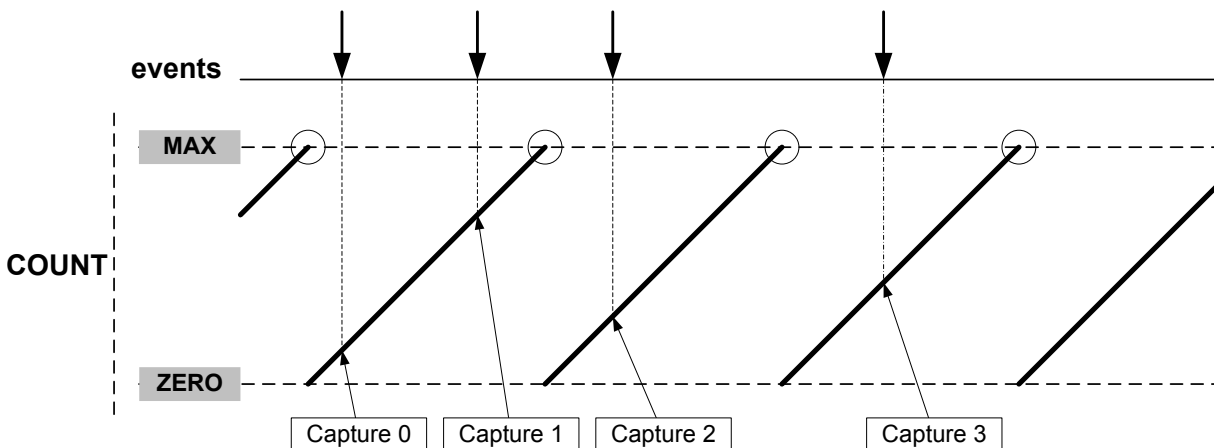
## 31.6.2.7 Capture Operations

To enable and use capture operations, the Match or Capture Channel x Event Input Enable bit in the Event Control register (EVCTRL.MCEIx) must be written to '1'. The capture channels to be used must also be enabled in the Capture Channel x Enable bit in the Control A register (CTRLA.CPTENx) before capturing can be performed.

### Event Capture Action

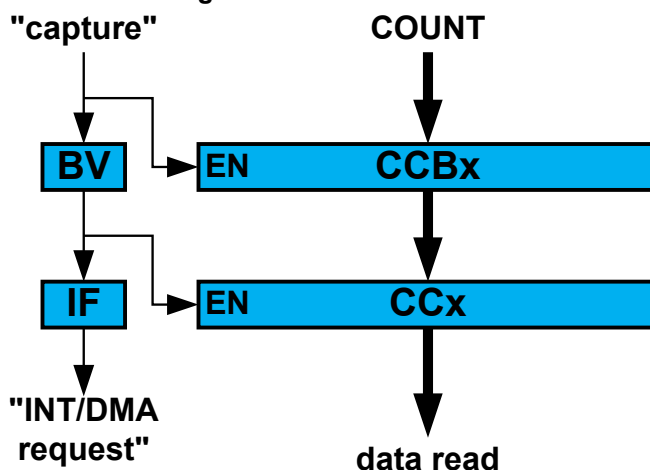
The compare/capture channels can be used as input capture channels to capture events from the Event System, and give them a timestamp. The following figure shows four capture events for one capture channel.

**Figure 31-14. Input Capture Timing**



For input capture, the buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBx is transferred to CCx. The buffer valid flag is passed to set the CCx interrupt flag (IF) and generate the optional interrupt, event or DMA request. CCBx register value can't be read, all captured data must be read from CCx register.

**Figure 31-15. Capture Double Buffering**



The TCC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Buffer Valid flag (STATUS.CCBV) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

### Period and Pulse-Width (PPW) Capture Action

relative local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected. DERIV0 is equivalent to an OR function of (LOCMIN, LOCMAx).

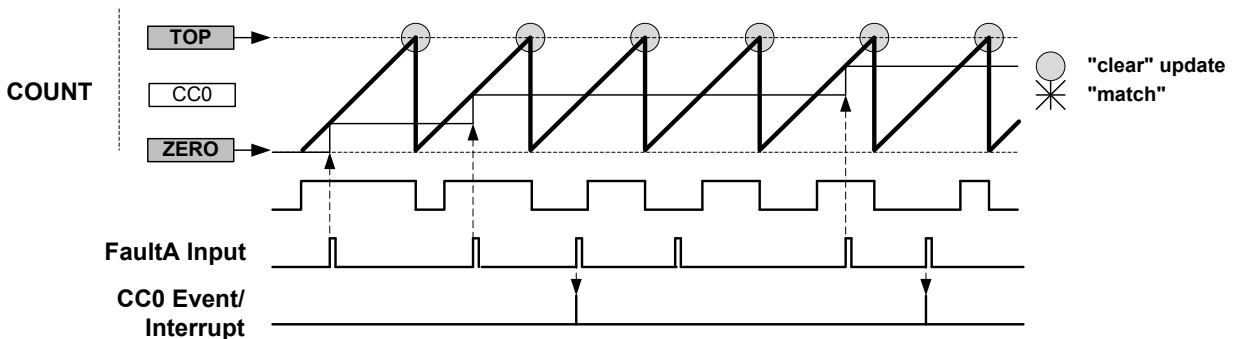
In CAPT operation, capture is performed on each capture event. The MCx interrupt flag is set on each new capture.

In CAPTMIN and CAPTMAX operation, capture is performed only when on capture event time, the counter value is lower (for CAPTMIN) or upper (for CAPMAX) than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is upper or equal (for CAPTMIN) or lower or equal (for CAPTMAX) to the value captured on the previous event. So interrupt flag is set when a new absolute local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected.

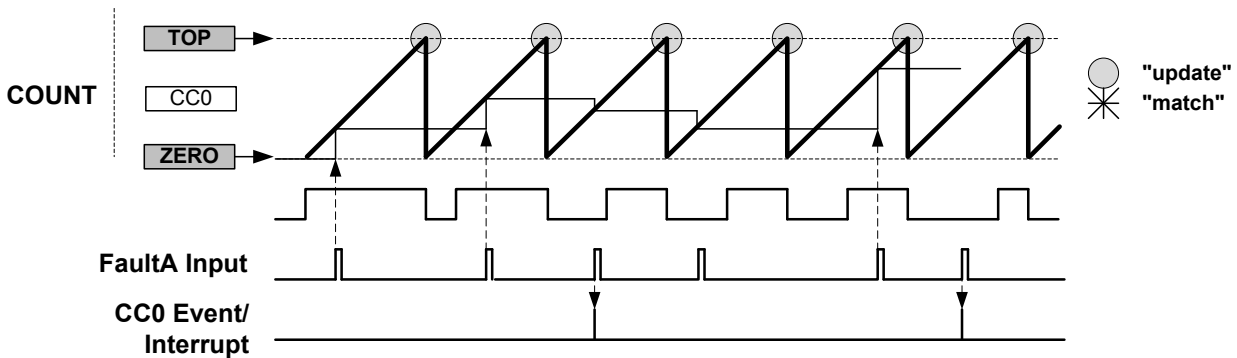
## Interrupt Generation

In CAPT mode, an interrupt is generated on each filtered Fault n and each dedicated CCx channel capture counter value. In other modes, an interrupt is only generated on an extreme captured value.

**Figure 31-26. Capture Action “CAPTMAX”**



**Figure 31-27. Capture Action “DERIV0”**



**Hardware Halt Action** This is configured by writing 0x1 to the Fault n Halt mode bits in the Recoverable Fault n Configuration register (FCTRLn.HALT). When enabled, the timer/counter is halted and the cycle is extended as long as the corresponding fault is present.

The next figure ('Waveform Generation with Halt and Restart Actions') shows an example where both restart action and hardware halt action are enabled for Fault A. The compare channel 0 output is clamped to inactive level as long as the timer/counter is halted. The timer/counter resumes the counting operation as soon as the fault condition is no longer present. As the restart action is enabled in this example, the timer/counter is restarted after the fault condition is no longer present.

- Decrement the counter on event
- Period and pulse width capture
- Non-recoverable fault

The TCC can take the following actions on counter Event 0 (TCCx EV0):

- Counter re-trigger
- Count on event (increment or decrement, depending on counter direction)
- Counter start - start counting on the event rising edge. Further events will not restart the counter; the counter will keep on counting using prescaled GCLK\_TCCx, until it reaches TOP or ZERO, depending on the direction.
- Counter increment on event. This will increment the counter, irrespective of the counter direction.
- Count during active state of an asynchronous event (increment or decrement, depending on counter direction). In this case, the counter will be incremented or decremented on each cycle of the prescaled clock, as long as the event is active.
- Non-recoverable fault

The counter Event Actions are available in the Event Control registers (EVCTRL.EVACT0 and EVCTRL.EVACT1). For further details, refer to [EVCTRL](#).

Writing a '1' ('0') to an Event Input bit in the Event Control register (EVCTRL.MCEIx or EVCTRL.TCEIx) enables (disables) the corresponding action on input event.

**Note:** When several events are connected to the TCC, the enabled action will apply for each of the incoming events. Refer to *EVSYS – Event System* for details on how to configure the event system.

### Related Links

[EVSYS – Event System](#)

### 31.6.5 Sleep Mode Operation

The TCC can be configured to operate in any sleep mode. To be able to run in standby the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. The MODULE can in any sleep mode wake up the device using interrupts or perform actions through the Event System.

### 31.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Pattern and Pattern Buffer registers (PATT and PATTB)
- Waveform register (WAVE)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERB)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBx)

The following registers are synchronized when read:

## 32-bit ARM-Based Microcontrollers

**Reset:** 0x00000000

**Property:** -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
		CCB3	CCB2	CCB1	CCB0	PERB	WAVEB	PATTB
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
					CC3	CC2	CC1	CC0
Access					R	R	R	R
Reset					0	0	0	0
Bit	7	6	5	4	3	2	1	0
	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

### Bits 19, 20, 21, 22 – CCBn: Compare/Capture Buffer Channel x Synchronization Busy

This bit is cleared when the synchronization of Compare/Capture Buffer Channel x register between the clock domains is complete.

This bit is set when the synchronization of Compare/Capture Buffer Channel x register between clock domains is started.

CCBx bit is available only for existing Compare/Capture Channels. For details on CC channels number, refer to each TCC feature list.

### Bit 18 – PERB: PER Buffer Synchronization Busy

This bit is cleared when the synchronization of PERB register between the clock domains is complete.

This bit is set when the synchronization of PERB register between clock domains is started.

### Bit 17 – WAVEB: WAVE Buffer Synchronization Busy

This bit is cleared when the synchronization of WAVEB register between the clock domains is complete.

This bit is set when the synchronization of WAVEB register between clock domains is started.

### Bit 16 – PATTB: PATT Buffer Synchronization Busy

This bit is cleared when the synchronization of PATTB register between the clock domains is complete.

This bit is set when the synchronization of PATTB register between clock domains is started.

### Bits 8, 9, 10, 11 – CCn: Compare/Capture Channel x Synchronization Busy

This bit is cleared when the synchronization of Compare/Capture Channel x register between the clock domains is complete.

## 32-bit ARM-Based Microcontrollers

CTRLA.RESOLUTION	Bits [23:m]
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

### Bits 5:0 – DITHERB[5:0]: Dithering Buffer Cycle Number

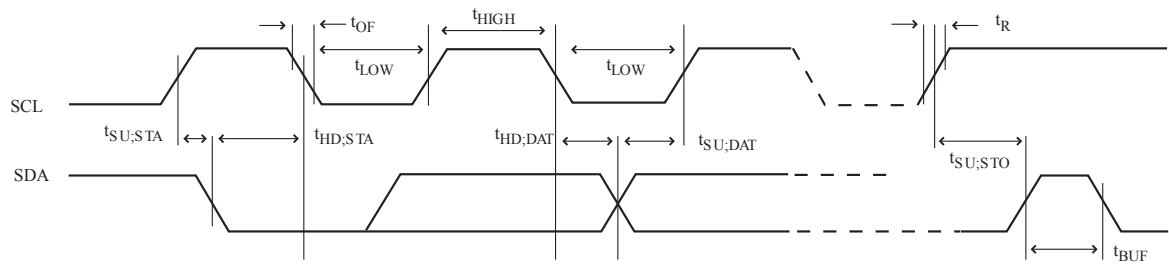
These bits represent the CCx.DITHER bits buffer. When the double buffering is enable, DITHERBUF bits value is copied to the CCx.DITHER bits on an UPDATE condition.

**Note:** This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)



**Figure 37-22. I<sup>2</sup>C Interface Bus Timing**



**Table 38-5. Device and Package Maximum Weight**

200	mg
-----	----

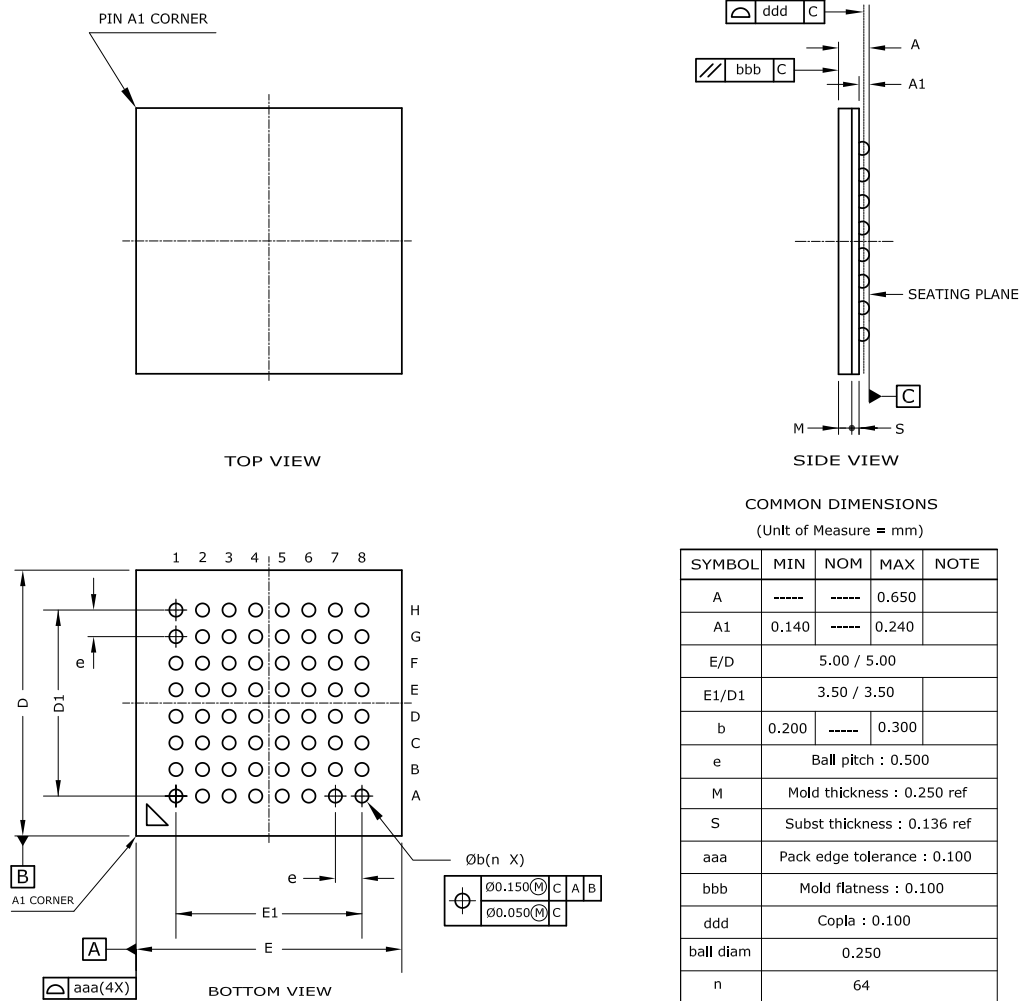
**Table 38-6. Package Characteristics**

Moisture Sensitivity Level	MSL3
----------------------------	------

**Table 38-7. Package Reference**

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

## 38.2.3 64-ball UFBGA



- Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
  2. Array as seen from the bottom of the package.
  3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
  4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

**Table 38-8. Device and Package Maximum Weight**

27.4	mg
------	----

**3 – In RAMP 2 mode with Fault keep, qualified and restart:**

If a fault occurred at the end of the period during the qualified state, the switch to the next ramp can have two restarts.

**Errata reference:** 13262

**Fix/Workaround:**

Avoid faults few cycles before the end or the beginning of a ramp.

**4 – With blanking enabled, a recoverable fault that occurs during the first increment of a rising TCC is not blanked.**

**Errata reference:** 12519

**Fix/Workaround:**

None

**5 – In Dual slope mode a Retrigger Event does not clear the TCC counter.**

**Errata reference:** 12354

**Fix/Workaround:**

None

**6 – In two ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.**

**Errata reference:** 12224

**Fix/Workaround:**

None

**7 – If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.**

**Errata reference:** 12107

**Fix/Workaround:**

None

**8 – When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.**

**Errata reference:** 12477

**Fix/Workaround:**

None.

**9 – TCC fault filtering on inverted fault is not working.**

**Errata reference:** 12512

**Fix/Workaround:**

Use only non-inverted faults.

**10 – When waking up from the STANDBY power save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to 1.**

**Errata reference:** 12227

**Fix/Workaround:**

After waking up from STANDBY power save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits

**3 – Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these mode.**  
**Example:** when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX won't work.

**Errata reference:** 14817

**Fix/Workaround:**

Basic capture mode must be set in lower channel and advance capture mode in upper channel.

**Example:** CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX

All capture will be done as expected.

## 40.3 Device Variant C

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

### 40.3.1 Die Revision F

#### 40.3.1.1 Device

**1 – The SYSTICK calibration value is incorrect.**

**Errata reference:** 14155

**Fix/Workaround:**

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the SysTick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

**2 – On pin PA24 and PA25 the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled except for USB.**

**Errata reference:** 12368

**Fix/Workaround:**

For pin PA24 and PA25, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

**3 – If APB clock is stopped and GCLK clock is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, as a consequence debug operation is impossible.**

**Errata reference:** 10416

**Fix/Workaround:**

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

**4 – If the external XOSC32K is broken, neither the external pin RST nor the GCLK software reset can reset the GCLK generators using XOSC32K as source clock.**

**Errata reference:** 12164

**Fix/Workaround:**

## 32-bit ARM-Based Microcontrollers

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
SFDR	Spurious Free Dynamic Range	1x Gain	63.1	65.0	66.5	dB
SINAD	Signal-to-Noise and Distortion	$F_{CLK\_ADC} = 2.1\text{MHz}$	50.7	59.5	61.0	dB
SNR	Signal-to-Noise Ratio	$F_{IN} = 40\text{kHz}$	49.9	60.0	64.0	dB
THD	Total Harmonic Distortion	$A_{IN} = 95\%\text{FSR}$	-65.4	-63.0	-62.1	dB
	Noise RMS	$T = 25^{\circ}\text{C}$	-	1.0	-	mV

**Table 44-18. Single-Ended Mode (Device Variant B)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ENOB	Effective Number of Bits	With gain compensation	-	9.7	10.1	Bits
TUE	Total Unadjusted Error	1x gain	-	7.9	40.0	LSB
INL	Integral Non-Linearity	1x gain	1.4	2.6	6.0	LSB
DNL	Differential Non-Linearity	1x gain	+/-0.6	+/-0.7	+/-0.95	LSB
	Gain Error	Ext. Ref. 1x	-5.0	0.6	+5.0	mV
	Gain Accuracy(4)	Ext. Ref. 0.5x	+/-0.1	+/-0.37	+/-0.55	%
		Ext. Ref. 2x to 16X	+/-0.01	+/-0.1	+/-0.2	%
	Offset Error	Ext. Ref. 1x	-5.0	0.6	+10.0	mV
SFDR	Spurious Free Dynamic Range	1x Gain	63.0	68.0	68.7	dB
SINAD	Signal-to-Noise and Distortion	$F_{CLK\_ADC} = 2.1\text{MHz}$	55.0	60.1	62.5	dB
SNR	Signal-to-Noise Ratio	$F_{IN} = 40\text{kHz}$	54.0	61.0	64.0	dB
THD	Total Harmonic Distortion	$A_{IN} = 95\%\text{FSR}$	-69.0	-68.0	-65.0	dB
	Noise RMS	$T = 25^{\circ}\text{C}$	-	1.0	-	mV

**Note:**

- Maximum numbers are based on characterization and not tested in production, and for 5% to 95% of the input voltage range.
- Respect the input common mode voltage through the following equations (where  $V_{CM\_IN}$  is the Input channel common mode voltage) for all  $V_{IN}$ :
  - $V_{CM\_IN} < 0.7 \cdot V_{DDANA} + V_{REF}/4 - 0.75\text{V}$
  - $V_{CM\_IN} > V_{REF}/4 - 0.3 \cdot V_{DDANA} - 0.1\text{V}$
- The ADC channels on pins PA08, PA09, PA10, PA11 are powered from the  $V_{DDIO}$  power supply. The ADC performance of these pins will not be the same as all the other ADC channels on pins powered from the  $V_{DDANA}$  power supply.
- The gain accuracy represents the gain error expressed in percent. Gain accuracy (%) = (Gain Error in V x 100) / ( $V_{ref}/\text{GAIN}$ )

### 44.6.4 Inputs and Sample and Hold Acquisition Times

The analog voltage source must be able to charge the sample and hold (S/H) capacitor in the ADC in order to achieve maximum accuracy. Seen externally the ADC input consists of a resistor ( $R_{SAMPLE}$ ) and a