

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g15b-mu

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2. Configuration Summary

	SAM D21J	SAM D21G	SAM D21E
Pins	64	48 (45 for WLCSP)	32 (35 for WLCSP)
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	256/128/64/32KB	256/128/64/32KB	256/128/64/32KB
SRAM	32/16/8/4KB	32/16/8/4KB	32/16/8/4KB
Timer Counter (TC) instances	5	3 (5 for WLCSP)	3
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	6/4/2
DMA channels	12	12	12
USB interface	1	1	1
Serial Communication Interface (SERCOM) instances	6	6	4
Inter-IC Sound (I ² S) interface	1	1	1
Analog-to-Digital Converter (ADC) channels	20	14	10
Analog Comparators (AC)	2	2	2
Digital-to-Analog Converter (DAC) channels	1	1	1
Real-Time Counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	One 32-bit value or	One 32-bit value or	One 32-bit value or
	two 16-bit values	two 16-bit values	two 16-bit values
External Interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		

32-bit ARM-Based Microcontrollers



Bits 7:4 - REVISION[3:0]: Revision Number

Revision of the peripheral. Starts at 0x0 and increments by one at both major and minor revisions.

Bit 3 – JEPU: JEP-106 Identity Code is used

This bit will always return one when read, indicating that JEP-106 code is used.

Bits 2:0 – JEPIDCH[2:0]: JEP-106 Identity Code High

These bits will always return 0x1 when read, indicating an Atmel device (Atmel JEP-106 identity code is 0x1F).

13.13.18 Peripheral Identification 3

 Name:
 PID3

 Offset:
 0x1FEC

 Reset:
 0x0000000

 Property:



16.5.3 Clocks

The PM bus clock (CLK_PM_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_PM_APB can be found in *Peripheral Clock Default State* table in the *Peripheral Clock Masking* section. If this clock is disabled in the Power Manager, it can only be re-enabled by a reset.

A generic clock (GCLK_MAIN) is required to generate the main clock. The clock source for GCLK_MAIN is configured by default in the Generic Clock Controller, and can be re-configured by the user if needed. Refer to *GCLK* – *Generic Clock Controller* for details.

Related Links

Peripheral Clock Masking GCLK - Generic Clock Controller

16.5.3.1 Main Clock

The main clock (CLK_MAIN) is the common source for the synchronous clocks. This is fed into the common 8-bit prescaler that is used to generate synchronous clocks to the CPU, AHB and APBx modules.

16.5.3.2 CPU Clock

The CPU clock (CLK_CPU) is routed to the CPU. Halting the CPU clock inhibits the CPU from executing instructions.

16.5.3.3 AHB Clock

The AHB clock (CLK_AHB) is the root clock source used by peripherals requiring an AHB clock. The AHB clock is always synchronous to the CPU clock and has the same frequency, but may run even when the CPU clock is turned off. A clock gate is inserted from the common AHB clock to any AHB clock of a peripheral.

16.5.3.4 APBx Clocks

The APBx clock (CLK_APBX) is the root clock source used by modules requiring a clock on the APBx bus. The APBx clock is always synchronous to the CPU clock, but can be divided by a prescaler, and will run even when the CPU clock is turned off. A clock gater is inserted from the common APB clock to any APBx clock of a module on APBx bus.

16.5.4 DMA

Not applicable.

16.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the PM interrupt requires the Interrupt Controller to be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

16.5.6 Events

Not applicable.

16.5.7 Debug Operation

When the CPU is halted in debug mode, the PM continues normal operation. In sleep mode, the clocks generated from the PM are kept running to allow the debugger accessing any modules. As a consequence, power measurements are not possible in debug mode.

- 2. Clock representation must be selected by writing the Clock Representation bit in the Control register (CTRL.CLKREP)
- 3. Prescaler value must be selected by writing the Prescaler bit group in the Control register (CTRL.PRESCALER)

The RTC prescaler divides the source clock for the RTC counter.

Note: In Clock/Calendar mode, the prescaler must be configured to provide a 1Hz clock to the counter for correct operation.

The frequency of the RTC clock (CLK_RTC_CNT) is given by the following formula:

 $f_{\text{CLK}_{\text{RTC}_{\text{CNT}}}} = \frac{f_{\text{GCLK}_{\text{RTC}}}}{2^{\text{PRESCALER}}}$

The frequency of the generic clock, GCLK_RTC, is given by f_{GCLK_RTC} , and $f_{CLK_RTC_CNT}$ is the frequency of the internal prescaled RTC clock, CLK_RTC_CNT.

19.6.2.2 Enabling, Disabling and Resetting

The RTC is enabled by setting the Enable bit in the Control register (CTRL.ENABLE=1). The RTC is disabled by writing CTRL.ENABLE=0.

The RTC is reset by setting the Software Reset bit in the Control register (CTRL.SWRST=1). All registers in the RTC, except DEBUG, will be reset to their initial state, and the RTC will be disabled. The RTC must be disabled before resetting it.

19.6.3 Operating Modes

The RTC counter supports three RTC operating modes: 32-bit Counter, 16-bit Counter and Clock/ Calendar. The operating mode is selected by writing to the Operating Mode bit group in the Control register (CTRL.MODE).

19.6.3.1 32-Bit Counter (Mode 0)

When the RTC Operating Mode bits in the Control register are zero (CTRL.MODE=00), the counter operates in 32-bit Counter mode. The block diagram of this mode is shown in Figure 19-1. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The counter will increment until it reaches the top value of 0xFFFFFFF, and then wrap to 0x00000000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 32-bit format.

The counter value is continuously compared with the 32-bit Compare register (COMP0). When a compare match occurs, the Compare 0interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMP0) is set on the next 0-to-1 transition of CLK_RTC_CNT.

If the Clear on Match bit in the Control register (CTRL.MATCHCLR) is '1', the counter is cleared on the next counter cycle when a compare match with COMP0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than are possible with the prescaler events. Note that when CTRL.MATCHCLR is '1', INTFLAG.CMP0 and INTFLAG.OVF will both be set simultaneously on a compare match with COMP0.

19.6.3.2 16-Bit Counter (Mode 1)

When the RTC Operating Mode bits in the Control register (CTRL.MODE) are 1, the counter operates in 16-bit Counter mode as shown in Figure 19-2. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. In 16-bit Counter mode, the 16-bit Period register (PER) holds the maximum value of the counter. The counter will increment until it reaches the PER value, and then

32-bit ARM-Based Microcontrollers

Offset	Name	Bit							
		Pos.							
0x0D									
	Reserved								
0x0F									
0x10	COUNT	7:0			COUN	IT[7:0]			
0x11	COONT	15:8	COUNT[15:8]						
0x12	Reserved								
0x13	Reserved								
0x14	DED	7:0	PER[7:0]						
0x15	PER	15:8	PER[15:8]						
0x16	Reserved								
0x17	Reserved								
0x18	COMPO	7:0			COM	P[7:0]	:		
0x19	COMPO	15:8	COMP[15:8]						
0x1A	001404	7:0			COM	P[7:0]			
0x1B		15:8			COMF	P[15:8]			

Table 19-3. MODE2 - Mode Register Summary

Offset	Name	Bit Pos								
										OWDOT
0x00	CTRL	7:0	MATCHCLR	CLKREP			MOD	E[1:0]	ENABLE	SWRST
0x01		15:8						PRESCA	LER[3:0]	
0x02	READREO	7:0					ADD	R[5:0]		
0x03	THE TENE Q	15:8	RREQ	RCONT						
0x04	EVICTE	7:0	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
0x05	EVCIRE	15:8	OVFEO							ALARMEO0
0x06	INTENCLR	7:0	OVF	SYNCRDY						ALARM0
0x07	INTENSET	7:0	OVF	SYNCRDY						ALARM0
0x08	INTFLAG	7:0	OVF	SYNCRDY						ALARM0
0x09	Reserved									
0x0A	STATUS	7:0	SYNCBUSY							
0x0B	DBGCTRL	7:0								DBGRUN
0x0C	FREQCORR	7:0	SIGN				VALUE[6:0]	:		
0x0D										
	Reserved									
0x0F										
0x10		7:0	MINUT	FE[1:0]			SECO	ND[5:0]		
0x11	CLOCK	15:8		HOU	R[3:0]			MINU	TE[5:2]	
0x12	CLUCK	23:16	MONT	H[1:0]			DAY[4:0]			HOUR[4]
0x13		31:24			YEA	R[5:0]			MON	FH[3:2]
0x14										
	Reserved									
0x17										

19.8.17 Status

	Name: Offset: Reset: Property:	STATUS 0x0A 0x00 -						
Bit	7	6	5	4	3	2	1	0
	SYNCBUS	SY .						
Access	R	·	·					

Reset 0

Bit 7 – SYNCBUSY: Synchronization Busy

This bit is cleared when the synchronization of registers between the clock domains is complete.

This bit is set when the synchronization of registers between clock domains is started.

19.8.18 Debug Control

Name: DBGCTRL Offset: 0x0B Reset: 0x00 Property: -

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Run During Debug

This bit is not reset by a software reset.

Writing a zero to this bit causes the RTC to halt during debug mode.

Writing a one to this bit allows the RTC to continue normal operation during debug mode.

19.8.19 Frequency Correction

Name:FREQCORROffset:0x0CReset:0x00Property:Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0	
	SIGN		VALUE[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Bit 7 – SIGN: Correction Sign

When static arbitration is selected, the arbiter will prioritize a low channel number over a high channel number as shown in the figure below. When using the static arbitration there is a risk of high channel numbers never being granted access as the active channel. This can be avoided using a dynamic arbitration scheme.

Figure 20-5. Static Priority Scheduling

Lowest Channel	Channel 0	Highest Priority
		^
	•	
	•	
	Channel x	
	Channel x+1	
	•	
	•	
	•	
		·
Highest Channel	Channel N	Lowest Priority

Dynamic Arbitration within a priority level is selected by writing a '1' to PRICTRL0.RRLVLENx.

The dynamic arbitration scheme in the DMAC is round-robin. With the round-robin scheme, the channel number of the last channel being granted access will have the lowest priority the next time the arbiter has to grant access to a channel within the same priority level, as shown in Figure 20-6. The channel number of the last channel being granted access as the active channel is stored in the Level x Channel Priority Number bit group in the Priority Control 0 register (PRICTRL0.LVLPRIx) for the corresponding priority level.

Figure 20-6. Dynamic (Round-Robin) Priority Scheduling



Writing a '1' to this bit will set the Channel Transfer Error Interrupt Enable bit, which enables the Channel Transfer Error interrupt.

Value	Description
0	The Channel Transfer Error interrupt is disabled.
1	The Channel Transfer Error interrupt is enabled.

20.8.22 Channel Interrupt Flag Status and Clear

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name:	CHINTFLAG
Offset:	0x4E
Reset:	0x00
Property:	-

Bit	7	6	5	4	3	2	1	0
						SUSP	TCMPL	TERR
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SUSP: Channel Suspend

This flag is cleared by writing a '1' to it.

This flag is set when a block transfer with suspend block action is completed, when a software suspend command is executed, when a suspend event is received or when an invalid descriptor is fetched by the DMA.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Channel Suspend interrupt flag for the corresponding channel.

For details on available software commands, refer to CHCTRLB.CMD.

For details on available event input actions, refer to CHCTRLB.EVACT.

For details on available block actions, refer to BTCTRL.BLOCKACT.

Bit 1 – TCMPL: Channel Transfer Complete

This flag is cleared by writing a '1' to it.

This flag is set when a block transfer is completed and the corresponding interrupt block action is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transfer Complete interrupt flag for the corresponding channel.

Bit 0 – TERR: Channel Transfer Error

This flag is cleared by writing a '1' to it.

This flag is set when a bus error is detected during a beat transfer or when the DMAC fetches an invalid descriptor.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transfer Error interrupt flag for the corresponding channel.

Name: DSTADDR Offset: 0x08 **Reset:** _ Property: -Bit 31 30 29 28 27 26 25 24 DSTADDR[31:24] Access Reset Bit 23 22 21 20 19 18 17 16 DSTADDR[23:16] Access Reset Bit 15 14 13 12 11 10 9 8 DSTADDR[15:8] Access Reset 3 2 Bit 7 6 5 4 1 0 DSTADDR[7:0] Access

20.10.4 Block Transfer Destination Address

The DSTADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Reset

Bits 31:0 – DSTADDR[31:0]: Transfer Destination Address

This bit group holds the destination address corresponding to the last beat transfer address in the block transfer.

20.10.5 Next Descriptor Address

The DESCADDR register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Name: DESCADDR Offset: 0x0C Reset: -Property: -

Bit	31	30	29	28	27	26	25	24
				DESCAD	DR[31:24]			
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
[DESCAD	DR[23:16]	-		
Access								
Reset								

- D represent the data bits per frame
- S represent the sum of start and first stop bits, if present.

Table 25-3 shows the BAUD register value versus baud frequency f_{BAUD} at a serial engine frequency of 48MHz. This assumes a *D* value of 8 bits and an *S* value of 2 bits (10 bits, including start and stop bits).

BAUD Register Value	Serial Engine CPF	f _{BAUD} at 48MHz Serial Engine Frequency (f _{REF})
0 - 406	160	3MHz
407 – 808	161	2.981MHz
809 – 1205	162	2.963MHz
65206	31775	15.11kHz
65207	31871	15.06kHz
65208	31969	15.01kHz

Table 25-3. BAUD Register Value vs. Baud Frequency

25.6.3 Additional Features

25.6.3.1 Address Match and Mask

The SERCOM address match and mask feature is capable of matching either one address, two unique addresses, or a range of addresses with a mask, based on the mode selected. The match uses seven or eight bits, depending on the mode.

Address With Mask

An address written to the Address bits in the Address register (ADDR.ADDR), and a mask written to the Address Mask bits in the Address register (ADDR.ADDRMASK) will yield an address match. All bits that are masked are not included in the match. Note that writing the ADDR.ADDRMASK to 'all zeros' will match a single unique address, while writing ADDR.ADDRMASK to 'all ones' will result in all addresses being accepted.

Figure 25-4. Address With Mask



Two Unique Addresses

The two addresses written to ADDR and ADDRMASK will cause a match.

Property: -

Bit	7	6	5	4	3	2	1	0
ſ	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R	R/W	R
Reset	0				0	0	0	0

Bit 7 - ERROR: Error

This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. The BUFOVF error will set this interrupt flag.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – SSL: Slave Select Low

This flag is cleared by writing '1' to it.

This bit is set when a high to low transition is detected on the _SS pin in slave mode and Slave Select Low Detect (CTRLB.SSDE) is enabled.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 2 – RXC: Receive Complete

This flag is cleared by reading the Data (DATA) register or by disabling the receiver.

This flag is set when there are unread data in the receive buffer. If address matching is enabled, the first data received in a transaction will be an address.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 1 – TXC: Transmit Complete

This flag is cleared by writing '1' to it or by writing new data to DATA.

In master mode, this flag is set when the data have been shifted out and there are no new data in DATA.

In slave mode, this flag is set when the _SS pin is pulled high. If address matching is enabled, this flag is only set if the transaction was initiated with an address match.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 0 – DRE: Data Register Empty

This flag is cleared by writing new data to DATA.

This flag is set when DATA is empty and ready for new data to transmit.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Startup Timing The minimum time between SDA transition and SCL rising edge is 6 APB cycles when the DATA register is written in smart mode. If a greater startup time is required due to long rise times, the time between DATA write and IF clear must be controlled by software.

Note: When timing is controlled by user, the Smart Mode cannot be enabled.

Related Links

Electrical Characteristics

Master Clock Generation (High-Speed Mode)

For I²C *Hs* transfers, there is no SCL synchronization. Instead, the SCL frequency is determined by the GCLK_SERCOMx_CORE frequency (f_{GCLK}) and the High-Speed Baud setting in the Baud register (BAUD.HSBAUD). When BAUD.HSBAUDLOW=0, the HSBAUD value will determine both SCL high and SCL low. In this case the following formula determines the SCL frequency.

$$f_{\rm SCL} = \frac{f_{\rm GCLK}}{2 + 2 \cdot HS \, BAUD}$$

When HSBAUDLOW is non-zero, the following formula determines the SCL frequency.

$$f_{\rm SCL} = \frac{f_{\rm GCLK}}{2 + HS \, BAUD + HSBAUDLOW}$$

Note: The I²C standard *Hs* (High-speed) requires a nominal high to low SCL ratio of 1:2, and HSBAUD should be set accordingly. At a minimum, BAUD.HSBAUD and/or BAUD.HSBAUDLOW must be non-zero.

Transmitting Address Packets

The I²C master starts a bus transaction by writing the I²C slave address to ADDR.ADDR and the direction bit, as described in Principle of Operation. If the bus is busy, the I²C master will wait until the bus becomes idle before continuing the operation. When the bus is idle, the I²C master will issue a start condition on the bus. The I²C master will then transmit an address packet using the address written to ADDR.ADDR. After the address packet has been transmitted by the I²C master, one of four cases will arise according to arbitration and transfer direction.

Case 1: Arbitration lost or bus error during address packet transmission

If arbitration was lost during transmission of the address packet, the Master on Bus bit in the Interrupt Flag Status and Clear register (INTFLAG.MB) and the Arbitration Lost bit in the Status register (STATUS.ARBLOST) are both set. Serial data output to SDA is disabled, and the SCL is released, which disables clock stretching. In effect the I²C master is no longer allowed to execute any operation on the bus until the bus is idle again. A bus error will behave similarly to the arbitration lost condition. In this case, the MB interrupt flag and Master Bus Error bit in the Status register (STATUS.BUSERR) are both set in addition to STATUS.ARBLOST.

The Master Received Not Acknowledge bit in the Status register (STATUS.RXNACK) will always contain the last successfully received acknowledge or not acknowledge indication.

In this case, software will typically inform the application code of the condition and then clear the interrupt flag before exiting the interrupt routine. No other flags have to be cleared at this moment, because all flags will be cleared automatically the next time the ADDR.ADDR register is written.

Case 2: Address packet transmit complete – No ACK received

If there is no I²C slave device responding to the address packet, then the INTFLAG.MB interrupt flag and STATUS.RXNACK will be set. The clock hold is active at this point, preventing further activity on the bus.

32-bit ARM-Based Microcontrollers

Bit	7	6	5	4	3 2		1	0
	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
Access	R	R/W		R	R	R	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 10 – LENERR: Transaction Length Error

This bit is set when the length counter is enabled (LENGTH.LENEN) and a STOP or repeated START is received before or after the length in LENGTH.LEN is reached.

This bit is cleared automatically when responding to a new start condition with ACK or NACK (CTRLB.CMD=0x3) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Bit 10 – HS: High-speed

This bit is set if the slave detects a START followed by a Master Code transmission.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status. However, this flag is automatically cleared when a STOP is received.

Bit 9 – SEXTTOUT: Slave SCL Low Extend Time-Out

This bit is set if a slave SCL low extend time-out occurs.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No SCL low extend time-out has occurred.
1	SCL low extend time-out has occurred.

Bit 7 – CLKHOLD: Clock Hold

The slave Clock Hold bit (STATUS.CLKHOLD) is set when the slave is holding the SCL line low, stretching the I2C clock. Software should consider this bit a read-only status flag that is set when INTFLAG.DRDY or INTFLAG.AMATCH is set.

This bit is automatically cleared when the corresponding interrupt is also cleared.

Bit 6 – LOWTOUT: SCL Low Time-out

This bit is set if an SCL low time-out occurs.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No SCL low time-out has occurred.
1	SCL low time-out has occurred.





The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Period and Pulse-Width (PPW) Capture Action

The TC can perform two input captures and restart the counter on one of the edges. This enables the TC to measure the pulse width and period and to characterize the frequency *f* and duty cycle of an input signal:

$$f = \frac{1}{T}$$
 dutyCycle $= \frac{t_p}{T}$

Selecting PWP (pulse-width, period) in the Event Action bit group in the Event Control register (EVCTRL.EVACT) enables the TC to perform one capture action on the rising edge and the other one on the falling edge. The period T will be captured into CC1 and the pulse width t_p in CC0. EVCTRL.EVACT=PPW (period and pulse-width)offers identical functionality, but will capture T into CC0 and t_p into CC1.

The TC Event Input Invert Enable bit in the Event Control register (EVCTRL.TCINV) is used to select whether the wraparound should occur on the rising edge or the falling edge. If EVCTRL.TCINV=1, the wraparound will happen on the falling edge.

To fully characterize the frequency and duty cycle of the input signal, activate capture on CC0 and CC1 by writing 0x3 to the Capture Channel x Enable bit group in the Control C register (CTRLC.CPTEN). When only one of these measurements is required, the second channel can be used for other purposes.

The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

32-bit ARM-Based Microcontrollers

Value	Name	Description
0x01	OFF (L3)	Corresponds to the powered-off, disconnected, and disabled state.
0x02	ON (L0)	Corresponds to the Idle and Active states.
0x04	SUSPEND (L2)	
0x08	SLEEP (L1)	
0x10	DNRESUME	Down Stream Resume.
0x20	UPRESUME	Up Stream Resume.
0x40	RESET	USB lines Reset.
Others		Reserved

32.8.1.5 Descriptor Address

Name:	DESCADD
Offset:	0x24
Reset:	0x0000000
Property:	PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
				DESCAL	DD[31:24]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
				DESCAL	DD[23:16]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
				DESCA	DD[15:8]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
				DESCA	DD[7:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DESCADD[31:0]: Descriptor Address Value

These bits define the base address of the main USB descriptor in RAM. The two least significant bits must be written to zero.

32.8.1.6 Pad Calibration

The Pad Calibration values must be loaded from the NVM Software Calibration Area into the USB Pad Calibration register by software, before enabling the USB, to achieve the specified accuracy. Refer to *NVM Software Calibration Area Mapping* for further details.

Refer to for further details.

Name: PADCAL Offset: 0x28 Offset: 0x08 Reset: 0xxxxxxxx Property: NA

Bit	15	14	13	12	11	10	9	8
					VARIABLE[10:4]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
		VARIABLE[3:0] SUBPID[3:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	х	0	0	0	x

Bits 14:4 – VARIABLE[10:0]: Variable field send with extended token

These bits define the VARIABLE field sent with extended token. See "Section 2.1.1 Protocol Extension Token in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum."

To support the USB2.0 Link Power Management addition the VARIABLE field should be set as described below.

VARIABLE	Description
VARIABLE[3:0]	bLinkState ⁽¹⁾
VARIABLE[7:4]	BESL (See LPM ECN) ⁽²⁾
VARIABLE[8]	bRemoteWake ⁽¹⁾
VARIABLE[10:9]	Reserved

(1) for a definition of LPM Token bRemoteWake and bLinkState fields, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum"
(2) for a definition of LPM Token BESL field, refer to "Table 2-3 in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum" and "Table X-X1 in Errata for ECN USB 2.0 Link Power Management.

Bits 3:0 – SUBPID[3:0]: SUBPID field send with extended token

These bits define the SUBPID field sent with extended token. See "Section 2.1.1 Protocol Extension Token in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum".

To support the USB2.0 Link Power Management addition the SUBPID field should be set as described in "Table 2.2 SubPID Types in the reference document ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum".

32.8.7.5 Host Status Bank

Name:	STATUS_BK
Offset:	0x0A & 0x1A
Reset:	Oxxxxxxx

37.12.68MHz RC Oscillator (OSC8M) CharacteristicsTable 37-55.Internal 8MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
f _{OUT}	Output frequency	Calibrated against a 8MHz reference at 25°C, over [-40, +85]C, over [1.62, 3.63]V	7.8	8	8.16	MHz
		Calibrated against a 8MHz reference at 25°C, at V_{DD} =3.3V	7.94	8	8.06	
		Calibrated against a 8MHz reference at 25°C, over [1.62, 3.63]V	7.92	8	8.08	
TempCo	Frequency vs. Temperature drift		-1.2		1	%
SupplyCo	Frequency vs. Supply drift		-2		2	%
I _{OSC8M}	Current consumption	IDLE2 on OSC32K versus IDLE2 on calibrated OSC8M enabled at 8MHz (FRANGE=1, PRESC=0)		64		μA
t _{STARTUP}	Startup time		-	2.1	3	μs
Duty	Duty cycle		-	50	-	%

37.12.7 Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics Table 37-56. FDPLL96M Characteristics⁽¹⁾ (Device Variant A)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
f _{IN}	Input frequency		32	-	2000	KHz
f _{OUT}	Output frequency		48	-	96	MHz
I _{FDPLL96M}	Current consumption	f _{IN} = 32 kHz, f _{OUT} = 48 MHz	-	500	700	μA
		f _{IN} = 32 kHz, f _{OUT} = 96 MHz	-	900	1200	
J _p	Period jitter	f _{IN} = 32 kHz, f _{OUT} = 48 MHz	-	1.5	2.0	%
		f _{IN} = 32 kHz, f _{OUT} = 96 MHz	-	3.0	10.0	
		f _{IN} = 2 MHz, f _{OUT} = 48 MHz	-	1.3	2.0	
		f _{IN} = 2 MHz, f _{OUT} = 96 MHz	-	3.0	7.0	
t _{LOCK}	Lock Time	After start-up, time to get lock signal. f _{IN} = 32 kHz, f _{OUT} = 96 MHz	-	1.3	2	ms
		f _{IN} = 2 MHz, f _{OUT} = 96 MHz	-	25	50	μs
Duty	Duty cycle		40	50	60	%

Table 38-5. Device and Package Maximum Weight

200	mg
Table 38-6. Package Charateristics	
Moisture Sensitivity Level	MSL3
Table 38-7. Package Reference	
JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

38.2.3 64-ball UFBGA



Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc. 2. Array as seen from the bottom of the package.

Dimension A includes stand-off helght A1, package body thickness, and Ild helght, but does not include attached features.
 Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 38-8. Device and Package Maximum Weight

27.4 mg	
---------	--

44.3 General Operating Ratings

The device must operate within the ratings in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 44-3. General Operating Conditions

Symbol	Parameter	Condition	Min.	Тур.	Max.	Units
V _{DD}	Power supply voltage		1.62(1)	3.3	3.63	V
V _{DDANA}	Analog supply voltage		1.62(1)	3.3	3.63	V
T _A	Temperature range		-40	25	85	°C
TJ	Junction temperature		-	-	145	°C

Note:

Notes: 1. With BOD33 disabled. If the BOD33 is enabled, check Table 37-20.

44.4 Maximum Clock Frequencies

Table 44-4. Maximum GCLK Generator Output Frequencies (Device Variant A)

Symbol	Description	Conditions	Max.	Units
f _{GCLKGEN0} / f _{GCLK_MAIN}	GCLK Generator Output Frequency	Undivided	96	MHz
[†] GCLKGEN1		Divided	32	MHz
f _{GCLKGEN2}				
f _{GCLKGEN3}				
f _{GCLKGEN4}				
f _{GCLKGEN5}				
f _{GCLKGEN6}				
f _{GCLKGEN7}				
f _{GCLKGEN8}				

Table 44-5. Maximum Peripheral Clock Frequencies (Device Variant A)

Symbol	Description	Max.	Units
f _{CPU}	CPU clock frequency	32	MHz
f _{AHB}	AHB clock frequency	32	MHz
f _{APBA}	APBA clock frequency	32	MHz
f _{APBB}	APBB clock frequency	32	MHz
f _{APBC}	APBC clock frequency	32	MHz
f _{GCLK_DFLL48M_REF}	DFLL48M Reference clock frequency	33	KHz
f _{GCLK_DPLL}	FDPLL96M Reference clock frequency	2	MHz

44.7 NVM Characteristics

Table 44-28. Maximum Operating Frequency

V _{DD} range	NVM Wait States	Maximum Operating Frequency	Units
1.62V to 2.7V	0	14	MHz
	1	28	-
	2	40	-
2.7V to 3.63V	0	24	-
	1	40	-

Note that on this flash technology, a max number of 8 consecutive write is allowed per row. Once this number is reached, a row erase is mandatory.

Table 44-29. Flash Endurance and Data Retention

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
Ret _{NVM25k}	Retention after up to 25k	Average ambient 55°C	10	50	-	Years
Ret _{NVM2.5k}	Retention after up to 2.5k	Average ambient 55°C	20	100	-	Years
Ret _{NVM100}	Retention after up to 100	Average ambient 55°C	25	>100	-	Years
Cyc _{NVM}	Cycling Endurance ⁽¹⁾	-40°C < Ta < 85°C	25k	150k	-	Cycles

Note: 1. An endurance cycle is a write and an erase operation.

 Table 44-30.
 EEPROM Emulation⁽¹⁾
 Endurance and Data Retention

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
Ret _{EEPROM100k}	Retention after up to 100k	Average ambient 55°C	10	50	-	Years
Ret _{EEPROM10k}	Retention after up to 10k	Average ambient 55°C	20	100	-	Years
Cyc _{EEPROM}	Cycling Endurance ⁽²⁾	-40°C < Ta < 85°C	100k	600k	-	Cycles

Notes: 1. The EEPROM emulation is a software emulation described in the App note AT03265.

2. An endurance cycle is a write and an erase operation.

Table 44-31. NVM Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units
t _{FPP}	Page programming time	-	-	-	2.5	ms
t _{FRE}	Row erase time	-	-	-	6	ms
t _{FCE}	DSU chip erase time (CHIP_ERASE)	-	-	-	240	ms