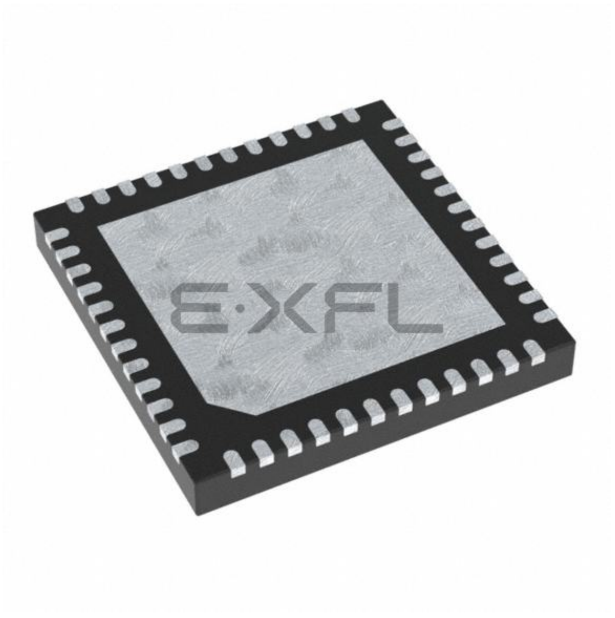
Microchip Technology - ATSAMD21G16B-MF Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g16b-mf

14.4 Enabling a Peripheral

In order to enable a peripheral that is clocked by a Generic Clock, the following parts of the system needs to be configured:

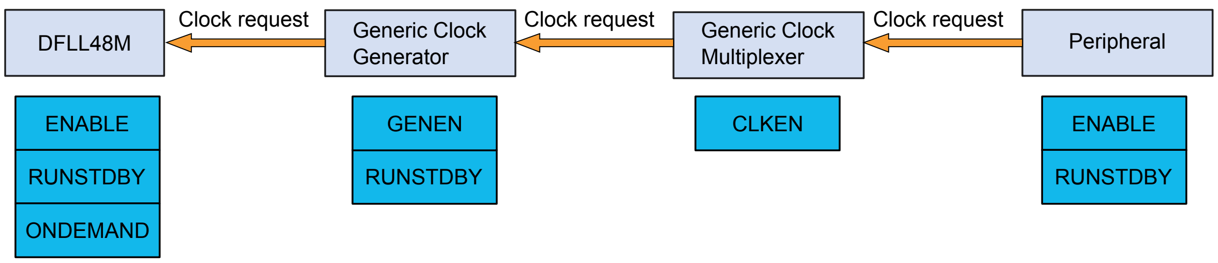
- A running Clock Source.
- A clock from the Generic Clock Generator must be configured to use one of the running Clock Sources, and the Generator must be enabled.
- The Generic Clock Multiplexer that provides the Generic Clock signal to the peripheral must be configured to use a running Generic Clock Generator, and the Generic Clock must be enabled.
- The user interface of the peripheral needs to be unmasked in the PM. If this is not done the peripheral registers will read all 0's and any writing attempts to the peripheral will be discarded.

14.5 Disabling a Peripheral

When disabling a peripheral and if a pin change interrupt is enabled on pins driven by the respective peripheral, a wake condition may be generated. If this happen the interrupt flag will not be set. As a consequence the system will not be able to identify the wake source. To avoid this, the interrupt enable register of the peripheral must be cleared (or the Nested Vectored Interrupt Controller (NVIC) Enable for the peripheral must be cleared) before disabling the peripheral.

14.6 On-demand, Clock Requests

Figure 14-4. Clock request routing



All clock sources in the system can be run in an on-demand mode: the clock source is in a stopped state unless a peripheral is requesting the clock source. Clock requests propagate from the peripheral, via the GCLK, to the clock source. If one or more peripheral is using a clock source, the clock source will be started/kept running. As soon as the clock source is no longer needed and no peripheral has an active request, the clock source will be stopped until requested again.

The clock request can reach the clock source only if the peripheral, the generic clock and the clock from the Generic Clock Generator in-between are enabled. The time taken from a clock request being asserted to the clock source being ready is dependent on the clock source startup time, clock source frequency as well as the divider used in the Generic Clock Generator. The total startup time Tstart from a clock request until the clock is available for the peripheral is between:

T_{start_max} = Clock source startup time + 2 × clock source periods + 2 × divided clock source periods

T_{start_min} = Clock source startup time + 1 × clock source period + 1 × divided clock source period

The time between the last active clock request stopped and the clock is shut down, T_{stop}, is between:

T_{stop_min} = 1 × divided clock source period + 1 × clock source period

T_{stop_max} = 2 × divided clock source periods + 2 × clock source periods

Values	Description
0x6	Generic clock generator 6
0x7	Generic clock generator 7
0x8	Generic clock generator 8
0x9-0xF	Reserved

A power reset will reset the GENDIV register for all IDs, including the generic clock generator used by the RTC. If a generic clock generator ID other than generic clock generator 0 is not a source of a ,“locked” generic clock or a source of the RTC generic clock, a user reset will reset the GENDIV for this ID.

After a power reset, the reset value of the GENDIV register is as shown in the next table.

GCLK Generator ID	Reset Value after a Power Reset
0x00	0x00000000
0x01	0x00000001
0x02	0x00000002
0x03	0x00000003
0x04	0x00000004
0x05	0x00000005
0x06	0x00000006
0x07	0x00000007
0x08	0x00000008

After a user reset, the reset value of the GENDIV register is as shown in next table.

GCLK Generator ID	Reset Value after a User Reset
0x00	0x00000000
0x01	0x00000001 if the generator is not used by the RTC and not a source of a 'locked' generic clock No change if the generator is used by the RTC or used by a GCLK with a WRTLOCK as one
0x02	0x00000002 if the generator is not used by the RTC and not a source of a 'locked' generic clock No change if the generator is used by the RTC or used by a GCLK with a WRTLOCK as one
0x03	0x00000003 if the generator is not used by the RTC and not a source of a 'locked' generic clock No change if the generator is used by the RTC or used by a GCLK with a WRTLOCK as one

19.8.17 Status

Name: STATUS
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	SYNCBUSY							
Access	R							
Reset	0							

Bit 7 – SYNCBUSY: Synchronization Busy
This bit is cleared when the synchronization of registers between the clock domains is complete.

This bit is set when the synchronization of registers between clock domains is started.

19.8.18 Debug Control

Name: DBGCTRL
Offset: 0x0B
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN: Run During Debug
This bit is not reset by a software reset.

Writing a zero to this bit causes the RTC to halt during debug mode.

Writing a one to this bit allows the RTC to continue normal operation during debug mode.

19.8.19 Frequency Correction

Name: FREQCORR
Offset: 0x0C
Reset: 0x00
Property: Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	SIGN	VALUE[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – SIGN: Correction Sign

Bits 19:16 – LVLPRI2[3:0]: Level 2 Channel Priority Number
When round-robin arbitration is enabled (PRICTRL0.RRLVLEN2=1) for priority level 2, this register holds the channel number of the last DMA channel being granted access as the active channel with priority level 2.

When static arbitration is enabled (PRICTRL0.RRLVLEN2=0) for priority level 2, and the value of this bit group is non-zero, it will not affect the static priority scheme.

This bit group is not reset when round-robin arbitration gets disabled (PRICTRL0.RRLVLEN2 written to '0').

Bit 15 – RRLVLEN1: Level 1 Round-Robin Scheduling Enable
For details on arbitration schemes, refer to Arbitration.

Value	Description
0	Static arbitration scheme for channels with level 1 priority.
1	Round-robin arbitration scheme for channels with level 1 priority.

Bits 11:8 – LVLPRI1[3:0]: Level 1 Channel Priority Number
When round-robin arbitration is enabled (PRICTRL0.RRLVLEN1=1) for priority level 1, this register holds the channel number of the last DMA channel being granted access as the active channel with priority level 1.

When static arbitration is enabled (PRICTRL0.RRLVLEN1=0) for priority level 1, and the value of this bit group is non-zero, it will not affect the static priority scheme.

This bit group is not reset when round-robin arbitration gets disabled (PRICTRL0.RRLVLEN1 written to '0').

Bit 7 – RRLVLEN0: Level 0 Round-Robin Scheduling Enable
For details on arbitration schemes, refer to Arbitration.

Value	Description
0	Static arbitration scheme for channels with level 0 priority.
1	Round-robin arbitration scheme for channels with level 0 priority.

Bits 3:0 – LVLPRI0[3:0]: Level 0 Channel Priority Number
When round-robin arbitration is enabled (PRICTRL0.RRLVLEN0=1) for priority level 0, this register holds the channel number of the last DMA channel being granted access as the active channel with priority level 0.

When static arbitration is enabled (PRICTRL0.RRLVLEN0=0) for priority level 0, and the value of this bit group is non-zero, it will not affect the static priority scheme.

This bit group is not reset when round-robin arbitration gets disabled (PRICTRL0.RRLVLEN0 written to '0').

20.8.10 Interrupt Pending

This register allows the user to identify the lowest DMA channel with pending interrupt.

Name: INTPEND
Offset: 0x20
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
	DESCADDR[15:8]							
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	DESCADDR[7:0]							
Access								
Reset								

Bits 31:0 – DESCADDR[31:0]: Next Descriptor Address
This bit group holds the SRAM address of the next descriptor. The value must be 128-bit aligned. If the value of this SRAM register is 0x00000000, the transaction will be terminated when the DMAC tries to load the next transfer descriptor.

21.5.5 Interrupts

There are two interrupt request lines, one for the external interrupts (EXTINT) and one for non-maskable interrupt (NMI).

The EXTINT interrupt request line is connected to the interrupt controller. Using the EIC interrupt requires the interrupt controller to be configured first.

The NMI interrupt request line is also connected to the interrupt controller, but does not require the interrupt to be configured.

Related Links

Nested Vector Interrupt Controller

21.5.6 Events

The events are connected to the Event System. Using the events requires the Event System to be configured first.

Related Links

EVSYS – Event System

21.5.7 Debug Operation

When the CPU is halted in debug mode, the EIC continues normal operation. If the EIC is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

21.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Flag Status and Clear register (INTFLAG)
- Non-Maskable Interrupt Flag Status and Clear register (NMIFLAG)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

21.5.9 Analog Connections

Not applicable.

21.6 Functional Description

21.6.1 Principle of Operation

The EIC detects edge or level condition to generate interrupts to the CPU interrupt controller or events to the Event System. Each external interrupt pin (EXTINT) can be filtered using majority vote filtering, clocked by GCLK_EIC

21.6.2 Basic Operation

21.6.2.1 Initialization

The EIC must be initialized in the following order:

Bits 31:20 – RWWEEP[11:0]: Read While Write EEPROM emulation area Pages
Indicates the number of pages in the RWW EEPROM emulation address space.

Bits 18:16 – PSZ[2:0]: Page Size
Indicates the page size. Not all devices of the device families will provide all the page sizes indicated in the table.

Value	Name	Description
0x0	8	8 bytes
0x1	16	16 bytes
0x2	32	32 bytes
0x3	64	64 bytes
0x4	128	128 bytes
0x5	256	256 bytes
0x6	512	512 bytes
0x7	1024	1024 bytes

Bits 15:0 – NVMP[15:0]: NVM Pages
Indicates the number of pages in the NVM main address space.

22.8.4 Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Name: INTENCLR
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
							ERROR	READY
Access							R/W	R/W
Reset							0	0

Bit 1 – ERROR: Error Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the ERROR interrupt enable.

This bit will read as the current value of the ERROR interrupt enable.

Bit 0 – READY: NVM Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the READY interrupt enable.

This bit will read as the current value of the READY interrupt enable.

22.8.5 Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	SAMPLING[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SAMPLING[31:0]: Input Sampling Mode
Configures the input sampling functionality of the I/O pin input samplers, for pins configured as inputs via the Data Direction register (DIR).

The input samplers are enabled and disabled in sub-groups of eight. Thus if any pins within a byte request continuous sampling, all pins in that eight pin sub-group will be continuously sampled.

Value	Description
0	The I/O pin input synchronizer is disabled.
1	The I/O pin input synchronizer is enabled.

23.8.11 Write Configuration

This write-only register is used to configure several pins simultaneously with the same configuration and/or peripheral multiplexing.

In order to avoid side effect of non-atomic access, 8-bit or 16-bit writes to this register will have no effect. Reading this register always returns zero.

Name: WRCONFIG
Offset: 0x28
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	HWSEL	WRPINCFG		WRPMUX	PMUX[3:0]			
Access	W	W		W	W	W	W	W
Reset	0	0		0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		DRVSTR				PULLEN	INEN	PMUXEN
Access		W				W	W	W
Reset		0				0	0	0

Bit	15	14	13	12	11	10	9	8
	PINMASK[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PINMASK[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

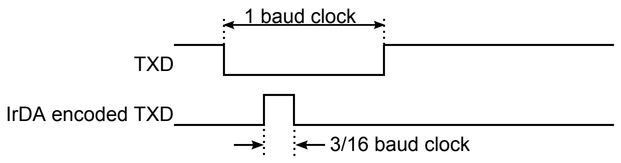
Bit 31 – HWSEL: Half-Word Select
This bit selects the half-word field of a 32-PORT group to be reconfigured in the atomic write operation.

This bit will always read as zero.

- and 16x sample rate (CTRLA.SAMPR[0]=0).

During transmission, each low bit is transmitted as a high pulse. The pulse width is 3/16 of the baud rate period, as illustrated in the figure below.

Figure 26-10. IrDA Transmit Encoding



The reception decoder has two main functions.

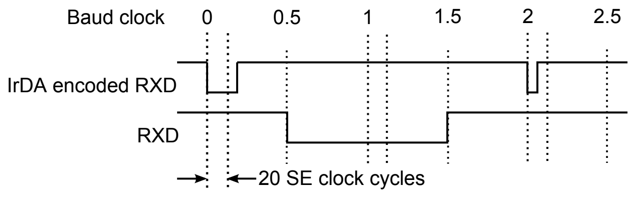
The first is to synchronize the incoming data to the IrDA baud rate counter. Synchronization is performed at the start of each zero pulse.

The second main function is to decode incoming Rx data. If a pulse width meets the minimum length set by configuration (RXPL.RXPL), it is accepted. When the baud rate counter reaches its middle value (1/2 bit length), it is transferred to the receiver.

Note: Note that the polarity of the transmitter and receiver are opposite: During transmission, a '0' bit is transmitted as a '1' pulse. During reception, an accepted '0' pulse is received as a '0' bit.

Example: The figure below illustrates reception where RXPL.RXPL is set to 19. This indicates that the pulse width should be at least 20 SE clock cycles. When using BAUD=0xE666 or 160 SE cycles per bit, this corresponds to 2/16 baud clock as minimum pulse width required. In this case the first bit is accepted as a '0', the second bit is a '1', and the third bit is also a '1'. A low pulse is rejected since it does not meet the minimum requirement of 2/16 baud clock.

Figure 26-11. IrDA Receive Decoding



26.6.3.4 Break Character Detection and Auto-Baud

Break character detection and auto-baud are available in this configuration:

- Auto-baud frame format (CTRLA.FORM = 0x04 or 0x05),
- Asynchronous mode (CTRLA.CMODE = 0),
- and 16x sample rate using fractional baud rate generation (CTRLA.SAMPR = 1).

The auto-baud follows the LIN format. All LIN Frames start with a Break Field followed by a Sync Field. The USART uses a break detection threshold of greater than 11 nominal bit times at the configured baud rate. At any time, if more than 11 consecutive dominant bits are detected on the bus, the USART detects a Break Field. When a Break Field has been detected, the Receive Break interrupt flag (INTFLAG.RXBRK) is set and the USART expects the Sync Field character to be 0x55. This field is used to update the actual baud rate in order to stay synchronized. If the received Sync character is not 0x55, then the Inconsistent Sync Field error flag (STATUS.ISF) is set along with the Error interrupt flag (INTFLAG.ERROR), and the baud rate is unchanged.

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)

Optional PAC Write-Protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller

27.5.9 Analog Connections

Not applicable.

27.6 Functional Description

27.6.1 Principle of Operation

The SPI is a high-speed synchronous data transfer interface It allows high-speed communication between the device and peripheral devices.

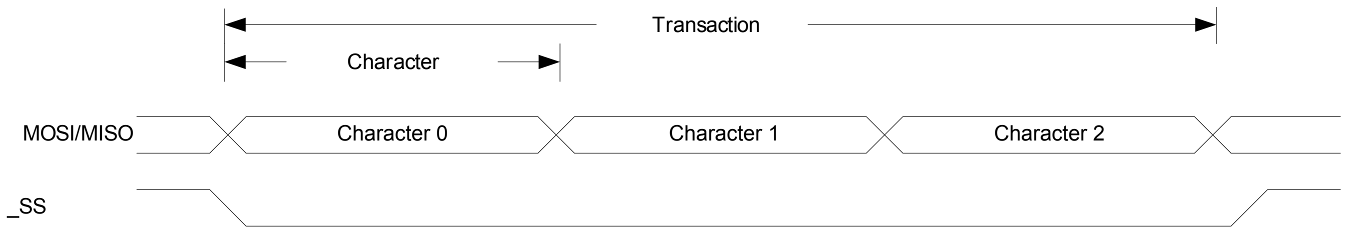
The SPI can operate as master or slave. As master, the SPI initiates and controls all data transactions. The SPI is single buffered for transmitting and double buffered for receiving.

When transmitting data, the Data register can be loaded with the next character to be transmitted during the current transmission.

When receiving, the data is transferred to the two-level receive buffer, and the receiver is ready for a new character.

The SPI transaction format is shown in SPI Transaction Format. Each transaction can contain one or more characters. The character size is configurable, and can be either 8 or 9 bits.

Figure 27-2. SPI Transaction Format



The SPI master must pull the slave select line ($\overline{SS}$) of the desired slave low to initiate a transaction. The master and slave prepare data to send via their respective shift registers, and the master generates the serial clock on the SCK line.

Data are always shifted from master to slave on the Master Output Slave Input line (MOSI); data is shifted from slave to master on the Master Input Slave Output line (MISO).

Each time character is shifted out from the master, a character will be shifted out from the slave simultaneously. To signal the end of a transaction, the master will pull the $\overline{SS}$ line high

27.6.2 Basic Operation

27.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the SPI is disabled (CTRL.ENABLE=0):

This frequency can be achieved by dividing the I^{2}S generic clock output of 18.432MHz by factor 2: Writing CLKCTRLn.MCKDIV=0x1 will select the correct division factor and output the desired SCKn frequency of 9.216MHz to the SCKn pin.

If MCKn is not required, the generic clock could be set to 9.216MHz and CLKCTRLn.MCKDIV=0x0.

29.6.2 Basic Operation

The Receiver can be operated by reading the Data Holding register (DATAm), whenever the Receive Ready m bit in the Interrupt Flag Status and Clear register (INTFLAG.RXRDYm) is set. Successive values read from DATAm register will correspond to the samples from the left and right audio channels. In TDM mode, the successive values read from DATAm register correspond to the first slot to the last slot. For instance, if I^{2}S is configured in TDM mode with 4 slots in a frame, then successive values written to DATAm register correspond to first, second, third, and fourth slot. The number of slots in TDM is configured in CLKCTRLn.NBSLOTS.

The Transmitter can be operated by writing to the Data Holding register (DATAm), whenever the Transmit Ready m bit in the Interrupt Flag Status and Clear register (INTFLAG.TXRDYm) is set. Successive values written to DATAm register should correspond to the samples from the left and right audio channels. In TDM mode, the successive values written to DATAm register correspond to the first, second, third, slot to the last slot. The number of slots in TDM is configured in CLKCTRLn.NBSLOTS.

The Receive Ready and Transmit Ready bits can be polled by reading the INTFLAG register.

The processor load can be reduced by enabling interrupt-driven operation. The RXRDYm and/or TXRDYm interrupt requests can be enabled by writing a '1' to the corresponding bit in the Interrupt Enable register (INTENSET). The interrupt service routine associated to the I^{2}S interrupt request will then be executed whenever Receive Ready or Transmit Ready status bits are set.

The processor load can be reduced further by enabling DMA-driven operation. Then, the DMA channels support up to four trigger sources from the I^{2}S peripheral. These four trigger sources in DMAC channel are

- I2S RX 0,
- I2S RX 1,
- I2S TX 0, and
- I2S TX 1.

For further reference, these are called I2S_DMAC_ID_RX_m and I2S_DMAC_ID_TX_m triggers (m=0..1). By using these trigger sources, one DMA data transfer will be executed whenever the Receive Ready or Transmit Ready status bits are set.

29.6.2.1 Master Clock, Serial Clock, and Frame Sync Generation

The generation of clocks in the I^{2}S is described in the next figure.

Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
			TXUR1	TXUR0			TXRDY1	TXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
			RXOR1	RXOR0			RXRDY1	RXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 13,12 – TXURx : Transmit Underrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Underrun x Interrupt Enable bit, which disables the Transmit Underrun x interrupt.

Value	Description
0	The Transmit Underrun x interrupt is disabled.
1	The Transmit Underrun x interrupt is enabled.

Bits 9,8 – TXRDYx : Transmit Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Ready x Interrupt Enable bit, which disables the Transmit Ready x interrupt.

Value	Description
0	The Transmit Ready x interrupt is disabled.
1	The Transmit Ready x interrupt is enabled.

Bits 4,5 – RXORx : Receive Overrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Overrun x Interrupt Enable bit, which disables the Receive Overrun x interrupt.

Value	Description
0	The Receive Overrun x interrupt is disabled.
1	The Receive Overrun x interrupt is enabled.

Bits 1,0 – RXRDYx : Receive Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Ready x Interrupt Enable bit, which disables the Receive Ready x interrupt.

Value	Description
0	The Receive Ready x interrupt is disabled.
1	The Receive Ready x interrupt is enabled.

Bit 6 – BK0RDY: Bank 0 is ready
Writing a one to the bit EPSTATUSCLR.BK0RDY will clear this bit.

Writing a one to the bit EPSTATUSSET.BK0RDY will set this bit.

Value	Description
0	The bank number 0 is not ready : For IN direction Endpoints, the bank is not yet filled in. For Control/OUT direction Endpoints, the bank is empty.
1	The bank number 0 is ready: For IN direction Endpoints, the bank is filled in. For Control/OUT direction Endpoints, the bank is full.

Bit 4 – STALLRQ: STALL bank x request
Writing a zero to the bit EPSTATUSCLR.STALLRQ will clear this bit.

Writing a one to the bit EPSTATUSSET.STALLRQ will set this bit.

This bit is cleared by hardware when receiving a SETUP packet.

Value	Description
0	Disable STALLRQx feature.
1	Enable STALLRQx feature: a STALL handshake will be sent to the host in regards to bank x.

Bit 2 – CURBK: Current Bank
Writing a zero to the bit EPSTATUSCLR.CURBK will clear this bit.

Writing a one to the bit EPSTATUSSET.CURBK will set this bit.

Value	Description
0	The bank0 is the bank that will be used in the next single/multi USB packet.
1	The bank1 is the bank that will be used in the next single/multi USB packet.

Bit 1 – DTGLIN: Data Toggle IN Sequence
Writing a zero to the bit EPSTATUSCLR.DTGLINCLR will clear this bit.

Writing a one to the bit EPSTATUSSET.DTGLINSET will set this bit.

Value	Description
0	The PID of the next expected IN transaction will be zero: data 0.
1	The PID of the next expected IN transaction will be one: data 1.

Bit 0 – DTGLOUT: Data Toggle OUT Sequence
Writing a zero to the bit EPSTATUSCLR.DTGLOUTCLR will clear this bit.

Writing a one to the bit EPSTATUSSET.DTGLOUTSET will set this bit.

Value	Description
0	The PID of the next expected OUT transaction will be zero: data 0.
1	The PID of the next expected OUR transaction will be one: data 1.

32.8.3.5 Device EndPoint Interrupt Flag n

Name:	EPINTFLAGn
Offset:	0x107 + (n x 0x20)
Reset:	0x00
Property:	-

Value	Description
0	The Upstream Resume interrupt is disabled.
1	The Upstream Resume interrupt is enabled.

Bit 5 – DNRSM: Down Resume Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Down Resume interrupt Enable bit and enable the DNRSM interrupt.

Value	Description
0	The Down Resume interrupt is disabled.
1	The Down Resume interrupt is enabled.

Bit 4 – WAKEUP: Wake Up Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Wake Up interrupt Enable bit and enable the WAKEUP interrupt request.

Value	Description
0	The WakeUp interrupt is disabled.
1	The WakeUp interrupt is enabled.

Bit 3 – RST: Bus Reset Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Bus Reset interrupt Enable bit and enable the Bus RST interrupt.

Value	Description
0	The Bus Reset interrupt is disabled.
1	The Bus Reset interrupt is enabled.

Bit 2 – HSOF: Host Start-of-Frame Interrupt Enable
Writing a zero to this bit has no effect.

Writing a one to this bit will set the Host Start-of-Frame interrupt Enable bit and enable the HSOF interrupt.

Value	Description
0	The Host Start-of-Frame interrupt is disabled.
1	The Host Start-of-Frame interrupt is enabled.

32.8.5.8 Host Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x1C
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
							DDISC	DCONN
Access							R/W	R/W
Reset							0	0

PRESCALER[2:0]	Name	Description
0x2	DIV16	Peripheral clock divided by 16
0x3	DIV32	Peripheral clock divided by 32
0x4	DIV64	Peripheral clock divided by 64
0x5	DIV128	Peripheral clock divided by 128
0x6	DIV256	Peripheral clock divided by 256
0x7	DIV512	Peripheral clock divided by 512

Bits 5:4 – RESSEL[1:0]: Conversion Result Resolution
These bits define whether the ADC completes the conversion at 12-, 10- or 8-bit result resolution.

RESSEL[1:0]	Name	Description
0x0	12BIT	12-bit result
0x1	16BIT	For averaging mode output
0x2	10BIT	10-bit result
0x3	8BIT	8-bit result

Bit 3 – CORREN: Digital Correction Logic Enabled

Value	Description
0	Disable the digital result correction.
1	Enable the digital result correction. The ADC conversion result in the RESULT register is then corrected for gain and offset based on the values in the GAINCAL and OFFSETCAL registers. Conversion time will be increased by X cycles according to the value in the Offset Correction Value bit group in the Offset Correction register.

Bit 2 – FREERUN: Free Running Mode

Value	Description
0	The ADC run is single conversion mode.
1	The ADC is in free running mode and a new conversion will be initiated when a previous conversion completes.

Bit 1 – LEFTADJ: Left-Adjusted Result

Value	Description
0	The ADC conversion result is right-adjusted in the RESULT register.
1	The ADC conversion result is left-adjusted in the RESULT register. The high byte of the 12-bit result will be present in the upper part of the result register. Writing this bit to zero (default) will right-adjust the value in the RESULT register.

Bit 0 – DIFFMODE: Differential Mode

Value	Description
0	The ADC is running in singled-ended mode.
1	The ADC is running in differential mode. In this mode, the voltage difference between the MUXPOS and MUXNEG inputs will be converted by the ADC.

33.8.6 Window Monitor Control

Name: WINCTRL
Offset: 0x08
Reset: 0x00
Property: Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
						WINMODE[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – WINMODE[2:0]: Window Monitor Mode
These bits enable and define the window monitor mode.

WINMODE[2:0]	Name	Description
0x0	DISABLE	No window mode (default)
0x1	MODE1	Mode 1: RESULT > WINLT
0x2	MODE2	Mode 2: RESULT < WINUT
0x3	MODE3	Mode 3: WINLT < RESULT < WINUT
0x4	MODE4	Mode 4: !(WINLT < RESULT < WINUT)
0x5-0x7		Reserved

33.8.7 Software Trigger

Name: SWTRIG
Offset: 0x0C
Reset: 0x00
Property: Write-Protected, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							START	FLUSH
Access							R/W	R/W
Reset							0	0

Bit 1 – START: ADC Start Conversion
Writing this bit to zero will have no effect.

Value	Description
0	The ADC will not start a conversion.
1	The ADC will start a conversion. The bit is cleared by hardware when the conversion has started. Setting this bit when it is already set has no effect.

Bit 0 – FLUSH: ADC Conversion Flush
After the flush, the ADC will resume where it left off; i.e., if a conversion was pending, the ADC will start a new conversion.

Property: Read-Synchronized

Bit	15	14	13	12	11	10	9	8
	RESULT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RESULT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RESULT[15:0]: Result Conversion Value
These bits will hold up to a 16-bit ADC result, depending on the configuration.

In single conversion mode without averaging, the ADC conversion will produce a 12-bit result, which can be left- or right-shifted, depending on the setting of CTRLB.LEFTADJ.

If the result is left-adjusted (CTRLB.LEFTADJ), the high byte of the result will be in bit position [15:8], while the remaining 4 bits of the result will be placed in bit locations [7:4]. This can be used only if an 8-bit result is required; i.e., one can read only the high byte of the entire 16-bit register.

If the result is not left-adjusted (CTRLB.LEFTADJ) and no oversampling is used, the result will be available in bit locations [11:0], and the result is then 12 bits long.

If oversampling is used, the result will be located in bit locations [15:0], depending on the settings of the Average Control register (AVGCTRL).

33.8.15 Window Monitor Lower Threshold

Name: WINLT
Offset: 0x1C
Reset: 0x0000
Property: Write-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	WINLT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WINLT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WINLT[15:0]: Window Lower Threshold
If the window monitor is enabled, these bits define the lower threshold value.

33.8.16 Window Monitor Upper Threshold

Name: WINUT

  - V_{VDDIN} = 3.3 V
- Oscillators
  - XOSC32K (32 kHz crystal oscillator) running with external 32kHz crystal in USB Host mode
- Clocks
  - USB Device mode: DFLL48M in USB recovery mode (Crystal less)
  - USB Host mode: DFLL48M in closed loop with XOSC32K (32 kHz crystal oscillator) running with external 32kHz crystal
  - CPU, AHB and APBn clocks undivided
- The following AHB module clocks are running: NVMCTRL, HPB2 bridge, HPB1 bridge, HPB0 bridge
  - All other AHB clocks stopped
- I/Os are inactive with internal pull-up
- CPU in IDLE0 mode
- Cache enabled
- BOD33 disabled

In this default conditions, the power consumption $I_{default}$ is measured.

Measurements do not include consumption of clock source (ex: DFLL48M or FDPLL96M) and CPU. However no CPU activity is required during all states (Suspend, IDLE, Data transfer).

Measurements have been done with an USB cable of 1.5m.

For USB Device mode, measurements include the maximum consumption (200µA) through pull-up resistor on the D+ line for USB attach. This value depends on USB Host characteristic.

Operating modes:

- Run the USB Device/Host states in regards of the Universal Serial Bus (USB) v2.0 standard.

USB power consumption is provided in the following tables.

Table 37-12. Typical USB Device Full Speed mode Current Consumption

USB Device state	Conditions	Typ.	Units
Suspend	GCLK_USB is off, using USB wakeup asynchronous interrupt. USB bus in suspend mode.	201	µA
Suspend	GCLK_USB is on. USB bus in suspend mode.	0.83	mA
IDLE	Start Of Frame is running. No packet transferred.	1.17	mA
Active OUT	Start Of Frame is running. Bulk OUT on 100% bandwidth.	2.17	mA
Active IN	Start Of Frame is running. Bulk IN on 100% bandwidth.	10.3	mA

$$\left(\frac{V_{\mathrm{ADC}}+-V_{\mathrm{ADCR}}}{\mathrm{temp}+-\mathrm{temp}_R}\right)=\left(\frac{V_{\mathrm{ADCH}}+-V_{\mathrm{ADCR}}}{\mathrm{temp}_H+-\mathrm{temp}_R}\right)$$

Given a temperature sensor ADC conversion value ADC_m, we can infer a coarse value of the temperature temp_C as:

$$\mathrm{temp}_C=\mathrm{temp}_R+\left[\frac{\left\{\left(\mathrm{ADC}_m\cdot\frac{1}{\left(2^{12}+-1\right)}\right)+-\left(\mathrm{ADC}_R\cdot\frac{\mathrm{INT1}V_R}{\left(2^{12}+-1\right)}\right)\right\}\cdot\left(\mathrm{temp}_H+-\mathrm{temp}_R\right)}{\left\{\left(\mathrm{ADC}_H\cdot\frac{\mathrm{INT1}V_H}{\left(2^{12}+-1\right)}\right)+-\left(\mathrm{ADC}_R\cdot\frac{\mathrm{INT1}V_R}{\left(2^{12}+-1\right)}\right)\right\}}\right]$$

[Equation 1]

Note:

1. In the previous expression, we have added the conversion of the ADC register value to be expressed in V.
2. This is a coarse value because we assume INT1V=1V for this ADC conversion.

Using the (temp_R, $\mathrm{INT1V}_R$) and (temp_H, $\mathrm{INT1V}_H$) points, using a linear interpolation we have the following equation:

$$\left(\frac{\mathrm{INT1}V+-\mathrm{INT1}V_R}{\mathrm{temp}+-\mathrm{temp}_R}\right)=\left(\frac{\mathrm{INT1}V_H+-\mathrm{INT1}V_R}{\mathrm{temp}_H+-\mathrm{temp}_R}\right)$$

Then using the coarse temperature value, we can infer a closer to reality INT1V value during the ADC conversion as:

$$\mathrm{INT1}V_m=\mathrm{INT1}V_R+\left(\frac{\left(\mathrm{INT1}V_H+-\mathrm{INT1}V_R\right)\cdot\left(\mathrm{temp}_C+-\mathrm{temp}_R\right)}{\left(\mathrm{temp}_H+-\mathrm{temp}_R\right)}\right)$$

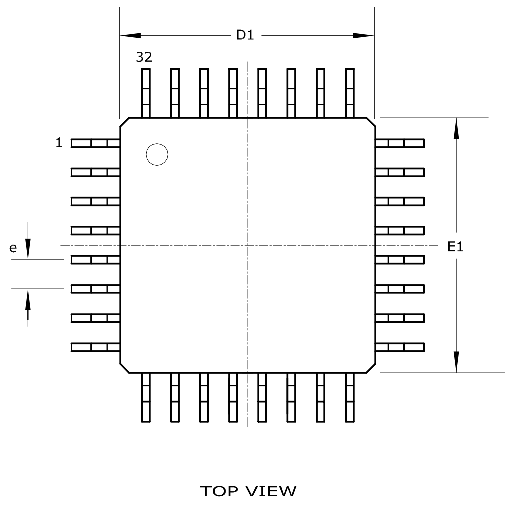
Back to [Equation 1], if we replace INT1V=1V by INT1V = $\mathrm{INT1V}_m$, we can deduce a finer temperature value as:

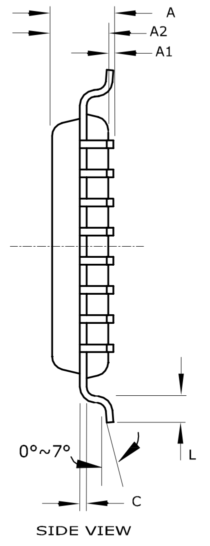
$$\mathrm{temp}_f=\mathrm{temp}_R+\left[\frac{\left\{\left(\mathrm{ADC}_m\cdot\frac{\mathrm{INT1}V_m}{\left(2^{12}+-1\right)}\right)+-\left(\mathrm{ADC}_R\cdot\frac{\mathrm{INT1}V_R}{\left(2^{12}+-1\right)}\right)\right\}\cdot\left(\mathrm{temp}_H\cdot\mathrm{temp}_R\right)}{\left\{\left(\mathrm{ADC}_H\cdot\frac{\mathrm{INT1}V_H}{\left(2^{12}+-1\right)}\right)+-\left(\mathrm{ADC}_R\cdot\frac{\mathrm{INT1}V_R}{\left(2^{12}+-1\right)}\right)\right\}}\right]$$

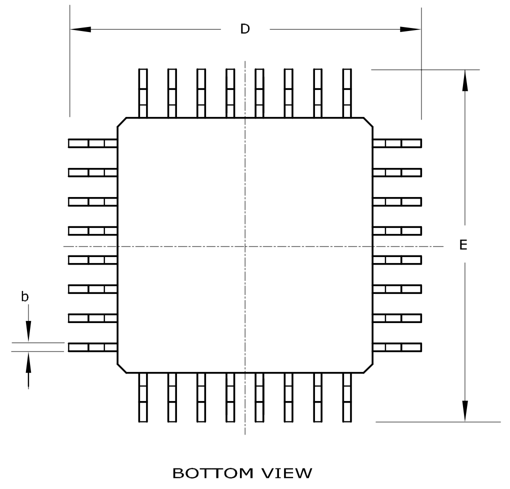
[Equation 1bis]

38.2.7 32 pin TQFP

DRAWINGS NOT SCALED







COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: **packagedrawings@atmel.com**	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

Table 38-20. Device and Package Maximum Weight

100	mg

Table 38-21. Package Charateristics

Moisture Sensitivity Level	MSL3