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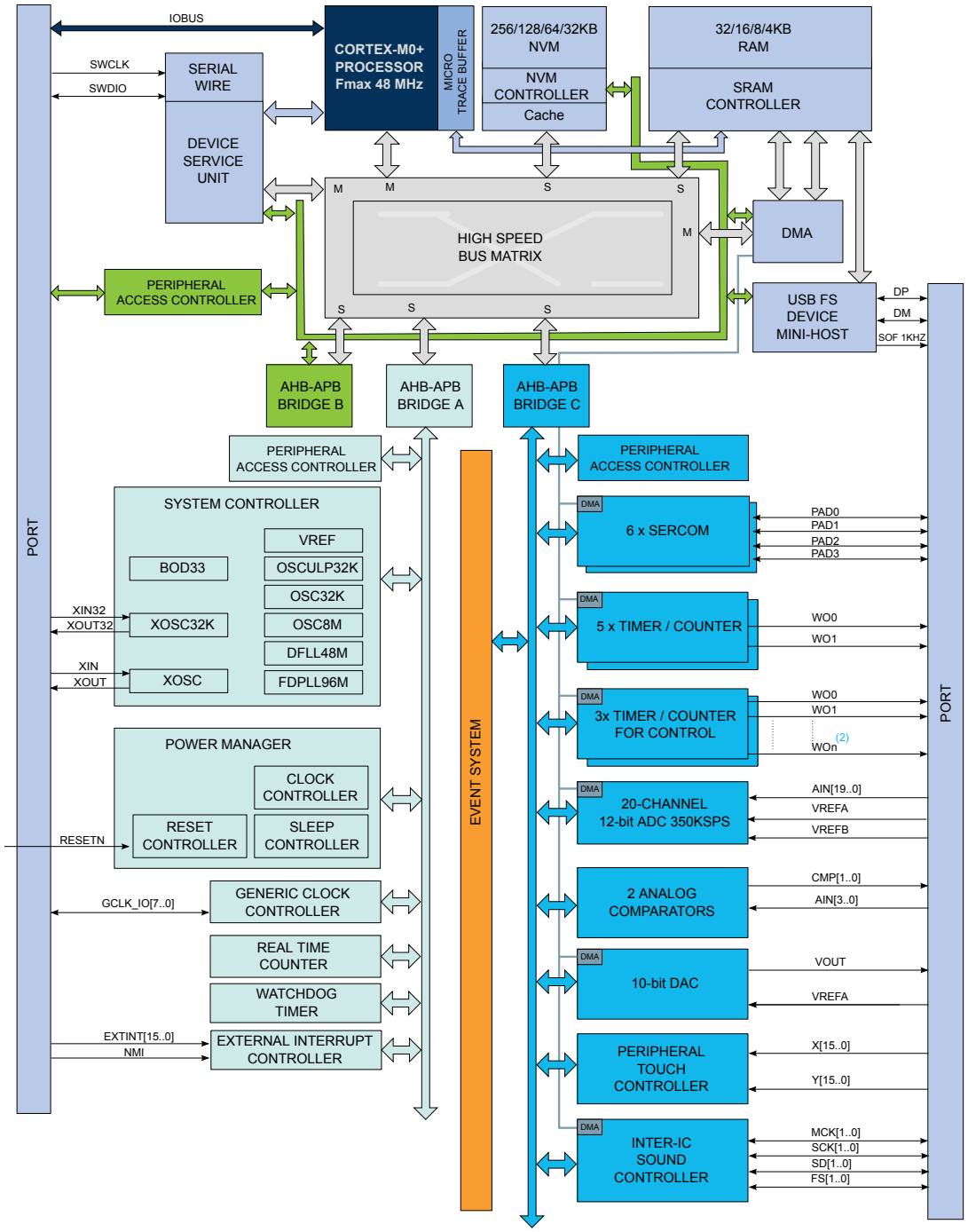
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 38 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 14x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g17a-aft |

# 4. Block Diagram




1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to the Configuration Summary for details.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines. Refer to the TCC Configuration for details.

**Related Links**

Configuration Summary

TCC Configurations

**Related Links**

Electrical Characteristics

## 8.3 Power-Up

This section summarizes the power-up sequence of the device. The behavior after power-up is controlled by the Power Manager. Refer to *PM – Power Manager* for details.

**Related Links**

PM – Power Manager

### 8.3.1 Starting of Clocks

After power-up, the device is set to its initial state and kept in reset, until the power has stabilized throughout the device. Once the power has stabilized, the device will use a 1MHz clock. This clock is derived from the 8MHz Internal Oscillator (OSC8M), which is divided by eight and used as a clock source for generic clock generator 0. Generic clock generator 0 is the main clock for the Power Manager (PM).

Some synchronous system clocks are active, allowing software execution.

Refer to the “Clock Mask Register” section in *PM – Power Manager* for the list of default peripheral clocks running. Synchronous system clocks that are running are by default not divided and receive a 1MHz clock through generic clock generator 0. Other generic clocks are disabled except GCLK_WDT, which is used by the Watchdog Timer (WDT).

**Related Links**

PM – Power Manager

### 8.3.2 I/O Pins

After power-up, the I/O pins are tri-stated.

### 8.3.3 Fetching of Initial Instructions

After reset has been released, the CPU starts fetching PC and SP values from the reset address, which is 0x00000000. This address points to the first executable address in the internal flash. The code read from the internal flash is free to configure the clock system and clock sources. Refer to *PM – Power Manager*, *GCLK – Generic Clock Controller* and *SYSCTRL – System Controller* for details. Refer to the ARM Architecture Reference Manual for more information on CPU startup (http://www.arm.com).

**Related Links**

PM – Power Manager

SYSCTRL – System Controller

Clock System

## 8.4 Power-On Reset and Brown-Out Detector

The SAM D21 embeds three features to monitor, warn and/or reset the device:

- POR: Power-on reset on VDDANA
- BOD33: Brown-out detector on VDDANA
- BOD12: Voltage Regulator Internal Brown-out detector on VDDCORE. The Voltage Regulator Internal BOD is calibrated in production and its calibration configuration is stored in the NVM User Row. This configuration should not be changed if the user row is written to assure the correct behavior of the BOD12.

**Related Links**

PM – Power Manager

### 15.5.3 Clocks

The GCLK bus clock (CLK_GCLK_APB) can be enabled and disabled in the Power Manager, and the default state of CLK_GCLK_APB can be found in the Peripheral Clock Masking section of PM – Power Manager.

**Related Links**

PM – Power Manager

### 15.5.4 DMA

Not applicable.

### 15.5.5 Interrupts

Not applicable.

### 15.5.6 Events

Not applicable.

### 15.5.7 Debug Operation

Not applicable.

### 15.5.8 Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

**Note:** Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

**Related Links**

PAC - Peripheral Access Controller

### 15.5.9 Analog Connections

Not applicable.

## 15.6 Functional Description

### 15.6.1 Principle of Operation

The GCLK module is comprised of eight Generic Clock Generators (Generators) sourcing m Generic Clock Multiplexers.

A clock source selected as input to a Generator can either be used directly, or it can be prescaled in the Generator. A generator output is used as input to one or more the Generic Clock Multiplexers to provide a peripheral (GCLK_PERIPHERAL). A generic clock can act as the clock to one or several of peripherals.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | CPUDIV[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 2:0 – CPUDIV[2:0]: CPU Prescaler Selection**
These bits define the division ratio of the main clock prescaler ($2^n$).

| CPUDIV[2:0] | Name | Description |
|---|---|---|
| 0x0 | DIV1 | Divide by 1 |
| 0x1 | DIV2 | Divide by 2 |
| 0x2 | DIV4 | Divide by 4 |
| 0x3 | DIV8 | Divide by 8 |
| 0x4 | DIV16 | Divide by 16 |
| 0x5 | DIV32 | Divide by 32 |
| 0x6 | DIV64 | Divide by 64 |
| 0x7 | DIV128 | Divide by 128 |

### 16.8.4 APBA Clock Select

**Name:** APBASEL
**Offset:** 0x09
**Reset:** 0x00
**Property:** Write-Protected

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | APBADIV[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 2:0 – APBADIV[2:0]: APBA Prescaler Selection**
These bits define the division ratio of the APBA clock prescaler ($2^n$).

| APBADIV[2:0] | Name | Description |
|---|---|---|
| 0x0 | DIV1 | Divide by 1 |
| 0x1 | DIV2 | Divide by 2 |
| 0x2 | DIV4 | Divide by 4 |
| 0x3 | DIV8 | Divide by 8 |
| 0x4 | DIV16 | Divide by 16 |
| 0x5 | DIV32 | Divide by 32 |
| 0x6 | DIV64 | Divide by 64 |
| 0x7 | DIV128 | Divide by 128 |

Writing a one to this bit will clear the OSC8M Ready Interrupt Enable bit, which disables the OSC8M Ready interrupt.

| Value | Description |
|---|---|
| 0 | The OSC8M Ready interrupt is disabled. |
| 1 | The OSC8M Ready interrupt is enabled, and an interrupt request will be generated when the OSC8M Ready Interrupt flag is set. |

**Bit 2 – OSC32KRDY: OSC32K Ready Interrupt Enable**
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the OSC32K Ready Interrupt Enable bit, which disables the OSC32K Ready interrupt.

| Value | Description |
|---|---|
| 0 | The OSC32K Ready interrupt is disabled. |
| 1 | The OSC32K Ready interrupt is enabled, and an interrupt request will be generated when the OSC32K Ready Interrupt flag is set. |

**Bit 1 – XOSC32KRDY: XOSC32K Ready Interrupt Enable**
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the XOSC32K Ready Interrupt Enable bit, which disables the XOSC32K Ready interrupt.

| Value | Description |
|---|---|
| 0 | The XOSC32K Ready interrupt is disabled. |
| 1 | The XOSC32K Ready interrupt is enabled, and an interrupt request will be generated when the XOSC32K Ready Interrupt flag is set. |

**Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable**
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the XOSC Ready Interrupt Enable bit, which disables the XOSC Ready interrupt.

| Value | Description |
|---|---|
| 0 | The XOSC Ready interrupt is disabled. |
| 1 | The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the XOSC Ready Interrupt flag is set. |

### 17.8.2 Interrupt Enable Set

**Name:** INTENSET
**Offset:** 0x04
**Reset:** 0x00000000
**Property:** Write-Protected

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | LDRFRAC[3:0] | | | |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | LDR[11:8] | | | |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | LDR[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 19:16 – LDRFRAC[3:0]: Loop Divider Ratio Fractional Part**
Write this field with the fractional part of the frequency multiplier.

**Bits 11:0 – LDR[11:0]: Loop Divider Ratio**
Write this field with the integer part of the frequency multiplier.

### 17.8.19 DPLL Control B

**Name:** DPLLCTRLB
**Offset:** 0x4C
**Reset:** 0x00000000
**Property:** Write-Protected

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | DIV[10:8] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | DIV[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | LBYPASS | | LTIME[2:0] | | |
| Access | | | | R/W | | R/W | R/W | R/W |
| Reset | | | | 0 | | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | REFCLK[1:0] | | WUF | LPEN | FILTER[1:0] | |
| Access | | | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 26:16 – DIV[10:0]: Clock Divider**
These bits are used to set the XOSC clock source division factor. Refer to Principle of Operation.

## 19.3 Block Diagram

**Figure 19-1. RTC Block Diagram (Mode 0 — 32-Bit Counter)**

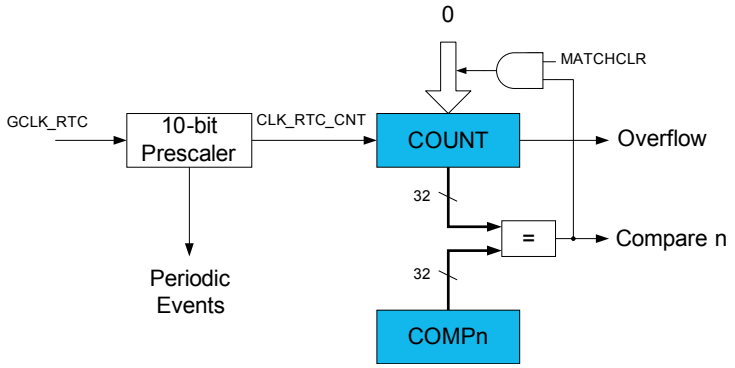



**Figure 19-2. RTC Block Diagram (Mode 1 — 16-Bit Counter)**

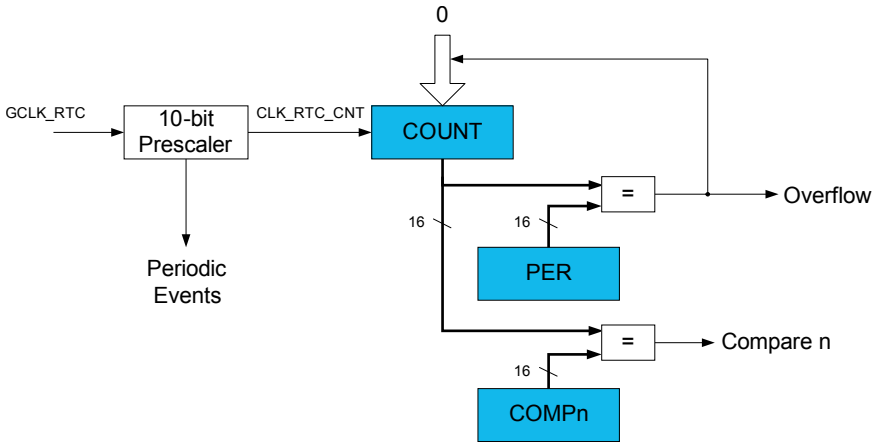
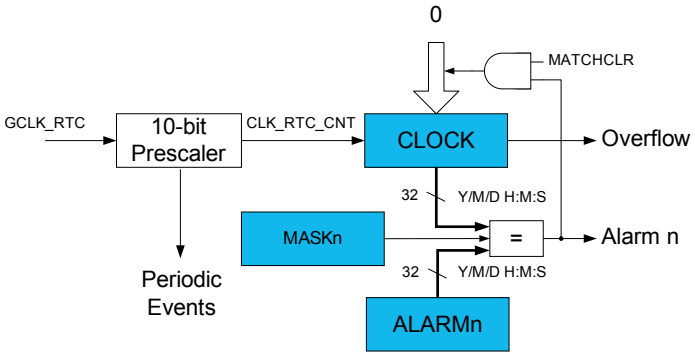



**Figure 19-3. RTC Block Diagram (Mode 2 — Clock/Calendar)**




## 19.4 Signal Description

Not applicable.

## 19.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

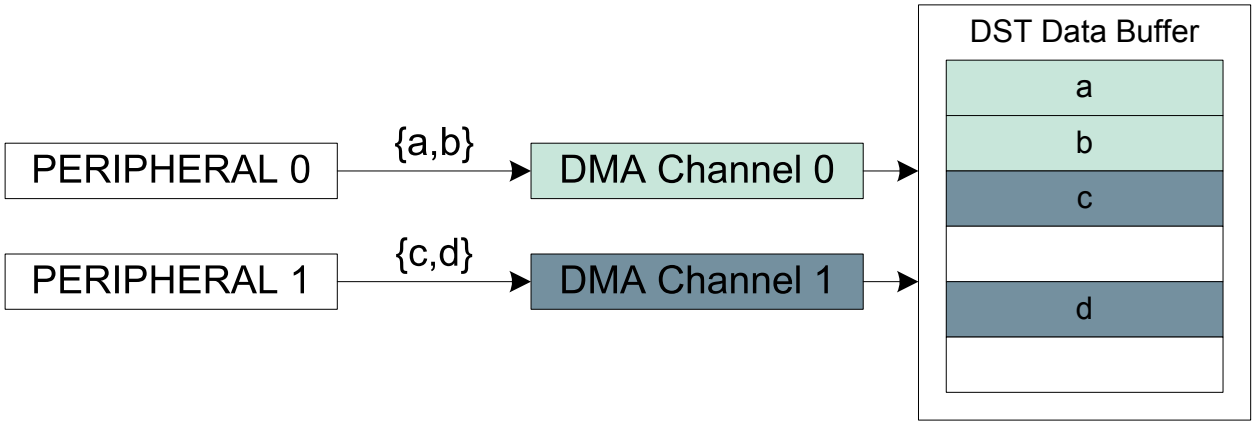
### 19.5.1 I/O Lines

Not applicable.

- BEATSIZE is the configured number of bytes in a beat
- STEPSIZE is the configured number of beats for each incrementation

Figure 20-9shows an example where DMA channel 0 is configured to increment destination address by one beat (BTCTRL.DSTINC=1) and DMA channel 1 is configured to increment destination address by two beats (BTCTRL.DSTINC=1, BTCTRL.STEPSEL=0, and BTCTRL.STEPSIZE=0x1). As the source address for both channels are peripherals, source incrementation is disabled (BTCTRL.SRCINC=0).

**Figure 20-9. Destination Address Increment**




#### 20.6.2.8 Error Handling

If a bus error is received from an AHB slave during a DMA data transfer, the corresponding active channel is disabled and the corresponding Channel Transfer Error Interrupt flag in the Channel Interrupt Status and Clear register (CHINTFLAG.TERR) is set. If enabled, the optional transfer error interrupt is generated. The transfer counter will not be decremented and its current value is written-back in the write-back memory section before the channel is disabled.

When the DMAC fetches an invalid descriptor (BTCTRL.VALID=0) or when the channel is resumed and the DMA fetches the next descriptor with null address (DESCADDR=0x00000000), the corresponding channel operation is suspended, the Channel Suspend Interrupt Flag in the Channel Interrupt Flag Status and Clear register (CHINTFLAG.SUSP) is set, and the Channel Fetch Error bit in the Channel Status register (CHSTATUS.FERR) is set. If enabled, the optional suspend interrupt is generated.

### 20.6.3 Additional Features

#### 20.6.3.1 Linked Descriptors

A transaction can consist of either a single block transfer or of several block transfers. When a transaction consist of several block transfers it is called linked descriptors.

Figure Figure 20-3 illustrates how linked descriptors work. When the first block transfer is completed on DMA channel 0, the DMAC fetches the next transfer descriptor which is pointed to by the value stored in the Next Descriptor Address (DESCADDR) register of the first transfer descriptor. Fetching the next transfer descriptor (DESCADDR) is continued until the last transfer descriptor. When the block transfer for the last transfer descriptor is executed and DESCADDR=0x00000000, the transaction is terminated. For further details on how the next descriptor is fetched from SRAM, refer to section Data Transmission.

**Adding Descriptor to the End of a List**

To add a new descriptor at the end of the descriptor list, create the descriptor in SRAM, with DESCADDR=0x00000000 indicating that it is the new last descriptor in the list, and modify the DESCADDR value of the current last descriptor to the address of the newly created descriptor.

**Modifying a Descriptor in a List**

In order to add descriptors to a linked list, the following actions must be performed:

## 20.7 Register Summary

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRL | 7:0 | | | | | | CRCENABLE | DMAENABLE | SWRST |
| 0x01 | | 15:8 | | | | | LVLEN3 | LVLEN2 | LVLEN1 | LVLEN0 |
| 0x02 | CRCCTRL | 7:0 | | | | | CRCPOLY[1:0] | | CRCBEATSIZE[1:0] | |
| 0x03 | | 15:8 | | | CRCSRC[5:0] | | | | | |
| 0x04 | CRCDATAIN | 7:0 | CRCDATAIN[7:0] | | | | | | | |
| 0x05 | | 15:8 | CRCDATAIN[15:8] | | | | | | | |
| 0x06 | | 23:16 | CRCDATAIN[23:16] | | | | | | | |
| 0x07 | | 31:24 | CRCDATAIN[31:24] | | | | | | | |
| 0x08 | CRCCHKSUM | 7:0 | CRCCHKSUM[7:0] | | | | | | | |
| 0x09 | | 15:8 | CRCCHKSUM[15:8] | | | | | | | |
| 0x0A | | 23:16 | CRCCHKSUM[23:16] | | | | | | | |
| 0x0B | | 31:24 | CRCCHKSUM[31:24] | | | | | | | |
| 0x0C | CRCSTATUS | 7:0 | | | | | | | CRCZERO | CRCBUSY |
| 0x0D | DBGCTRL | 7:0 | | | | | | | | DBGRUN |
| 0x0E | QOSCTRL | 7:0 | | | DQOS[1:0] | | FQOS[1:0] | | WRBQOS[1:0] | |
| 0x0F | Reserved | | | | | | | | | |
| 0x10 | SWTRIGCTRL | 7:0 | SWTRIG7 | SWTRIG6 | SWTRIG5 | SWTRIG4 | SWTRIG3 | SWTRIG2 | SWTRIG1 | SWTRIG0 |
| 0x11 | | 15:8 | | | | | SWTRIG11 | SWTRIG10 | SWTRIG9 | SWTRIG8 |
| 0x12 | | 23:16 | | | | | | | | |
| 0x13 | | 31:24 | | | | | | | | |
| 0x14 | PRICTRL0 | 7:0 | RRLVLEN0 | | | | LVLPRI0[3:0] | | | |
| 0x15 | | 15:8 | RRLVLEN1 | | | | LVLPRI1[3:0] | | | |
| 0x16 | | 23:16 | RRLVLEN2 | | | | LVLPRI2[3:0] | | | |
| 0x17 | | 31:24 | RRLVLEN3 | | | | LVLPRI3[3:0] | | | |
| 0x18 ... 0x1F | Reserved | | | | | | | | | |
| 0x20 | INTPEND | 7:0 | | | | | ID[3:0] | | | |
| 0x21 | | 15:8 | PEND | BUSY | FERR | | | SUSP | TCMPL | TERR |
| 0x22 ... 0x23 | Reserved | | | | | | | | | |
| 0x24 | INTSTATUS | 7:0 | CHINT7 | CHINT6 | CHINT5 | CHINT4 | CHINT3 | CHINT2 | CHINT1 | CHINT0 |
| 0x25 | | 15:8 | | | | | CHINT11 | CHINT10 | CHINT9 | CHINT8 |
| 0x26 | | 23:16 | | | | | | | | |
| 0x27 | | 31:24 | | | | | | | | |
| 0x28 | BUSYCH | 7:0 | BUSYCH7 | BUSYCH6 | BUSYCH5 | BUSYCH4 | BUSYCH3 | BUSYCH2 | BUSYCH1 | BUSYCH0 |
| 0x29 | | 15:8 | | | | | BUSYCH11 | BUSYCH10 | BUSYCH9 | BUSYCH8 |
| 0x2A | | 23:16 | | | | | | | | |
| 0x2B | | 31:24 | | | | | | | | |
| 0x2C | PENDCH | 7:0 | PENDCH7 | PENDCH6 | PENDCH5 | PENDCH4 | PENDCH3 | PENDCH2 | PENDCH1 | PENDCH0 |
| 0x2D | | 15:8 | | | | | PENDCH11 | PENDCH10 | PENDCH9 | PENDCH8 |
| 0x2E | | 23:16 | | | | | | | | |
| 0x2F | | 31:24 | | | | | | | | |

| Value | Description |
|---|---|
| 0 | The external interrupt x is disabled. |
| 1 | The external interrupt x is enabled. |

### 21.8.8 Interrupt Flag Status and Clear

**Name:** INTFLAG
**Offset:** 0x10
**Reset:** 0x00000000
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | EXTINT17 | EXTINT16 |
| Access | | | | | | | R/W | R/W |
| Reset | | | | | | | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | EXTINT15 | EXTINT14 | EXTINT13 | EXTINT12 | EXTINT11 | EXTINT10 | EXTINT9 | EXTINT8 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | EXTINT7 | EXTINT6 | EXTINT5 | EXTINT4 | EXTINT3 | EXTINT2 | EXTINT1 | EXTINT0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – EXTINTx : External Interrupt x [x=17..0]**
This flag is cleared by writing a one to it.

This flag is set when EXTINTx pin matches the external interrupt sense configuration and will generate an interrupt request if INTENCLR/SET.EXTINT[x] is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the External Interrupt x flag.

### 21.8.9 Wake-Up Enable

**Name:** WAKEUP
**Offset:** 0x14
**Reset:** 0x00000000
**Property:** Write-Protected

**IDLE** No frame is transferred on the communication line. Signal is always high in this state.

### 26.6.2 Basic Operation

#### 26.6.2.1 Initialization

The following registers are enable-protected, meaning they can only be written when the USART is disabled (CTRL.ENABLE=0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits.
- Control B register (CTRLB), except the Receiver Enable (RXEN) and Transmitter Enable (TXEN) bits.
- Baud register (BAUD)

When the USART is enabled or is being enabled (CTRLA.ENABLE=1), any writing attempt to these registers will be discarded. If the peripheral is being disabled, writing to these registers will be executed after disabling is completed. Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the USART is enabled, it must be configured by these steps:

1. Select either external (0x0) or internal clock (0x1) by writing the Operating Mode value in the CTRLA register (CTRLA.MODE).
2. Select either asynchronous (0) or or synchronous (1) communication mode by writing the Communication Mode bit in the CTRLA register (CTRLA.CMODE).
3. Select pin for receive data by writing the Receive Data Pinout value in the CTRLA register (CTRLA.RXPO).
4. Select pads for the transmitter and external clock by writing the Transmit Data Pinout bit in the CTRLA register (CTRLA.TXPO).
5. Configure the Character Size field in the CTRLB register (CTRLB.CHSIZE) for character size.
6. Set the Data Order bit in the CTRLA register (CTRLA.DORD) to determine MSB- or LSB-first data transmission.
7. To use parity mode:
    7.1. Enable parity mode by writing 0x1 to the Frame Format field in the CTRLA register (CTRLA.FORM).
    7.2. Configure the Parity Mode bit in the CTRLB register (CTRLB.PMODE) for even or odd parity.
8. Configure the number of stop bits in the Stop Bit Mode bit in the CTRLB register (CTRLB.SBMODE).
9. When using an internal clock, write the Baud register (BAUD) to generate the desired baud rate.
10. Enable the transmitter and receiver by writing '1' to the Receiver Enable and Transmitter Enable bits in the CTRLB register (CTRLB.RXEN and CTRLB.TXEN).

#### 26.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Writing ‘1’ to the Software Reset bit in the Control A register (CTRLA.SWRST) will reset all registers of this peripheral to their initial states, except the DBGCTRL register, and the peripheral is disabled.

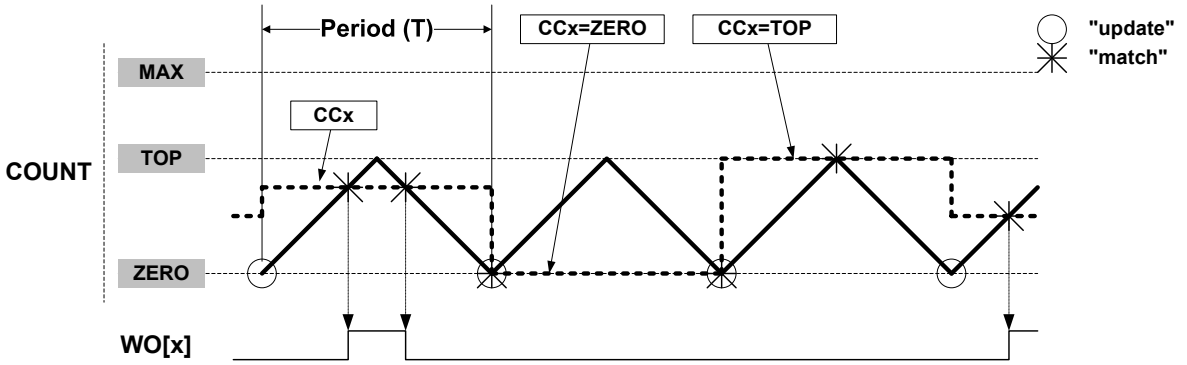
Refer to the CTRLA register description for details.

## 29.8 Register Summary

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | CTRLA | 7:0 | | | SEREN1 | SEREN0 | CKEN1 | CKEN0 | ENABLE | SWRST |
| 0x01<br>...<br>0x03 | Reserved | | | | | | | | | |
| 0x04 | CLKCTRLn0 | 7:0 | BITDELAY | FSWIDTH[1:0] | | NBSLOTS[2:0] | | | SLOTSIZE[1:0] | |
| 0x05 | | 15:8 | | | | SCKSEL | FSINV | | | FSSEL |
| 0x06 | | 23:16 | MCKDIV[4:0] | | | | | MCKEN | | MCKSEL |
| 0x07 | | 31:24 | MCKOUTINV | SCKOUTINV | FSOUTINV | MCKOUTDIV[4:0] | | | | |
| 0x08 | CLKCTRLn1 | 7:0 | BITDELAY | FSWIDTH[1:0] | | NBSLOTS[2:0] | | | SLOTSIZE[1:0] | |
| 0x09 | | 15:8 | | | | SCKSEL | FSINV | | | FSSEL |
| 0x0A | | 23:16 | MCKDIV[4:0] | | | | | MCKEN | | MCKSEL |
| 0x0B | | 31:24 | MCKOUTINV | SCKOUTINV | FSOUTINV | MCKOUTDIV[4:0] | | | | |
| 0x0C | INTENCLR | 7:0 | | | RXOR1 | RXOR0 | | | RXRDY1 | RXRDY0 |
| 0x0D | | 15:8 | | | TXUR1 | TXUR0 | | | TXRDY1 | TXRDY0 |
| 0x0E<br>...<br>0x0F | Reserved | | | | | | | | | |
| 0x10 | INTENSET | 7:0 | | | RXOR1 | RXOR0 | | | RXRDY1 | RXRDY0 |
| 0x11 | | 15:8 | | | TXUR1 | TXUR0 | | | TXRDY1 | TXRDY0 |
| 0x12<br>...<br>0x13 | Reserved | | | | | | | | | |
| 0x14 | INTFLAG | 7:0 | | | RXOR1 | RXOR0 | | | RXRDY1 | RXRDY0 |
| 0x15 | | 15:8 | | | TXUR1 | TXUR0 | | | TXRDY1 | TXRDY0 |
| 0x16<br>...<br>0x17 | Reserved | | | | | | | | | |
| 0x18 | SYNCBUSY | 7:0 | | | SEREN1 | SEREN0 | CKEN1 | CKEN0 | ENABLE | SWRST |
| 0x19 | | 15:8 | | | | | | | DATA1 | DATA0 |
| 0x1A<br>...<br>0x1F | Reserved | | | | | | | | | |
| 0x20 | SERCTRLn0 | 7:0 | SLOTADJ | | CLKSEL | TXSAME | TXDEFAULT[1:0] | | SERMODE[1:0] | |
| 0x21 | | 15:8 | BITREV | EXTEND[1:0] | | WORDADJ | | DATASIZE[2:0] | | |
| 0x22 | | 23:16 | SLOTDIS8 | SLOTDIS7 | SLOTDIS6 | SLOTDIS5 | SLOTDIS4 | SLOTDIS3 | SLOTDIS1 | SLOTDIS0 |
| 0x23 | | 31:24 | | | | | | RXLOOP | DMA | MONO |
| 0x24 | SERCTRLn1 | 7:0 | SLOTADJ | | CLKSEL | TXSAME | TXDEFAULT[1:0] | | SERMODE[1:0] | |
| 0x25 | | 15:8 | BITREV | EXTEND[1:0] | | WORDADJ | | DATASIZE[2:0] | | |
| 0x26 | | 23:16 | SLOTDIS8 | SLOTDIS7 | SLOTDIS6 | SLOTDIS5 | SLOTDIS4 | SLOTDIS3 | SLOTDIS1 | SLOTDIS0 |
| 0x27 | | 31:24 | | | | | | RXLOOP | DMA | MONO |
| 0x28<br>...<br>0x2F | Reserved | | | | | | | | | |

In DSBOTH operation, a second update time occurs on TOP when circular buffer is enabled.

**Figure 31-7. Dual-Slope Pulse Width Modulation**




Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM ($R_{PWM\_DS}$):

$$R_{PWM\_DS} = \frac{\log(PER+1)}{\log(2)}.$$

The PWM frequency $f_{PWM\_DS}$ depends on the period setting (TOP) and the peripheral clock frequency $f_{GCLK\_TCC}$, and can be calculated by the following equation:

$$f_{PWM\_DS} = \frac{f_{GCLK\_TCC}}{2N \cdot PER}$$

*N* represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency ($f_{GCLK\_TCC}$) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width ($P_{PWM\_DS}$) depends on the compare channel (CCx) register value and the peripheral clock frequency ($f_{GCLK\_TCC}$), and can be calculated by the following equation:

$$P_{PWM\_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK\_TCC}}$$

*N* represents the prescaler divider used.

**Note:** In DSTOP, DSBOTTOM and DSBOTH operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB]=0, falling if CCx[MSB]=1.)

**Related Links**

Circular Buffer

#### Dual-Slope Critical PWM Generation

### Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC_NUM/2) control the generated waveform output edge during down-counting.

- Decrement the counter on event
- Period and pulse width capture
- Non-recoverable fault

The TCC can take the following actions on counter Event 0 (TCCx EV0):

- Counter re-trigger
- Count on event (increment or decrement, depending on counter direction)
- Counter start - start counting on the event rising edge. Further events will not restart the counter; the counter will keep on counting using prescaled GCLK_TCCx, until it reaches TOP or ZERO, depending on the direction.
- Counter increment on event. This will increment the counter, irrespective of the counter direction.
- Count during active state of an asynchronous event (increment or decrement, depending on counter direction). In this case, the counter will be incremented or decremented on each cycle of the prescaled clock, as long as the event is active.
- Non-recoverable fault

The counter Event Actions are available in the Event Control registers (EVCTRL.EVACT0 and EVCTRL.EVACT1). For further details, refer to EVCTRL.

Writing a '1' ('0') to an Event Input bit in the Event Control register (EVCTRL.MCEIx or EVCTRL.TCEIx) enables (disables) the corresponding action on input event.

**Note:** When several events are connected to the TCC, the enabled action will apply for each of the incoming events. Refer to *EVSYS – Event System* for details on how to configure the event system.

**Related Links**

EVSYS – Event System

### 31.6.5 Sleep Mode Operation

The TCC can be configured to operate in any sleep mode. To be able to run in standby the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. The MODULE can in any sleep mode wake up the device using interrupts or perform actions through the Event System.

### 31.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Pattern and Pattern Buffer registers (PATT and PATTB)
- Waveform register (WAVE)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERB)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBx)

The following registers are synchronized when read:

**Offset:** 0x40
**Reset:** 0xFFFFFFFF
**Property:** Write-Synchronized

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | PER[17:10] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | PER[9:2] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | PER[1:0] | | DITHER[5:0] | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 23:6 – PER[17:0]: Period Value**
These bits hold the value of the period buffer register.

**Note:** When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

**Note:** This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

| CTRLA.RESOLUTION | Bits [23:m] |
|---|---|
| 0x0 - NONE | 23:0 |
| 0x1 - DITH4 | 23:4 |
| 0x2 - DITH5 | 23:5 |
| 0x3 - DITH6 | 23:6 (depicted) |

**Bits 5:0 – DITHER[5:0]: Dithering Cycle Number**
These bits hold the number of extra cycles that are added on the PWM pulse period every 64 PWM frames.
**Note:** This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

| CTRLA.RESOLUTION | Bits [n:0] |
|---|---|
| 0x0 - NONE | - |
| 0x1 - DITH4 | 3:0 |

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B | Reserved | | | | | | | | | |
| 0x1C | INTFLAG | 7:0 | RAMACER | UPRSM | DNRSM | WAKEUP | RST | HSOF | | |
| 0x1D | | 15:8 | | | | | | | DDISC | DCONN |
| 0x1E | Reserved | | | | | | | | | |
| 0x1F | Reserved | | | | | | | | | |
| 0x20 | PINTSMRY | 7:0 | PINT[7:0] | | | | | | | |
| 0x21 | | 15:8 | PINT[15:8] | | | | | | | |
| 0x22 | Reserved | | | | | | | | | |
| 0x23 | | | | | | | | | | |

**Table 32-6. Host Pipe Register n**

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1m0 | PCFGn | 7:0 | | | PTYPE[2:0] | | | BK | PTOKEN[1:0] | |
| 0x1m1 | Reserved | | | | | | | | | |
| 0x1m2 | Reserved | | | | | | | | | |
| 0x1m3 | BINTERVAL | 7:0 | BINTERVAL[7:0] | | | | | | | |
| 0x1m4 | PSTATUSCLRn | 7:0 | BK1RDY | BK0RDY | | PFREEZE | | CURBK | | DTGL |
| 0x1m5 | PSTATUSETn | 7:0 | BK1RDY | BK0RDY | | PFREEZE | | CURBK | | DTGL |
| 0x1m6 | PSTATUSn | 7:0 | BK1RDY | BK0RDY | | PFREEZE | | CURBK | | DTGL |
| 0x1m7 | PINTFLAGn | 7:0 | | | STALL | TXSTP | PERR | TRFAIL | TRCPT1 | TRCPT0 |
| 0x1m8 | PINTENCLRn | 7:0 | | | STALL | TXSTP | PERR | TRFAIL | TRCPT1 | TRCPT0 |
| 0x1m9 | PINTENSETn | 7:0 | | | STALL | TXSTP | PERR | TRFAIL | TRCPT1 | TRCPT0 |
| 0x1mA | Reserved | | | | | | | | | |
| 0x1mB | Reserved | | | | | | | | | |

**Table 32-7. Host Pipe n Descriptor Bank 0**

| Offset 0x n0 + index | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | ADDR | 7:0 | ADD[7:0] | | | | | | | |
| 0x01 | | 15:8 | ADD[15:8] | | | | | | | |
| 0x02 | | 23:16 | ADD[23:16] | | | | | | | |
| 0x03 | | 31:24 | ADD[31:24] | | | | | | | |
| 0x04 | PCKSIZE | 7:0 | BYTE_COUNT[7:0] | | | | | | | |
| 0x05 | | 15:8 | MULTI_PACKET_SIZE[1:0] | | BYTE_COUNT[13:8] | | | | | |
| 0x06 | | 23:16 | MULTI_PACKET_SIZE[9:2] | | | | | | | |
| 0x07 | | 31:24 | AUTO_ZLP | SIZE[2:0] | | | MULTI_PACKET_SIZE[13:10] | | | |
| 0x08 | EXTREG | 7:0 | VARIABLE[3:0] | | | | SUBPID[3:0] | | | |
| 0x09 | | 15:8 | | VARIABLE[10:4] | | | | | | |
| 0x0A | STATUS_BK | 7:0 | | | | | | | ERRORFLOW | CRCERR |
| 0x0B | | 15:8 | | | | | | | | |
| 0x0C | CTRL_PIPE | 7:0 | | PDADDR[6:0] | | | | | | |
| 0x0D | | 15:8 | PEPMAX[3:0] | | | | PEPNUM[3:0] | | | |
| 0x0E | STATUS_PIPE | 7:0 | ERCNT[2:0] | | | CRC16ER | TOUTER | PIDER | DAPIDER | DTGLER |
| 0x0F | | 15:8 | | | | | | | | |

| GAIN[3:0] | Name | Description |
|---|---|---|
| 0x5-0xE | | Reserved |
| 0xF | DIV2 | 1/2x |

**Bits 23:20 – INPUTOFFSET[3:0]: Positive Mux Setting Offset**
The pin scan is enabled when INPUTSCAN != 0. Writing these bits to a value other than zero causes the first conversion triggered to be converted using a positive input equal to MUXPOS + INPUTOFFSET. Setting this register to zero causes the first conversion to use a positive input equal to MUXPOS.

After a conversion, the INPUTOFFSET register will be incremented by one, causing the next conversion to be done with the positive input equal to MUXPOS + INPUTOFFSET. The sum of MUXPOS and INPUTOFFSET gives the input that is actually converted.

**Bits 19:16 – INPUTSCAN[3:0]: Number of Input Channels Included in Scan**
This register gives the number of input sources included in the pin scan. The number of input sources included is INPUTSCAN + 1. The input channels included are in the range from MUXPOS + INPUTOFFSET to MUXPOS + INPUTOFFSET + INPUTSCAN.

The range of the scan mode must not exceed the number of input channels available on the device.

**Bits 12:8 – MUXNEG[4:0]: Negative Mux Input Selection**
These bits define the Mux selection for the negative ADC input. selections.

| Value | Name | Description |
|---|---|---|
| 0x00 | PIN0 | ADC AIN0 pin |
| 0x01 | PIN1 | ADC AIN1 pin |
| 0x02 | PIN2 | ADC AIN2 pin |
| 0x03 | PIN3 | ADC AIN3 pin |
| 0x04 | PIN4 | ADC AIN4 pin |
| 0x05 | PIN5 | ADC AIN5 pin |
| 0x06 | PIN6 | ADC AIN6 pin |
| 0x07 | PIN7 | ADC AIN7 pin |
| 0x08-0x17 | Reserved | |
| 0x18 | GND | Internal ground |
| 0x19 | IOGND | I/O ground |
| 0x1A-0x1F | Reserved<br>Note: 1. Only available in SAM R21G. | |

**Bits 4:0 – MUXPOS[4:0]: Positive Mux Input Selection**
These bits define the Mux selection for the positive ADC input. The following table shows the possible input selections. If the internal bandgap voltage or temperature sensor input channel is selected, then the Sampling Time Length bit group in the SamplingControl register must be written.

| MUXPOS[4:0] | Group configuration | Description |
|---|---|---|
| 0x00 | PIN0 | ADC AIN0 pin |
| 0x01 | PIN1 | ADC AIN1 pin |
| 0x02 | PIN2 | ADC AIN2 pin |

# 34. AC – Analog Comparators

## 34.1 Overview

The Analog Comparator (AC) supports two individual comparators. Each comparator (COMP) compares the voltage levels on two inputs, and provides a digital output based on this comparison. Each comparator may be configured to generate interrupt requests and/or peripheral events upon several different combinations of input change.

Hysteresis and propagation delay are two important properties of the comparators' dynamic behavior. Both parameters may be adjusted to achieve the optimal operation for each application.

The input selection includes four shared analog port pins and several internal signals. Each comparator output state can also be output on a pin for use by external devices.

The comparators are always grouped in pairs on each port. The AC peripheral implements one pair of comparators. These are called Comparator 0 (COMP0) and Comparator 1 (COMP1) They have identical behaviors, but separate control registers. The pair can be set in window mode to compare a signal to a voltage range instead of a single voltage level.

## 34.2 Features

- Two individual comparators
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - 4-levels or Off
- Analog comparator outputs available on pins
  - Asynchronous or synchronous
- Flexible input selection:
  - Four pins selectable for positive or negative inputs
  - Ground (for zero crossing)
  - Bandgap reference voltage
  - 64-level programmable VDD scaler per comparator
  - DAC
- Interrupt generation on:
  - Rising or falling edge
  - Toggle
  - End of comparison
- Window function interrupt generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
  - Signal outside window
- Event generation on:
  - Comparator output
  - Window function inside/outside window

**Table 44-15. Differential Mode (Device Variant A)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ENOB | Effective Number Of Bits | With gain compensation | - | 10.5 | 10.9 | bits |
| TUE | Total Unadjusted Error | 1x Gainn | 1.5 | 4.3 | 17.0 | LSB |
| INLI | Integral Non Linearity | 1x Gainn | 1.0 | 1.3 | 6.5 | LSB |
| DNL | Differential Non Linearity | 1x Gainn | +/-0.3 | +/-0.5 | +/-0.95 | LSB |
| | Gain Error | Ext. Ref 1x | -15.0 | 2.5 | +20.0 | mV |
| | | $V_{REF}=V_{DDANA}/1.48$ | -20.0 | -1.5 | +20.0 | mV |
| | | Bandgap | -15.0 | -5.0 | +15.0 | mV |
| | Gain Accuracy(5) | Ext. Ref. 0.5x | +/-0.1 | +/-0.2 | +/-0.45 | % |
| | | Ext. Ref. 2x to 16x | +/-0.1 | +/-0.2 | +/-2.0 | % |
| | Offset Error | Ext. Ref. 1x | -10.0 | -1.5 | +10.0 | mV |
| | | $V_{REF}=V_{DDANA}/1.48$ | -10.0 | 0.5 | +15.0 | mV |
| | | Bandgap | -10.0 | 3.0 | +15.0 | mV |
| SFDR | Spurious Free Dynamic Range | 1x Gain<br>$F_{CLK\_ADC}$ = 2.1MHz<br>$F_{IN}$ = 40kHz<br>$A_{IN}$ = 95%FSR | 64.2 | 70.0 | 78.9 | dB |
| SINAD | Signal-to-Noise and Distortion | | 64.1 | 65.0 | 66 | dB |
| SNR | Signal-to-Noise Ratio | | 64.3 | 65.5 | 66.0 | dB |
| THD | Total Harmonic Distortion | | -74.8 | -64.0 | -65.0 | dB |
| | Noise RMS | T=25°C | 0.6 | 1.0 | 1.6 | mV |

**Table 44-16. Differential Mode (Device Variant B)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ENOB | Effective Number Of Bits | With gain compensation | - | 10.5 | 10.8 | bits |
| TUE | Total Unadjusted Error | 1x Gainn | 1.5 | 2.7 | 14 | LSB |
| INLI | Integral Non Linearity | 1x Gainn | 0.9 | 1.3 | 4 | LSB |
| DNL | Differential Non Linearity | 1x Gainn | +/-0.3 | +/-0.5 | +/-0.95 | LSB |
| | Gain Error | Ext. Ref 1x | -10.0 | -1.3 | +10 | mV |
| | | $V_{REF}=V_{DDANA}/1.48$ | -25.0 | -10.1 | +10.0 | mV |
| | | Bandgap | -25.0 | +2 | +10.0 | mV |
| | Gain Accuracy(5) | Ext. Ref. 0.5x | +/-0.005 | +/-0.05 | +/-0.15 | % |
| | | Ext. Ref. 2x to 16x | +/-0.1 | +/-0.03 | +/-0.5 | % |
| | Offset Error | Ext. Ref. 1x | -8.0 | -1.0 | +8.0 | mV |
| | | $V_{REF}=V_{DDANA}/1.48$ | -8.0 | 0.6 | +8.0 | mV |
| | | Bandgap | -6.0 | -1.0 | +8.0 | mV |

## Quality Management System Certified by DNV

**ISO/TS 16949**

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.