Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g18a-aft

Bit 5 – USB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – DMAC:
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

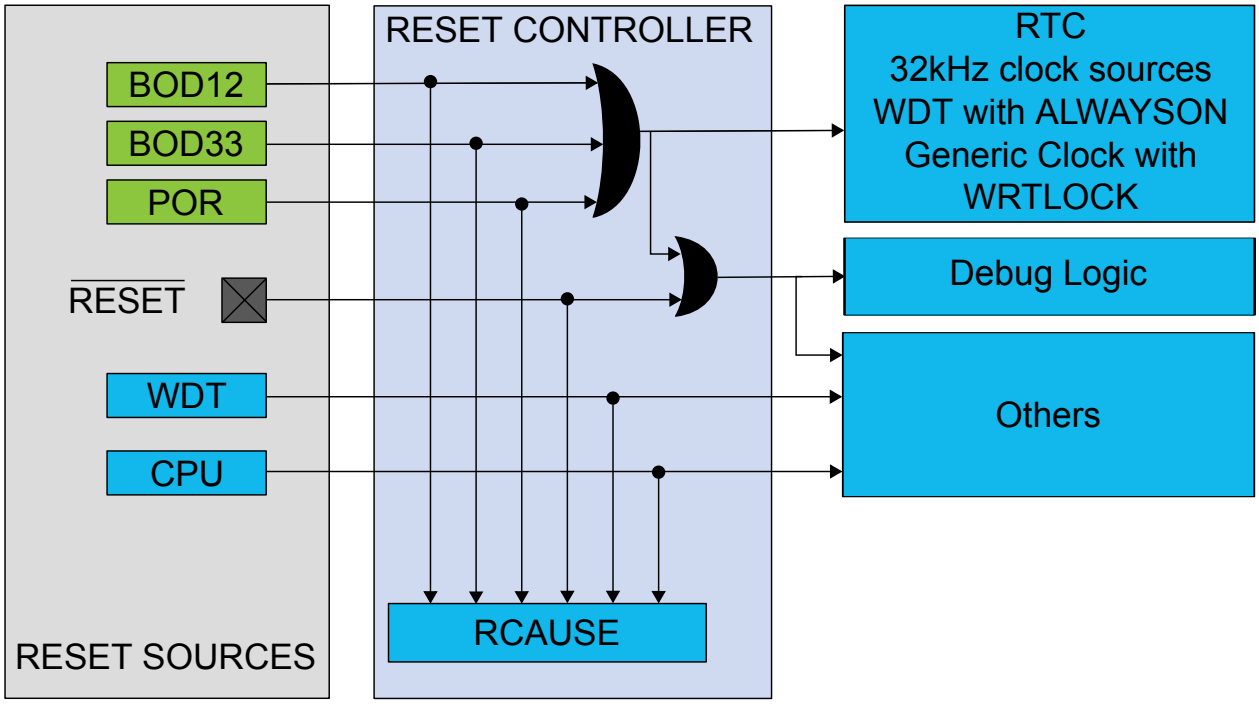
Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –

Figure 16-3. Reset Controller



16.6.2.8 Sleep Mode Controller

Sleep mode is activated by the Wait For Interrupt instruction (WFI). The Idle bits in the Sleep Mode register (SLEEP.IDLE) and the SLEEPDEEP bit of the System Control register of the CPU should be used as argument to select the level of the sleep mode.

There are two main types of sleep mode:

- IDLE mode: The CPU is stopped. Optionally, some synchronous clock domains are stopped, depending on the IDLE argument. Regulator operates in normal mode.
- STANDBY mode: All clock sources are stopped, except those where the RUNSTDBY bit is set. Regulator operates in low-power mode. Before entering standby mode the user must make sure that a significant amount of clocks and peripherals are disabled, so that the voltage regulator is not overloaded.

Table 16-3. Sleep Mode Entry and Exit Table

Mode	Level	Mode Entry	Wake-Up Sources
IDLE	0	SCR.SLEEPDEEP = 0 SLEEP.IDLE=Level WFI	Synchronous(2) (APB, AHB), asynchronous(1)
	1		Synchronous (APB), asynchronous
	2		Asynchronous
STANDBY		SCR.SLEEPDEEP = 1 WFI	Asynchronous

Note:

1. Asynchronous: interrupt generated on generic clock or external clock or external event.
2. Synchronous: interrupt generated on the APB clock.

In this device, SleepWalking is supported only on GCLK clocks by using the on-demand clock principle of the clock sources. Refer to *On-demand, Clock Requests* for more details.

Related Links

On-demand, Clock Requests

16.6.4 DMA Operation

Not applicable.

16.6.5 Interrupts

The peripheral has the following interrupt sources:

- Clock Ready flag

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled or the peripheral is reset. An interrupt flag is cleared by writing a one to the corresponding bit in the INTFLAG register. Each peripheral can have one interrupt request line per interrupt source or one common interrupt request line for all the interrupt sources. Refer to *Nested Vector Interrupt Controller* for details. If the peripheral has one common interrupt request line for all the interrupt sources, the user must read the INTFLAG register to determine which interrupt condition is present.

Related Links

Nested Vector Interrupt Controller

16.6.6 Events

Not applicable.

16.6.7 Sleep Mode Operation

In all IDLE sleep modes, the power manager is still running on the selected main clock.

In STANDDBY sleep mode, the power manager is frozen and is able to go back to ACTIVE mode upon any asynchronous interrupt.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the Overflow interrupt flag.

Bit 6 – SYNCRDY: Synchronization Ready
This flag is cleared by writing a one to the flag.

This flag is set on a 1-to-0 transition of the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY), except when caused by enable or software reset, and an interrupt request will be generated if INTENCLR/SET.SYNCRDY is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the Synchronization Ready interrupt flag.

Bit 0 – CMP0: Compare 0
This flag is cleared by writing a one to the flag.

This flag is set on the next CLK_RTC_CNT cycle after a match with the compare condition, and an interrupt request will be generated if INTENCLR/SET.CMP0 is one.

Writing a zero to this bit has no effect.

Writing a one to this bit clears the Compare 0 interrupt flag.

19.8.15 Interrupt Flag Status and Clear - MODE1

Name: INTFLAG
Offset: 0x08
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	OVF	SYNCRDY					CMP1	CMP0
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit 7 – OVF: Overflow
This flag is cleared by writing a one to the flag.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is one.

Writing a zero to this bit has no effect.

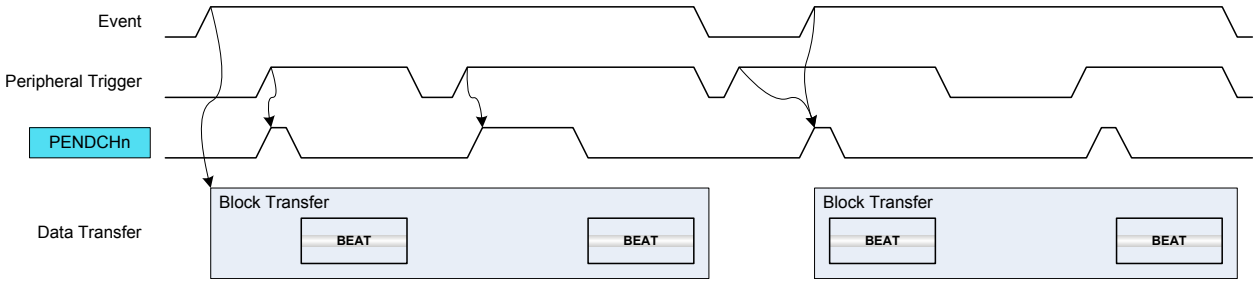
Writing a one to this bit clears the Overflow interrupt flag.

Bit 6 – SYNCRDY: Synchronization Ready
This flag is cleared by writing a one to the flag.

This flag is set on a 1-to-0 transition of the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY), except when caused by enable or software reset, and an interrupt request will be generated if INTENCLR/SET.SYNCRDY is one.

  - Enable 12 independent transfers
  - Automatic descriptor fetch for each channel
  - Suspend/resume operation support for each channel
- Flexible arbitration scheme
  - 4 configurable priority levels for each channel
  - Fixed or round-robin priority scheme within each priority level
- From 1 to 256KB data transfer in a single block transfer
- Multiple addressing modes
  - Static
  - Configurable increment scheme
- Optional interrupt generation
  - On block transfer complete
  - On error detection
  - On channel suspend
- 4 event inputs
  - One event input for each of the 4 least significant DMA channels
  - Can be selected to trigger normal transfers, periodic transfers or conditional transfers
  - Can be selected to suspend or resume channel operation
- 4 event outputs
  - One output event for each of the 4 least significant DMA channels
  - Selectable generation on AHB, block, or transaction transfer complete
- Error management supported by write-back function
  - Dedicated Write-Back memory section for each channel to store ongoing descriptor transfer
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE® 802.3)

Figure 20-14. Conditional Block Transfer with Beat Peripheral Triggers



Channel Suspend

The event input is used to suspend an ongoing channel operation. The event is acknowledged when the current AHB access is completed. For further details on Channel Suspend, refer to Channel Suspend.

Channel Resume

The event input is used to resume a suspended channel operation. The event is acknowledged as soon as the event is received and the Channel Suspend Interrupt Flag (CHINTFLAG.SUSP) is cleared. For further details refer to Channel Suspend.

Skip Next Block Suspend

This event can be used to skip the next block suspend action. If the channel is suspended before the event rises, the channel operation is resumed and the event is acknowledged. If the event rises before a suspend block action is detected, the event is kept until the next block suspend detection. When the block transfer is completed, the channel continues the operation (not suspended) and the event is acknowledged.

Related Links

USER

20.6.3.5 Event Output Selection

Event output selection is available only for the least significant DMA channels. The pulse width of an event output from a channel is one AHB clock cycle.

The output of channel events is enabled by writing a '1' to the Channel Event Output Enable bit in the Control B register (CHCTRLB.EVOE). The event output cause is selected by writing to the Event Output Selection bits in the Block Transfer Control register (BTCTRL.EVOSEL). It is possible to generate events after each block transfer (BTCTRL.EVOSEL=0x1) or beat transfer (BTCTRL.EVOSEL=0x3). To enable an event being generated when a transaction is complete, the block event selection must be set in the last transfer descriptor only.

The figure Figure 20-15 shows an example where the event output generation is enabled in the first block transfer, and disabled in the second block.

Bit	7	6	5	4	3	2	1	0
	CRCCHKSUM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CRCCHKSUM[31:0]: CRC Checksum
These bits store the generated CRC result. When CRC-16 is enabled, the 16 msb will always read '0'.

These bits should only be read when CRC Module Busy bit in the CRC Status register CRCSTATUS.BUSY=0.

If CRC-16 is selected and CRCSTATUS.BUSY=0 (CRC generation is completed), this bit group will contain a valid checksum.

If CRC-32 is selected and CRCSTATUS.BUSY=0 (CRC generation is completed), this bit group will contain a valid *reversed* checksum, i.e.: bit 31 is swapped with bit 0, bit 30 with bit 1, etc.

20.8.5 CRC Status

Name: CRCSTATUS
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
							CRCZERO	CRCBUSY
Access							R	R/W
Reset							0	0

Bit 1 – CRCZERO: CRC Zero
This bit is cleared when a new CRC source is selected.

This bit is set when the CRC generation is complete and the CRC Checksum is zero.

When running CRC-32 and appending the checksum at the end of the packet (as little endian), the final checksum should be 0x2144df1c, and not zero. However, if the checksum is complemented before it is appended (as little endian) to the data, the final result in the checksum register will be zero. See the description of CRCCHKSUM to read out different versions of the checksum.

Bit 0 – CRCBUSY: CRC Module Busy
This flag is cleared by writing a one to it when used with I/O interface. When used with a DMA channel, the bit is set when the corresponding DMA channel is enabled, and cleared when the corresponding DMA channel is disabled. This register bit cannot be cleared by the application when the CRC is used with a DMA channel.

This bit is set when a source configuration is selected and as long as the source is using the CRC module.

20.8.6 Debug Control

Name: DBGCTRL
Offset: 0x0D
Reset: 0x00

CMD[1:0]	Name	Description
0x2	RESUME	Channel resume operation
0x3	-	Reserved

Bits 23:22 – TRIGACT[1:0]: Trigger Action
These bits define the trigger action used for a transfer.

TRIGACT[1:0]	Name	Description
0x0	BLOCK	One trigger required for each block transfer
0x1	-	Reserved
0x2	BEAT	One trigger required for each beat transfer
0x3	TRANSACTION	One trigger required for each transaction

Bits 13:8 – TRIGSRC[5:0]: Trigger Source
These bits define the peripheral trigger which is source of the transfer. For details on trigger selection and trigger modes, refer to Transfer Triggers and Actions and CHCTRLB.TRIGACT.

Value	Name	Description
0x00	DISABLE	Only software/event triggers
0x01	SERCOM0 RX	SERCOM0 RX Trigger
0x02	SERCOM0 TX	SERCOM0 TX Trigger
0x03	SERCOM1 RX	SERCOM1 RX Trigger
0x04	SERCOM1 TX	SERCOM1 TX Trigger
0x05	SERCOM2 RX	SERCOM2 RX Trigger
0x06	SERCOM2 TX	SERCOM2 TX Trigger
0x07	SERCOM3 RX	SERCOM3 RX Trigger
0x08	SERCOM3 TX	SERCOM3 TX Trigger
0x09	SERCOM4 RX	SERCOM4 RX Trigger
0x0A	SERCOM4 TX	SERCOM4 TX Trigger
0x0B	SERCOM5 RX	SERCOM5 RX Trigger
0x0C	SERCOM5 TX	SERCOM5 TX Trigger
0x0D	TCC0 OVF	TCC0 Overflow Trigger
0x0E	TCC0 MC0	TCC0 Match/Compare 0 Trigger
0x0F	TCC0 MC1	TCC0 Match/Compare 1 Trigger
0x10	TCC0 MC2	TCC0 Match/Compare 2 Trigger
0x11	TCC0 MC3	TCC0 Match/Compare 3 Trigger
0x12	TCC1 OVF	TCC1 Overflow Trigger
0x13	TCC1 MC0	TCC1 Match/Compare 0 Trigger
0x14	TCC1 MC1	TCC1 Match/Compare 1 Trigger
0x15	TCC2 OVF	TCC2 Overflow Trigger
0x16	TCC2 MC0	TCC2 Match/Compare 0 Trigger
0x17	TCC2 MC1	TCC2 Match/Compare 1 Trigger
0x18	TC0 OVF	TC0 Overflow Trigger
0x19	TC0 MC0	TC0 Match/Compare 0 Trigger
0x1A	TC0 MC1	TC0 Match/Compare 1 Trigger
0x1B	TC1 OVF	TC1 Overflow Trigger

22. NVMCTRL – Non-Volatile Memory Controller

22.1 Overview

Non-Volatile Memory (NVM) is a reprogrammable Flash memory that retains program and data storage even with power off. It embeds a main array and a separate smaller array intended for EEPROM emulation (RWWEE) that can be programmed while reading the main array. The NVM Controller (NVMCTRL) connects to the AHB and APB bus interfaces for system access to the NVM block. The AHB interface is used for reads and writes to the NVM block, while the APB interface is used for commands and configuration.

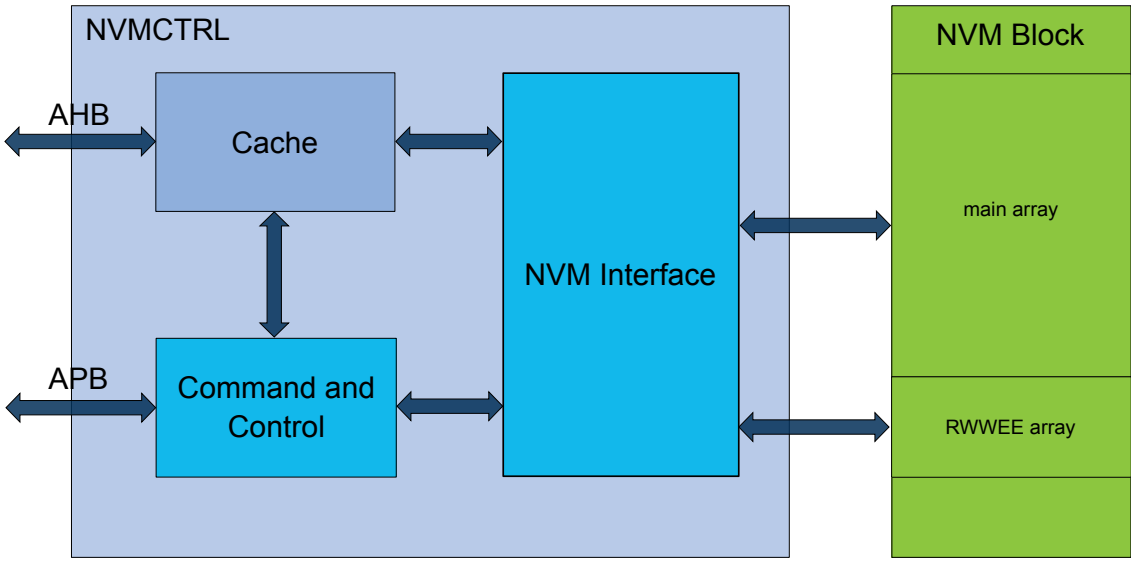
22.2 Features

- 32-bit AHB interface for reads and writes
- Read While Write EEPROM emulation area
- All NVM sections are memory mapped to the AHB, including calibration and system configuration
- 32-bit APB interface for commands and control
- Programmable wait states for read optimization
- 16 regions can be individually protected or unprotected
- Additional protection for boot loader
- Supports device protection through a security bit
- Interface to Power Manager for power-down of Flash blocks in sleep modes
- Can optionally wake up on exit from sleep or on first access
- Direct-mapped cache

Note: A register with property "Enable-Protected" may contain bits that are *not* enable-protected.

22.3 Block Diagram

Figure 22-1. Block Diagram



23.7 Register Summary

Offset	Name	Bit Pos.								
0x00	DIR	7:0	DIR[7:0]							
0x01		15:8	DIR[15:8]							
0x02		23:16	DIR[23:16]							
0x03		31:24	DIR[31:24]							
0x04	DIRCLR	7:0	DIRCLR[7:0]							
0x05		15:8	DIRCLR[15:8]							
0x06		23:16	DIRCLR[23:16]							
0x07		31:24	DIRCLR[31:24]							
0x08	DIRSET	7:0	DIRSET[7:0]							
0x09		15:8	DIRSET[15:8]							
0x0A		23:16	DIRSET[23:16]							
0x0B		31:24	DIRSET[31:24]							
0x0C	DIRTGL	7:0	DIRTGL[7:0]							
0x0D		15:8	DIRTGL[15:8]							
0x0E		23:16	DIRTGL[23:16]							
0x0F		31:24	DIRTGL[31:24]							
0x10	OUT	7:0	OUT[7:0]							
0x11		15:8	OUT[15:8]							
0x12		23:16	OUT[23:16]							
0x13		31:24	OUT[31:24]							
0x14	OUTCLR	7:0	OUTCLR[7:0]							
0x15		15:8	OUTCLR[15:8]							
0x16		23:16	OUTCLR[23:16]							
0x17		31:24	OUTCLR[31:24]							
0x18	OUTSET	7:0	OUTSET[7:0]							
0x19		15:8	OUTSET[15:8]							
0x1A		23:16	OUTSET[23:16]							
0x1B		31:24	OUTSET[31:24]							
0x1C	OUTTGL	7:0	OUTTGL[7:0]							
0x1D		15:8	OUTTGL[15:8]							
0x1E		23:16	OUTTGL[23:16]							
0x1F		31:24	OUTTGL[31:24]							
0x20	IN	7:0	IN[7:0]							
0x21		15:8	IN[15:8]							
0x22		23:16	IN[23:16]							
0x23		31:24	IN[31:24]							
0x24	CTRL	7:0	SAMPLING[7:0]							
0x25		15:8	SAMPLING[15:8]							
0x26		23:16	SAMPLING[23:16]							
0x27		31:24	SAMPLING[31:24]							
0x28	WRCONFIG	7:0	PINMASK[7:0]							
0x29		15:8	PINMASK[15:8]							
0x2A		23:16		DRVSTR				PULLEN	INEN	PMUXEN
0x2B		31:24	HWSEL	WRPINCFG		WRPMUX		PMUX[3:0]		

CPOL	TxD Change	RxD Sample
0x0	Rising XCK edge	Falling XCK edge
0x1	Falling XCK edge	Rising XCK edge

Bit 28 – CMODE: Communication Mode
This bit selects asynchronous or synchronous communication.

This bit is not synchronized.

Value	Description
0	Asynchronous communication.
1	Synchronous communication.

Bits 27:24 – FORM[3:0]: Frame Format
These bits define the frame format.

These bits are not synchronized.

FORM[3:0]	Description
0x0	USART frame
0x1	USART frame with parity
0x2-0x3	Reserved
0x4	Auto-baud - break detection and auto-baud.
0x5	Auto-baud - break detection and auto-baud with parity
0x6-0xF	Reserved

Bits 23:22 – SAMPA[1:0]: Sample Adjustment
These bits define the sample adjustment.

These bits are not synchronized.

SAMPA[1:0]	16x Over-sampling (CTRLA.SAMPR=0 or 1)	8x Over-sampling (CTRLA.SAMPR=2 or 3)
0x0	7-8-9	3-4-5
0x1	9-10-11	4-5-6
0x2	11-12-13	5-6-7
0x3	13-14-15	6-7-8

Bits 21:20 – RXPO[1:0]: Receive Data Pinout
These bits define the receive data (RxD) pin configuration.

These bits are not synchronized.

RXPO[1:0]	Name	Description
0x0	PAD[0]	SERCOM PAD[0] is used for data reception
0x1	PAD[1]	SERCOM PAD[1] is used for data reception

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

28.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
		LOWTOUT			SCLSM		SPEED[1:0]	
Access		R/W			R/W		R/W	R/W
Reset		0			0		0	0

Bit	23	22	21	20	19	18	17	16
	SEXTTOEN		SDAHOLD[1:0]					PINOUT
Access	R/W		R/W	R/W				R/W
Reset	0		0	0				0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – LOWTOUT: SCL Low Time-Out
This bit enables the SCL low time-out. If SCL is held low for 25ms-35ms, the slave will release its clock hold, if enabled, and reset the internal state machine. Any interrupt flags set at the time of time-out will remain set.

Value	Description
0	Time-out disabled.
1	Time-out enabled.

Bit 27 – SCLSM: SCL Clock Stretch Mode
This bit controls when SCL will be stretched for software interaction.

This bit is not synchronized.

Value	Description
0	SCL stretch according to Figure 28-9
1	SCL stretch only after ACK bit according to Figure 28-10

Bits 25:24 – SPEED[1:0]: Transfer Speed
These bits define bus speed.

These bits are not synchronized.

Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
			TXUR1	TXUR0			TXRDY1	TXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
			RXOR1	RXOR0			RXRDY1	RXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 13,12 – TXURx : Transmit Underrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Underrun x Interrupt Enable bit, which disables the Transmit Underrun x interrupt.

Value	Description
0	The Transmit Underrun x interrupt is disabled.
1	The Transmit Underrun x interrupt is enabled.

Bits 9,8 – TXRDYx : Transmit Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Ready x Interrupt Enable bit, which disables the Transmit Ready x interrupt.

Value	Description
0	The Transmit Ready x interrupt is disabled.
1	The Transmit Ready x interrupt is enabled.

Bits 4,5 – RXORx : Receive Overrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Overrun x Interrupt Enable bit, which disables the Receive Overrun x interrupt.

Value	Description
0	The Receive Overrun x interrupt is disabled.
1	The Receive Overrun x interrupt is enabled.

Bits 1,0 – RXRDYx : Receive Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Ready x Interrupt Enable bit, which disables the Receive Ready x interrupt.

Value	Description
0	The Receive Ready x interrupt is disabled.
1	The Receive Ready x interrupt is enabled.

The user can follow the current bank looking at Current Bank bit in PSTATUS (PSTATUS.CURBK) and by looking at Data Toggle for IN pipe bit in PSTATUS (PSTATUS.DTGLIN).

When the pipe is configured as single bank (Pipe Bank bit in PCFG (PCFG.BK) is 0), only PINTFLAG.TRCPT0 and PSTATUS.BK0 are used. When the pipe is configured as dual bank (PCFG.BK is 1), both PINTFLAG.TRCPT0/1 and PSTATUS.BK0/1 are used.

32.6.3.11 Management of OUT Pipes

OUT packets are sent by the host. All the data stored in the bank will be sent to the device provided the bank is filled. The pipe and its descriptor in RAM must be configured.

The host can send data to the device by writing to the data bank 0 in single bank or the data bank 0/1 in dual bank.

The generation of OUT packet starts when the pipe is unfrozen (PSTATUS.PFREEZE is zero).

The user writes the OUT data to the data buffer pointer by ADDR in the pipe descriptor and allows the USB to send the data by writing a one to the PSTATUS.BK0/1RDY. This will also cause a switch to the next bank if the OUT pipe is part of a dual bank configuration.

PINTFLAGn.TRCPT0/1 must be cleared before setting PSTATUS.BK0/1RDY to avoid missing an PINTFLAGn.TRCPT0/1 event.

32.6.3.12 Alternate Pipe

The user has the possibility to run sequentially several logical pipes on the same physical pipe. It allows addressing of any device endpoint of any attached device on the bus.

Before switching pipe, the user should save the pipe context (Pipe registers and descriptor for pipe n).

After switching pipe, the user should restore the pipe context (Pipe registers and descriptor for pipe n) and in particular PCFG, and PSTATUS.

32.6.3.13 Data Flow Error

This error exists only for isochronous and interrupt pipes for both IN and OUT directions. It sets the Transmit Fail bit in PINTFLAG (PINTFLAG.TRFAIL), which triggers an interrupt if the Transmit Fail bit in PINTENCLR/SET(PINTENCLR/SET.TRFAIL) is set. The user must check the Pipe Interrupt Summary register (PINTSMRY) to find out the pipe which triggered the interrupt. Then the user must check the origin of the interrupt's bank by looking at the Pipe Bank Status register (STATUS_BK) for each bank. If the Error Flow bit in the STATUS_BK (STATUS_BK.ERRORFLOW) is set then the user is able to determine the origin of the data flow error. As the user knows that the endpoint is an IN or OUT the error flow can be deduced as OUT underflow or as an IN overflow.

An underflow can occur during an OUT stage if the host attempts to send data from an empty bank. If a new transaction is successful, the relevant bank descriptor STATUS_BK.ERRORFLOW will be cleared.

An overflow can occur during an IN stage if the device tries to send a packet while the bank is full. Typically this occurs when a CPU is not fast enough. The packet data is not written to the bank and is lost. If a new transaction is successful, the relevant bank descriptor STATUS_BK.ERRORFLOW will be cleared.

32.6.3.14 CRC Error

This error exists only for isochronous IN pipes. It sets the PINTFLAG.TRFAIL, which triggers an interrupt if PINTENCLR/SET.TRFAIL is set. The user must check the PINTSMRY to find out the pipe which triggered the interrupt. Then the user must check the origin of the interrupt's bank by looking at the bank descriptor STATUS_BK for each bank and if the CRC Error bit in STATUS_BK (STATUS_BK.CRCERR) is set then the user is able to determine the origin of the CRC error. A CRC error can occur during the IN stage if the USB detects a corrupted packet. The IN packet will remain stored in the bank and PINTFLAG.TRCPT0/1 will be set.

33. ADC – Analog-to-Digital Converter

33.1 Overview

The Analog-to-Digital Converter (ADC) converts analog signals to digital values. The ADC has 12-bit resolution, and is capable of converting up to 350ksps. The input selection is flexible, and both differential and single-ended measurements can be performed. An optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

ADC measurements can be started by either application software or an incoming event from another peripheral in the device. ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used.

An integrated temperature sensor is available for use with the ADC. The bandgap voltage as well as the scaled I/O and core voltages can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user-defined thresholds, with minimum software intervention required.

The ADC may be configured for 8-, 10- or 12-bit results, reducing the conversion time. ADC conversion results are provided left- or right-adjusted, which eases calculation when the result is represented as a signed value. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

33.2 Features

- 8-, 10- or 12-bit resolution
- Up to 350,000 samples per second (350ksps)
- Differential and single-ended inputs
  - Up to 32 analog input
  - 25 positive and 10 negative, including internal and external
- Five internal inputs
  - Bandgap
  - Temperature sensor
  - DAC
  - Scaled core supply
  - Scaled I/O supply
- 1/2x to 16x gain
- Single, continuous and pin-scan conversion options
- Windowing monitor with selectable channel
- Conversion range:
  - V_{ref} [1v to V_{DDANA} - 0.6V]
  - ADCx * GAIN [0V to -V_{ref}]
- Built-in internal reference and external reference options
  - Four bits for reference selection

Name: DATA
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0]: Data value to be converted
DATA register contains the 10-bit value that is converted to a voltage by the DAC. The adjustment of these 10 bits within the 16-bit register is controlled by CTRLB.LEFTADJ.

Table 35-1. Valid Data Bits

CTRLB.LEFTADJ	DATA	Description
0	DATA[9:0]	Right adjusted, 10-bits
1	DATA[15:6]	Left adjusted, 10-bits

35.8.9 Data Buffer

Name: DATABUF
Offset: 0x0C
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	DATABUF[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATABUF[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATABUF[15:0]: Data Buffer
DATABUF contains the value to be transferred into DATA register.

Figure 37-17. 10 Sensor / PTC_GCLK = 2MHz / FREQ_MODE_HOP

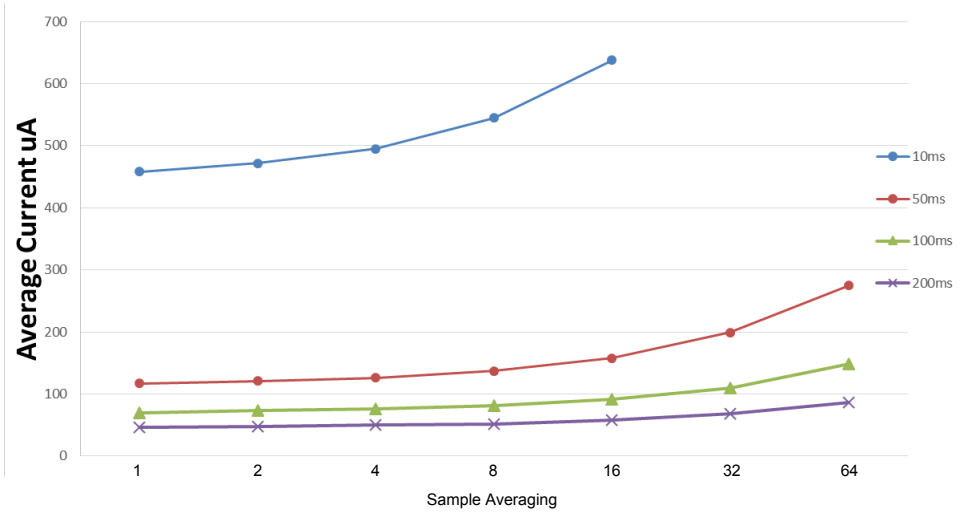


Figure 37-18. 100 Sensor / PTC_GCLK = 4MHz / FREQ_MODE_NONE

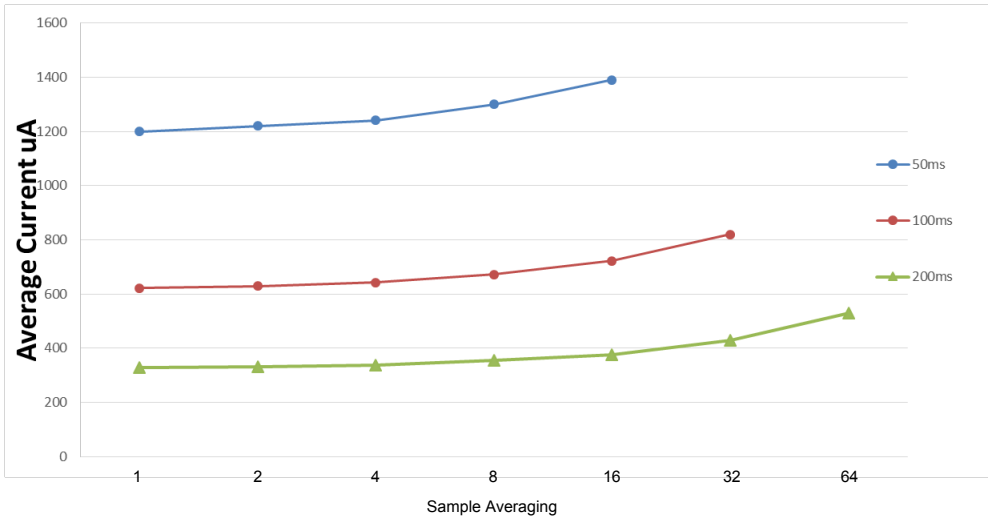


Table 37-61. SPI Timing Characteristics and Requirements(1)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master			84		ns
t_{SCKW}	SCK high/low width	Master		-	$0.5*t_{SCK}$	-	
t_{SCKR}	SCK rise time(2)	Master		-	-	-	
t_{SCKF}	SCK fall time(2)	Master		-	-	-	
t_{MIS}	MISO setup to SCK	Master		-	21	-	
t_{MIH}	MISO hold after SCK	Master		-	13	-	
t_{MOS}	MOSI setup SCK	Master		-	$t_{SCK}/2 - 3$	-	
t_{MOH}	MOSI hold after SCK	Master		-	3	-	
t_{SSCK}	Slave SCK Period	Slave		$1*t_{CLK\_APB}$	-	-	
t_{SSCKW}	SCK high/low width	Slave		$0.5*t_{SSCK}$	-	-	
t_{SSCKR}	SCK rise time(2)	Slave		-	-	-	
t_{SSCKF}	SCK fall time(2)	Slave		-	-	-	
t_{SIS}	MOSI setup to SCK	Slave		$t_{SSCK}/2 - 9$	-	-	
t_{SIH}	MOSI hold after SCK	Slave		$t_{SSCK}/2 - 3$	-	-	
t_{SSS}	SS setup to SCK	Slave	PRELOADEN =1	$2*t_{CLK\_APB} + t_{SOS}$	-	-	
			PRELOADEN =0	$t_{SOS}+7$	-	-	
t_{SSH}	SS hold after SCK	Slave		$t_{SIH} - 4$	-	-	
t_{SOS}	MISO setup SCK	Slave		-	$t_{SSCK}/2 - 18$	-	
t_{SOH}	MISO hold after SCK	Slave		-	18	-	
t_{SOSS}	MISO setup after SS low	Slave		-	18	-	
t_{SOSH}	MISO hold after SS high	Slave		-	10	-	

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. See I/O Pin Characteristics

37.15.3 SERCOM in I²C Mode Timing

This section describes the requirements for devices connected to the I²C Interface Bus.

Periodic Events: Bit names updated fro, PERx to PEREOx in example, Figure 19-4. CLOCK.HOUR[4:0]: Updated Table 19-4 Mode 0 and Mode 2: CMPx bit renamed to CMP0 since only one CMP0 is available. Bit description of CLOCK.HOUR[4:0]: Updated Table 19-4 ALARMn register renamed to ALARM0.
DMAC – Direct Memory Access Controller
Updated block diagram, Block Diagram. General updated description.
EIC – External Interrupt Controller
Register Summary and Register Description: EVCTRL register: Added bits EXTINTO17 and EXTINTO16 in bit position 17 and 16 respectively. INTENCLR, INTENSET, INTENFLAG registers: Added bits EXTINT17 and EXTINT16 in bit position 17 and 16 respectively. WAKEUP register: Added bits WAKEUPEN17 and WAKEUPEN16 in bit position 17 and 16 respectively. CONFIG2 register added, CONFIG0 and CONFIG1 registers updated: Added bits FILTEN0...31 and SENSE0...31.
NVMCTRL – Non-Volatile Memory Controller
CTRLB register: Removed table from NVM Read Wait States description (RWS[3:0])
PORT - I/O Pin Controller
Instances of the term “pad” replaced with “pin”. Instances of the term “bundle” replaced with “group” and “interface”. Basic Operation description updated. Peripheral Multiplexing n (PMUX0) register: Offset formula updated.
EVSYS – Event System
Updated information in Features. Power Management updated: Description of on how event generators can generate an event when the system clock is stopped moved to Sleep Mode Operation. Clocks updated: Renamed EVSYS channel dedicated generic clock from GCLK_EVSYS_x to GCLK_EVSYS_CHANNELx. Updated description in Principle of Operation. Updated description in sub sections of Basic Operation. Updated description in The Overrun Channel n Interrupt. Channel x Overrun bit description in INTFLAG updated.
SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter
Updated description in Break Character Detection and Auto-Baud. Updated description in Start-of-Frame Detection.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.9	+/-1.2	+/-2.0	LSB
			V_{DD} = 3.6V	+/-0.9	+/-1.1	+/-1.5	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-1.1	+/-1.7	+/-3.0	
			V_{DD} = 3.6V	+/-1.0	+/-1.1	+/-1.6	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-1.1	+/-1.4	+/-2.5	
			V_{DD} = 3.6V	+/-1.0	+/-1.5	+/-1.8	
	Gain error	Ext. V_{REF}		+/-1.0	+/-5	+/-10	mV
	Offset error	Ext. V_{REF}		+/-2	+/-3	+/-8	mV

Table 44-23. Accuracy Characteristics(1)(Device Variant B)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
RES	Input resolution			-	-	10	Bits
INL	Integral non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	0.7	0.75	2.0	LSB
			V_{DD} = 3.6V	0.6	0.65	1.5	
		V_{REF} = V_{DDANA}	V_{DD} = 1.6V	0.6	0.85	2.0	
			V_{DD} = 3.6V	0.5	0.8	1.5	
		V_{REF}= INT1V	V_{DD} = 1.6V	0.5	0.75	1.5	
			V_{DD} = 3.6V	0.7	0.8	1.5	
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.3	+/-0.4	+/-1.0	LSB
			V_{DD} = 3.6V	+/-0.25	+/-0.4	+/-0.75	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-0.4	+/-0.55	+/-1.5	
			V_{DD} = 3.6V	+/-0.2	+/-0.3	+/-0.75	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-0.5	+/-0.7	+/-1.5	
			V_{DD} = 3.6V	+/-0.4	+/-0.7	+/-1.5	
	Gain error	Ext. V_{REF}		+/-0.5	+/-5	+/-12	mV
	Offset error	Ext. V_{REF}		+/-2	+/-1.5	+/-8	mV

1. All values measured using a conversion rate of 350ksps.