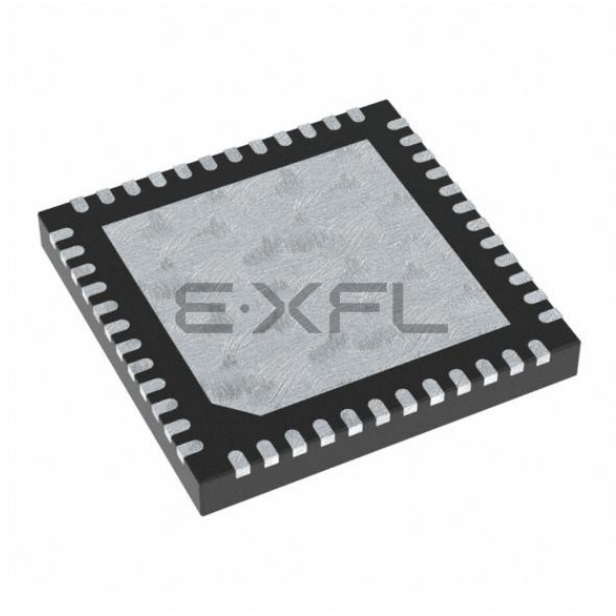

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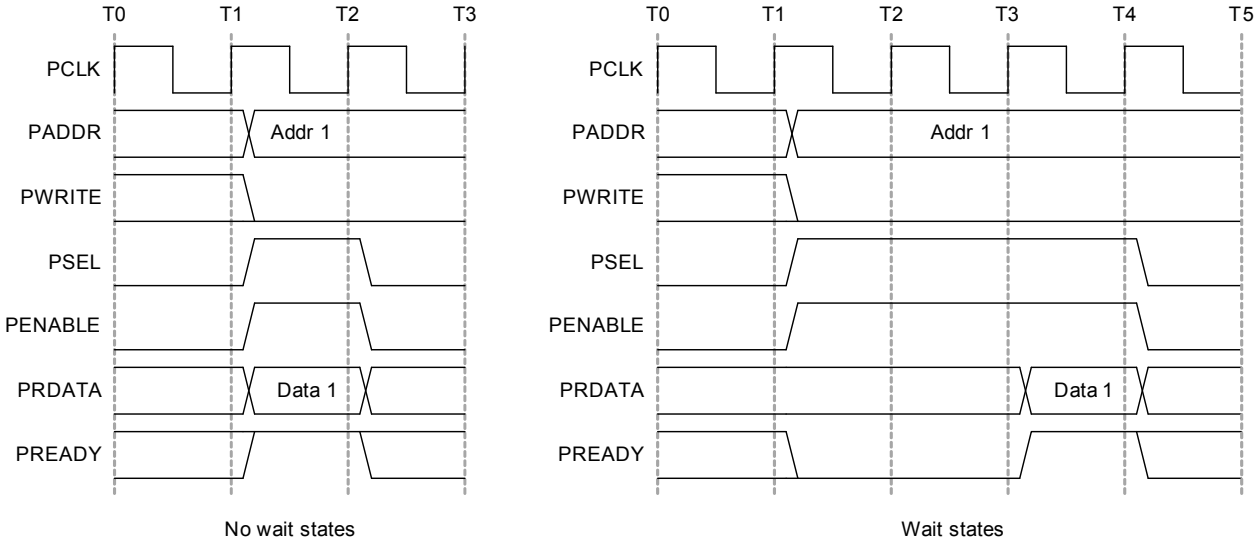
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g18a-mft

Figure 11-2. APB Read Access.



Related Links

PM – Power Manager

11.6 PAC - Peripheral Access Controller

11.6.1 Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

Write-protect registers allow the user to disable a selected peripheral's write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – WDT:
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – GCLK
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – SYSCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

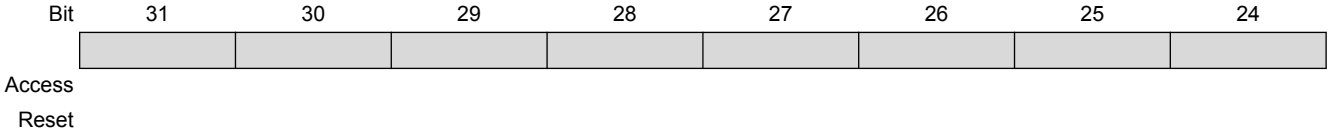
Bit 1 – PM
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000000
Property: –



15.6.2 Basic Operation

15.6.2.1 Initialization

Before a Generator is enabled, the corresponding clock source should be enabled. The Peripheral clock must be configured as outlined by the following steps:

1. The Generic Clock Generator division factor must be set by performing a single 32-bit write to the Generic Clock Generator Division register (GENDIV):
   - The Generic Clock Generator that will be selected as the source of the generic clock by setting the ID bit group (GENDIV.ID).
   - The division factor must be selected by the DIV bit group (GENDIV.DIV)
     Note: Refer to *Generic Clock Generator Division register (GENDIV)* for details.
2. The generic clock generator must be enabled by performing a single 32-bit write to the Generic Clock Generator Control register (GENCTRL):
   - The Generic Clock Generator will be selected as the source of the generic clock by the ID bit group (GENCTRL.ID)
   - The Generic Clock generator must be enabled (GENCTRL.GENEN=1)
     Note: Refer to *Generic Clock Generator Control register (GENCTRL)* for details.
3. The generic clock must be configured by performing a single 16-bit write to the Generic Clock Control register (CLKCTRL):
   - The Generic Clock that will be configured via the ID bit group (CLKCTRL.ID)
   - The Generic Clock Generator used as the source of the generic clock by writing the GEN bit group (CLKCTRL.GEN)
     Note: Refer to *Generic Clock Control register (CLKCTRL)* for details.

Related Links

GENDIV

GENCTRL

CLKCTRL

15.6.2.2 Enabling, Disabling and Resetting

The GCLK module has no enable/disable bit to enable or disable the whole module.

The GCLK is reset by setting the Software Reset bit in the Control register (CTRL.SWRST) to 1. All registers in the GCLK will be reset to their initial state, except for Generic Clocks Multiplexer and associated Generators that have their Write Lock bit set to 1 (CLKCTRL.WRTLOCK). For further details, refer to Configuration Lock.

15.6.2.3 Generic Clock Generator

Each Generator (GCLK_GEN) can be set to run from one of eight different clock sources except GCLKGEN[1], which can be set to run from one of seven sources. GCLKGEN[1] is the only Generator that can be selected as source to other Generators but can not act as source to itself.

Each generator GCLKGEN[x] can be connected to one specific pin GCLK_IO[x]. The GCLK_IO[x] can be set to act as source to GCLKGEN[x] or GCLK_IO[x] can be set up to output the clock generated by GCLKGEN[x].

The selected source can be divided. Each Generator can be enabled or disabled independently.

Each GCLKGEN clock signal can then be used as clock source for Generic Clock Multiplexers. Each Generator output is allocated to one or several Peripherals.

GCLKGEN[0], is used as GCLK_MAIN for the synchronous clock controller inside the Power Manager.

Table 15-5. Generic Clock Selection ID and CLKCTRL Value after User Reset

Module Instance	Reset Value after a User Reset		
	CLKCTRL.GEN	CLCTRL.CLKEN	CLKCTRL.WRTLOCK
RTC	0x00 if WRTLOCK=0 and CLKEN=0 No change if WRTLOCK=1 or CLKEN=1	0x00 if WRTLOCK=0 and CLKEN=0 No change if WRTLOCK=1 or CLKEN=1	No change
WDT	0x02 if WRTLOCK=0 No change if WRTLOCK=1	If WRTLOCK=0 0x01 if WDT Enable bit in NVM User Row written to one 0x00 if WDT Enable bit in NVM User Row written to zero If WRTLOCK=1 no change	No change
Others	0x00 if WRTLOCK=0 No change if WRTLOCK=1	0x00 if WRTLOCK=0 No change if WRTLOCK=1	No change

Value	Name	Description
0x00	GCLK_DFLL48M_REF	DFLL48M Reference
0x01	GCLK_DPLL	FDPLL96M input clock source for reference
0x02	GCLK_DPLL_32K	FDPLL96M 32kHz clock for FDPLL96M internal lock timer
0x03	GCLK_WDT	WDT
0x04	GCLK_RTC	RTC
0x05	GCLK_EIC	EIC
0x06	GCLK_USB	USB
0x07	GCLK_EVSYS_CHANNEL_0	EVSYS_CHANNEL_0
0x08	GCLK_EVSYS_CHANNEL_1	EVSYS_CHANNEL_1
0x09	GCLK_EVSYS_CHANNEL_2	EVSYS_CHANNEL_2
0x0A	GCLK_EVSYS_CHANNEL_3	EVSYS_CHANNEL_3
0x0B	GCLK_EVSYS_CHANNEL_4	EVSYS_CHANNEL_4
0x0C	GCLK_EVSYS_CHANNEL_5	EVSYS_CHANNEL_5
0x0D	GCLK_EVSYS_CHANNEL_6	EVSYS_CHANNEL_6
0x0E	GCLK_EVSYS_CHANNEL_7	EVSYS_CHANNEL_7
0x0F	GCLK_EVSYS_CHANNEL_8	EVSYS_CHANNEL_8
0x10	GCLK_EVSYS_CHANNEL_9	EVSYS_CHANNEL_9
0x11	GCLK_EVSYS_CHANNEL_10	EVSYS_CHANNEL_10
0x12	GCLK_EVSYS_CHANNEL_11	EVSYS_CHANNEL_11
0x13	GCLK_SERCOMx_SLOW	SERCOMx_SLOW
0x14	GCLK_SERCOM0_CORE	SERCOM0_CORE
0x15	GCLK_SERCOM1_CORE	SERCOM1_CORE
0x16	GCLK_SERCOM2_CORE	SERCOM2_CORE
0x17	GCLK_SERCOM3_CORE	SERCOM3_CORE
0x18	GCLK_SERCOM4_CORE	SERCOM4_CORE
0x19	GCLK_SERCOM5_CORE	SERCOM5_CORE
0x1A	GCLK_TCC0, GCLK_TCC1	TCC0,TCC1
0x1B	GCLK_TCC2, GCLK_TC3	TCC2,TC3
0x1C	GCLK_TC4, GCLK_TC5	TC4,TC5

Value	Name	Description
0x0	BYTE	8-bit bus transfer
0x1	HWORD	16-bit bus transfer
0x2	WORD	32-bit bus transfer
other		Reserved

Bits 4:3 – BLOCKACT[1:0]: Block Action
These bits define what actions the DMAC should take after a block transfer has completed.

BLOCKACT[1:0]	Name	Description
0x0	NOACT	Channel will be disabled if it is the last block transfer in the transaction
0x1	INT	Channel will be disabled if it is the last block transfer in the transaction and block interrupt
0x2	SUSPEND	Channel suspend operation is completed
0x3	BOTH	Both channel suspend operation and block interrupt

Bits 2:1 – EVOSEL[1:0]: Event Output Selection
These bits define the event output selection.

EVOSEL[1:0]	Name	Description
0x0	DISABLE	Event generation disabled
0x1	BLOCK	Event strobe when block transfer complete
0x2		Reserved
0x3	BEAT	Event strobe when beat transfer complete

Bit 0 – VALID: Descriptor Valid
Writing a '0' to this bit in the Descriptor or Write-Back memory will suspend the DMA channel operation when fetching the corresponding descriptor.

The bit is automatically cleared in the Write-Back memory section when channel is aborted, when an error is detected during the block transfer, or when the block transfer is completed.

Value	Description
0	The descriptor is not valid.
1	The descriptor is valid.

20.10.2 Block Transfer Count

The BTCNT register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Name: BTCNT
Offset: 0x02
Reset: -
Property: -

Bit	7	6	5	4	3	2	1	0
	OUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUT[31:0]: PORT Data Output Value
For pins configured as outputs via the Data Direction register (DIR), these bits set the logical output drive level.

For pins configured as inputs via the Data Direction register (DIR) and with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN), these bits will set the input pull direction.

Value	Description
0	The I/O pin output is driven low, or the input is connected to an internal pull-down.
1	The I/O pin output is driven high, or the input is connected to an internal pull-up.

23.8.6 Data Output Value Clear

This register allows the user to set one or more output I/O pin drive levels low, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Set (OUTSET) registers.

Name: OUTCLR
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	OUTCLR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	OUTCLR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OUTCLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTCLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTCLR[31:0]: PORT Data Output Value Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit will clear the corresponding bit in the OUT register. Pins configured as outputs via the Data Direction register (DIR) will be set to low output drive level. Pins configured as inputs via DIR and

- Data (DATA) when in master operation

Required write-synchronization is denoted by the "Write-Synchronized" property in the register description.

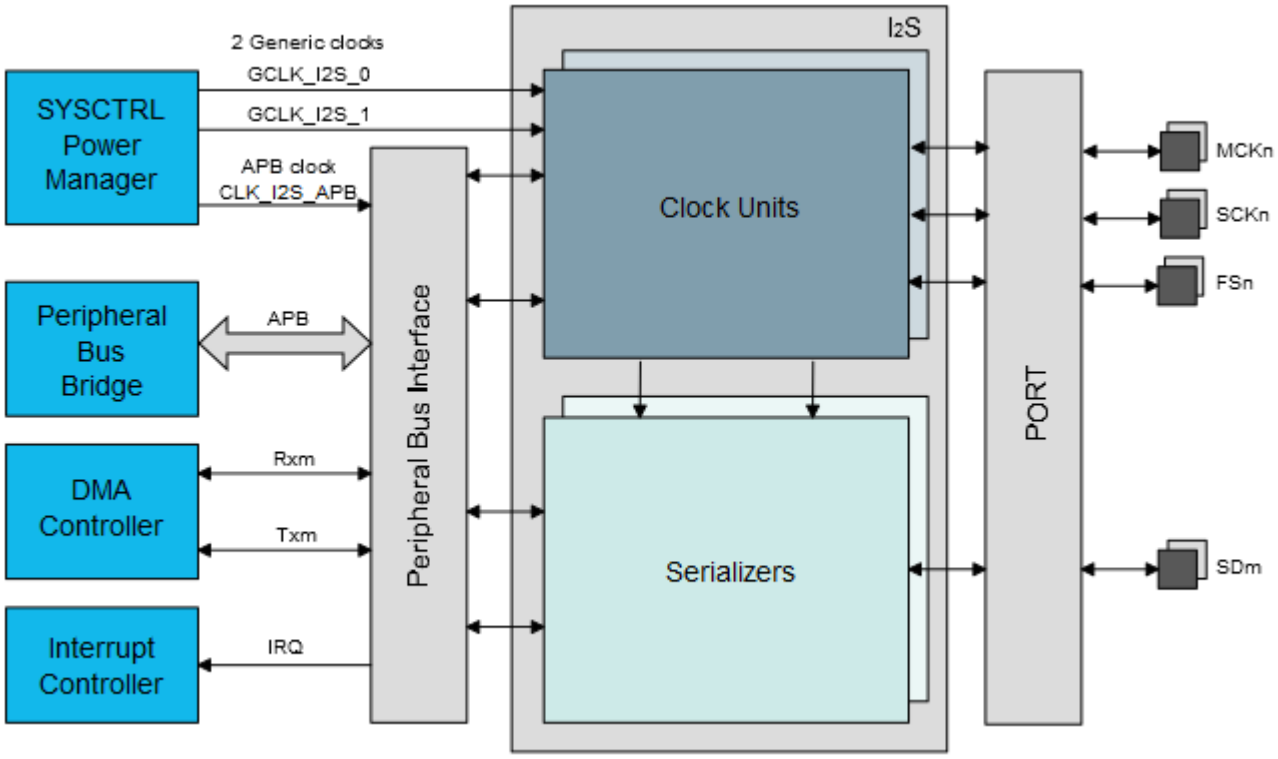
Related Links

Register Synchronization

  - Suitable for a wide range of sample frequencies *fs*, including 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, and 192kHz
  - 16×*fs* to 1024×*fs* Master Clock generated for external audio CODECs
- Master, slave, and controller modes:
  - Master: Data received/transmitted based on internally-generated clocks. Output Serial Clock on SCKn pin, Master Clock on MCKn pin, and Frame Sync Clock on FSn pin
  - Slave: Data received/transmitted based on external clocks on Serial Clock pin (SCKn) or Master Clock pin (MCKn)
  - Controller: Only output internally generated Master clock (MCKn), Serial Clock (SCKn), and Frame Sync Clock (FSn)
- Individual enabling and disabling of Clock Units and Serializers
- DMA interfaces for each Serializer receiver or transmitter to reduce processor overhead:
  - Either one DMA channel for all data slots or
  - One DMA channel per data channel in stereo
- Smart Data Holding register management to avoid data slots mix after overrun or underrun

29.3 Block Diagram

Figure 29-1. I²S Block Diagram



Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
			TXUR1	TXUR0			TXRDY1	TXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
			RXOR1	RXOR0			RXRDY1	RXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 13,12 – TXURx : Transmit Underrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Underrun x Interrupt Enable bit, which disables the Transmit Underrun x interrupt.

Value	Description
0	The Transmit Underrun x interrupt is disabled.
1	The Transmit Underrun x interrupt is enabled.

Bits 9,8 – TXRDYx : Transmit Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Ready x Interrupt Enable bit, which disables the Transmit Ready x interrupt.

Value	Description
0	The Transmit Ready x interrupt is disabled.
1	The Transmit Ready x interrupt is enabled.

Bits 4,5 – RXORx : Receive Overrun x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Overrun x Interrupt Enable bit, which disables the Receive Overrun x interrupt.

Value	Description
0	The Receive Overrun x interrupt is disabled.
1	The Receive Overrun x interrupt is enabled.

Bits 1,0 – RXRDYx : Receive Ready x Interrupt Enable [x=1..0]
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Ready x Interrupt Enable bit, which disables the Receive Ready x interrupt.

Value	Description
0	The Receive Ready x interrupt is disabled.
1	The Receive Ready x interrupt is enabled.

31.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0		RESOLUTION[1:0]					ENABLE	SWRST
0x01		15:8		ALOCK	PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
0x02		23:16								
0x03		31:24					CPTEN3	CPTEN2	CPTEN1	CPTEN0
0x04	CTRLBCLR	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x06 ... 0x07	Reserved									
0x08	SYNCBUSY	7:0	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x09		15:8					CC3	CC2	CC1	CC0
0x0A		23:16		CCB3	CCB2	CCB1	CCB0	PERB	WAVEB	PATTB
0x0B		31:24								
0x0C	FCTRLA	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
0x0D		15:8		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
0x0E		23:16	BLANKVAL[7:0]							
0x0F		31:24					FILTERVAL[3:0]			
0x10	FCTRLB	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
0x11		15:8		CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
0x12		23:16	BLANKVAL[7:0]							
0x13		31:24					FILTERVAL[3:0]			
0x14	WEXCTRL	7:0							OTMX[1:0]	
0x15		15:8					DTIEN3	DTIEN2	DTIEN1	DTIEN0
0x16		23:16	DTLS[7:0]							
0x17		31:24	DTHS[7:0]							
0x18	DRVCTRL	7:0	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
0x19		15:8	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
0x1A		23:16	INVEN7	INVEN6	INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
0x1B		31:24	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
0x1C ... 0x1D	Reserved									
0x1E	DBGCTRL	7:0						FDDBD		DBGRUN
0x1F	Reserved									
0x20	EVCTRL	7:0	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
0x21		15:8	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO
0x22		23:16					MCEI3	MCEI2	MCEI1	MCEI0
0x23		31:24					MCEO3	MCEO2	MCEO1	MCEO0
0x24	INTENCLR	7:0					ERR	CNT	TRG	OVF
0x25		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS			
0x26		23:16					MC3	MC2	MC1	MC0
0x27		31:24								

Bit	15	14	13	12	11	10	9	8
	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:28 – FILTERVAL1[3:0]: Non-Recoverable Fault Input 1 Filter Value
These bits define the filter value applied on TCE1 event input line. When the TCE1 event input line is configured as a synchronous event, this value must be 0x0.

Bits 27:24 – FILTERVAL0[3:0]: Non-Recoverable Fault Input 0 Filter Value
These bits define the filter value applied on TCE0 event input line. When the TCE0 event input line is configured as a synchronous event, this value must be 0x0.

Bits 23,22,21,20,19,18,17,16 – INVENx: Waveform Output x Inversion
These bits are used to select inversion on the output of channel x.

Writing a '1' to INVENx inverts output from WO[x].

Writing a '0' to INVENx disables inversion of output from WO[x].

Bits 15,14,13,12,11,10,9,8 – NRVx: NRVx Non-Recoverable State x Output Value
These bits define the value of the enabled override outputs, under non-recoverable fault condition.

Bits 7,6,5,4,3,2,1,0 – NREx: Non-Recoverable State x Output Enable
These bits enable the override of individual outputs by NRVx value, under non-recoverable fault condition.

Value	Description
0	Non-recoverable fault tri-state the output.
1	Non-recoverable faults set the output to NRVx level.

31.8.8 Debug control

Name: DBGCTRL
Offset: 0x1E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						FDDBD		DBGRUN
Access						R/W		R/W
Reset						0		0

Bit 2 – FDDBD: Fault Detection on Debug Break Detection
This bit is not affected by software reset and should not be changed by software while the TCC is enabled.

Bit	7	6	5	4	3	2	1	0
	BK1RDY	BK0RDY	STALLRQ1	STALLRQ0		CURBK	DTGLIN	DTGLOUT
Access	W	W	W	W		W	W	W
Reset	0	0	0	0		0	0	0

Bit 7 – BK1RDY: Bank 1 Ready Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.BK1RDY bit.

Bit 6 – BK0RDY: Bank 0 Ready Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.BK0RDY bit.

Bit 5 – STALLRQ1: STALL bank 1 Request Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.STALLRQ1 bit.

Bit 4 – STALLRQ0: STALL bank 0 Request Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.STALLRQ0 bit.

Bit 2 – CURBK: Current Bank Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.CURBK bit.

Bit 1 – DTGLIN: Data Toggle IN Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.DTGLIN bit.

Bit 0 – DTGLOUT: Data Toggle OUT Clear
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the EPSTATUS.DTGLOUT bit.

32.8.3.3 EndPoint Status Set n

Name: EPSTATUSSETn
Offset: 0x105 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	BK1RDY	BK0RDY	STALLRQ1	STALLRQ0		CURBK	DTGLIN	DTGLOUT
Access	W	W	W	W		W	W	W
Reset	0	0	0	0		0	0	0

Bit 7 – BK1RDY: Bank 1 Ready Set
Writing a zero to this bit has no effect.

32.8.5.6 Host Interrupt Enable Register Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Name: INTENCLR
Offset: 0x14
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
							DDISC	DCONN
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RAMACER	UPRSM	DNRSM	WAKEUP	RST	HSOF		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 9 – DDISC: Device Disconnection Interrupt Disable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Device Disconnection interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Device Disconnection interrupt is disabled.
1	The Device Disconnection interrupt is enabled and an interrupt request will be generated when the Device Disconnection interrupt Flag is set.

Bit 8 – DCONN: Device Connection Interrupt Disable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the Device Connection interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The Device Connection interrupt is disabled.
1	The Device Connection interrupt is enabled and an interrupt request will be generated when the Device Connection interrupt Flag is set.

Bit 7 – RAMACER: RAM Access Interrupt Disable
Writing a zero to this bit has no effect.

Writing a one to this bit will clear the RAM Access interrupt Enable bit and disable the corresponding interrupt request.

Value	Description
0	The RAM Access interrupt is disabled.
1	The RAM Access interrupt is enabled and an interrupt request will be generated when the RAM Access interrupt Flag is set.

35.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Flag Status and Clear (INTFLAG) register
- Data Buffer (DATABUF) register

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger

Related Links

PAC - Peripheral Access Controller

35.5.9 Analog Connections

The DAC has one output pin (VOUT) and one analog input pin (VREFA) that must be configured first.

When internal input is used, it must be enabled before DAC Controller is enabled.

35.6 Functional Description

35.6.1 Principle of Operation

The DAC converts the digital value located in the Data register (DATA) into an analog voltage on the DAC output (VOUT).

A conversion is started when new data is written to the Data register. The resulting voltage is available on the DAC output after the conversion time. A conversion can also be started by input events from the Event System.

35.6.2 Basic Operation

35.6.2.1 Initialization

The following registers are enable-protected, meaning they can only be written when the DAC is disabled (CTRLA.ENABLE is zero):

- Control B register (CTRLB)
- Event Control register (EVCTRL)

Enable-protection is denoted by the Enable-Protected property in the register description.

Before enabling the DAC, it must be configured by selecting the voltage reference using the Reference Selection bits in the Control B register (CTRLB.REFSEL).

35.6.2.2 Enabling, Disabling and Resetting

The DAC Controller is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The DAC Controller is disabled by writing a '0' to CTRLA.ENABLE.

The DAC Controller is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the DAC will be reset to their initial state, and the DAC Controller will be disabled. Refer to the CTRLA register for details.

35.6.2.3 Enabling the Output Buffer

To enable the DAC output on the V_{OUT} pin, the output driver must be enabled by writing a one to the External Output Enable bit in the Control B register (CTRLB.EOEN).

Table 37-13. Typical USB Host Full Speed mode Current Consumption

USB Device state	Conditions	Typ.	Units
Wait connection	GCLK_USB is off, using USB wakeup asynchronous interrupt. USB bus not connected.	0.10	µA
Wait connection	GCLK_USB is on. USB bus not connected.	0.19	mA
Suspend	GCLK_USB is off, using USB wakeup asynchronous interrupt. USB bus in suspend mode.	201	µA
Suspend	GCLK_USB is on. USB bus in suspend mode.	0.83	mA
IDLE	Start Of Frame is running. No packet transferred.	1.17	mA
Active OUT	Start Of Frame is running. Bulk OUT on 100% bandwidth.	2.17	mA
Active IN	Start Of Frame is running. Bulk IN on 100% bandwidth.	10.3	mA

37.8 I/O Pin Characteristics

37.8.1 Normal I/O Pins

Table 37-14. Normal I/O Pins Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{PULL}	Pull-up - Pull-down resistance	All pins except for PA24 and PA25	20	40	60	kΩ
V_{IL}	Input low-level voltage	V_{DD}=1.62V-2.7V	-	-	0.25*V_{DD}	V
		V_{DD}=2.7V-3.63V	-	-	0.3*V_{DD}	
V_{IH}	Input high-level voltage	V_{DD}=1.62V-2.7V	0.7*V_{DD}	-	-	
		V_{DD}=2.7V-3.63V	0.55*V_{DD}	-	-	
V_{OL}	Output low-level voltage	V_{DD}>1.6V, I_{OL} maxI	-	0.1*V_{DD}	0.2*V_{DD}	
V_{OH}	Output high-level voltage	V_{DD}>1.6V, I_{OH} maxII	0.8*V_{DD}	0.9*V_{DD}	-	

Table 37-44. NVM Characteristics (Device Variant B and C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{FPP}	Page programming time	-	-	-	2.5	ms
t_{FRE}	Row erase time	-	-	-	1.2	ms
t_{FCE}	DSU chip erase time (CHIP_ERASE)	-	-	-	240	ms

37.12 Oscillators Characteristics

37.12.1 Crystal Oscillator (XOSC) Characteristics

37.12.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 37-45. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{CPXIN}	XIN clock frequency		-	-	32	MHz

37.12.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT . The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L + - C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Table 37-46. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Crystal oscillator frequency		0.4	-	32	MHz
ESR	Crystal Equivalent Series Resistance Safety Factor = 3 The AGC doesn't have any noticeable impact on these measurements.	f = 0.455 MHz, C_L = 100pF XOSC.GAIN = 0	-	-	5.6K	Ω
		f = 2MHz, C_L = 20pF XOSC.GAIN = 0	-	-	416	
		f = 4MHz, C_L = 20pF XOSC.GAIN = 1	-	-	243	
		f = 8 MHz, C_L = 20pF XOSC.GAIN = 2	-	-	138	
		f = 16 MHz, C_L = 20pF XOSC.GAIN = 3	-	-	66	
		f = 32MHz, C_L = 18pF XOSC.GAIN = 4	-	-	56	
C_{XIN}	Parasitic capacitor load		-	5.9	-	pF

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

16 – In Standby, Idle1 and Idle2 sleep modes the device might not wake up from sleep. An External Reset, Power on Reset or Watch Dog Reset will start the device again.
Errata reference: 13140
Fix/Workaround:
the SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20uA compared to numbers in the electrical characteristics chapter.

17 – Digital pin outputs from Timer/Counters, AC (Analog Comparator), GCLK (Generic Clock Controller), and SERCOM (I2C and SPI) do not change value during standby sleep mode.
Errata reference: 12537
Fix/Workaround:
Set the voltage regulator in Normal mode before entering STANDBY sleep mode in order to keep digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

18 – The voltage regulator in low power mode is not functional at temperatures above 85C.
Errata reference: 12291
Fix/Workaround:
Enable normal mode on the voltage regulator in standby sleep mode.
Example code:
// Set the voltage regulator in normal mode configuration in standby sleep mode
SYSCTRL->VREG.bit.RUNSTDBY = 1;

40.1.2.2 DSU

1 – If a debugger has issued a DSU Cold-Plugging procedure and then released the CPU from the resulting ""CPU Reset Extension"", the CPU will be held in ""CPU Reset Extension"" after any upcoming reset event.
Errata reference: 12015
Fix/workaround:
The CPU must be released from the ""CPU Reset Extension"" either by writing a one in the DSU STATUSA.CRSTEXT register or by applying an external reset with SWCLK high or by power cycling the device.

2 – The MBIST ""Pause-on-Error"" feature is not functional on this device.
Errata reference: 14324
Fix/Workaround:
Do not use the ""Pause-on-Error"" feature.

Add a NOP instruction between each write to CRCDATAIN register.

40.2.2.6 EIC

1 – When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using CTRLA ENABLE bit.
Errata reference: 15341
Fix/Workaround:
Clear the INTFLAG bit once the EIC enabled and before enabling the interrupts.

40.2.2.7 NVMCTRL

1 – Default value of MANW in NVM.CTRLB is 0.
This can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to NVM area.
Errata reference: 13134
Fix/Workaround:
Set MANW in the NVM.CTRLB to 1 at startup

40.2.2.8 I2S

1 – I2S RX serializer in LSBIT mode (SERCTRL.BITREV set) only works when the slot size is 32 bits.
Errata reference: 13320
Fix/Workaround:
In SERCTRL.SERMODE RX, SERCTRL.BITREV LSBIT must be used with CLKCTRL.SLOTSIZE 32.

40.2.2.9 SERCOM

1 – In USART autobaud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.
Errata reference: 13852
Fix/Workaround:
None

40.2.2.10 TCC

1 – FCTRLX.CAPTURE[CAPTMARK] does not work as described in the datasheet. CAPTMARK cannot be used to identify captured values triggered by fault inputs source A or B on the same channel.
Errata reference: 13316
Fix/Workaround:
Use two different channels to timestamp FaultA and FaultB.

2 – Using TCC in dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses, or shrink of left aligned pulses.
Errata reference: 15625
Fix/Workaround:
Do not use retrigger events/actions when TCC is configured in dithering mode.

Updated V_{DD} max from 3.63V to 3.63V in Absolute Maximum Ratings. Updated VDDIN pin from 57 to 56 in GPIO Clusters. Power Consumption: Updated Max values for STANDBY from 190.6µA and 197.3µA to 100µA in Table 37-7. Added Peripheral Power Consumption. I/O Pin Characteristics: tRISE and tFALL updated with different load conditions depending on the DVRSTR value in . I/O Pin Characteristics: Correct typo IOL and IOH Max values inverted between PORT.PINCFG.DRVSTR=0 and 1, tRISE and tFALL updated with different load conditions depending on the DVRSTR value in Table 37-14. Analog Characteristics: Removed note from Table 37-18. Analog-to-Digital (ADC) characteristics: Added Max DC supply current (I_{DD}), R_{SAMPLE} maximum value changed from 2.8kW to 3.5kW, Conversion time Typ value change to Min Value in Table 37-22. Digital to Analog Converter (DAC) Characteristics: Added Max DC supply current (I_{DD}) in Table 37-30. Analog Comparator Characteristics: Added Min and Max values for VSCALE INL, DNL, Offset Error and Gain Error in Table 37-34. Internal 1.1V Bandgap Reference Characteristics: Added Min and Max values, removed accuracy row in Table 37-36. SERCOM in I2C Mode Timing: Add Typical values for t_R in Table 37-62. Removed Asynchronous Watchdog Clock Characterization. 32.768kHz Internal oscillator (OSC32K) Characteristics: Added Max current consumption (I_{OSC32K}) in Table 37-53. Updated Crystal Oscillator Characteristics (XOSC32K) ESR maximum values, Crystal Oscillator Characteristics. Updated Crystal Oscillator Characteristics (XOSC) ESR maximum value, Crystal Oscillator Characteristics from 348kΩ to 141kΩ. Digital Frequency Locked Loop (DFLL48M) Characteristics: Updated presentation, now separating between Open- and Closed Loop Modes. Added f_{REF} Min and Max values to Table 37-50. Updated typical Startup time ($t_{STARTUP}$) from 6.1µs to 8µs in Table 37-51. Updated typical Fine lock time (t_{LFINE}) from 700µs to 600µs in Table 37-51. Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics: Added Current consumption ($I_{FDPLL96M}$), Period Jitter (Jp), Lock time (t_{LOCK}), Duty cycles parameters in Table 37-56. Added USB Characteristics. Timing Characteristics: Added SCK period (t_{SCK}) Typ value in Table 37-60.
Errata
Errata for revision B added.

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