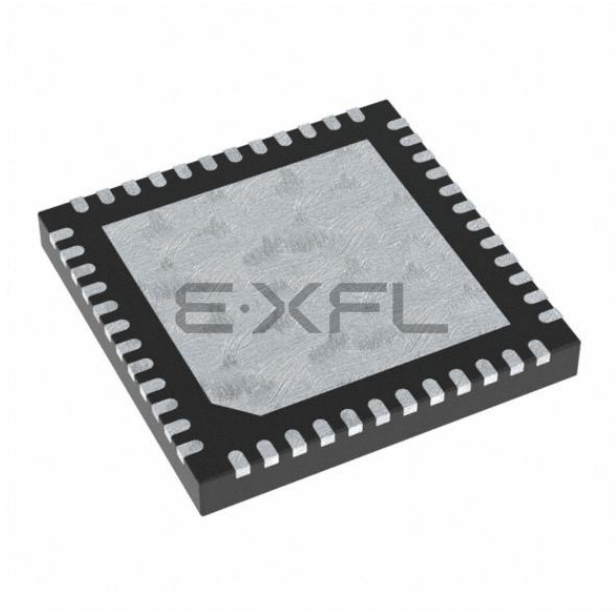

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21g18a-mu

13. DSU - Device Service Unit

13.1 Overview

The Device Service Unit (DSU) provides a means to detect debugger probes. This enables the ARM Debug Access Port (DAP) to have control over multiplexed debug pads and CPU reset. The DSU also provides system-level services to debug adapters in an ARM debug system. It implements a CoreSight Debug ROM that provides device identification as well as identification of other debug components within the system. Hence, it complies with the ARM Peripheral Identification specification. The DSU also provides system services to applications that need memory testing, as required for IEC60730 Class B compliance, for example. The DSU can be accessed simultaneously by a debugger and the CPU, as it is connected on the High-Speed Bus Matrix. For security reasons, some of the DSU features will be limited or unavailable when the device is protected by the NVMCTRL security bit.

Related Links

NVMCTRL – Non-Volatile Memory Controller

Security Bit

13.2 Features

- CPU reset extension
- Debugger probe detection (Cold- and Hot-Plugging)
- Chip-Erase command and status
- 32-bit cyclic redundancy check (CRC32) of any memory accessible through the bus matrix
- ARM® CoreSight™ compliant device identification
- Two debug communications channels
- Debug access port security filter
- Onboard memory built-in self-test (MBIST)

16.5.8 Register Access Protection

Registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC), except the following:

- Interrupt Flag register (INTFLAG).
- Reset Cause register (RCAUSE).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

Write-protection does not apply for accesses through an external debugger. Refer to *PAC – Peripheral Access Controller* for details.

Related Links

PAC - Peripheral Access Controller

16.5.9 Analog Connections

Not applicable.

16.6 Functional Description

16.6.1 Principle of Operation

16.6.1.1 Synchronous Clocks

The GCLK_MAIN clock from GCLK module provides the source for the main clock, which is the common root for the synchronous clocks for the CPU and APBx modules. The main clock is divided by an 8-bit prescaler, and each of the derived clocks can run from any tapping off this prescaler or the undivided main clock, as long as $f_{CPU} \geq f_{APBx}$. The synchronous clock source can be changed on the fly to respond to varying load in the application. The clocks for each module in each synchronous clock domain can be individually masked to avoid power consumption in inactive modules. Depending on the sleep mode, some clock domains can be turned off (see Table 16-4).

16.6.1.2 Reset Controller

The Reset Controller collects the various reset sources and generates reset for the device. The device contains a power-on-reset (POR) detector, which keeps the system reset until power is stable. This eliminates the need for external reset circuitry to guarantee stable operation when powering up the device.

16.6.1.3 Sleep Mode Controller

In ACTIVE mode, all clock domains are active, allowing software execution and peripheral operation. The PM Sleep Mode Controller allows the user to choose between different sleep modes depending on application requirements, to save power (see Table 16-4).

16.6.2 Basic Operation

16.6.2.1 Initialization

After a power-on reset, the PM is enabled and the Reset Cause register indicates the POR source (RCAUSE.POR). The default clock source of the GCLK_MAIN clock is started and calibrated before the CPU starts running. The GCLK_MAIN clock is selected as the main clock without any division on the prescaler. The device is in the ACTIVE mode.

By default, only the necessary clocks are enabled (see Table 16-1).

16.6.2.2 Enabling, Disabling and Resetting

The PM module is always enabled and can not be reset.

Bit 4 – NVMCTRL: NVMCTRL AHB Clock Mask

Value	Description
0	The AHB clock for the NVMCTRL is stopped.
1	The AHB clock for the NVMCTRL is enabled.

Bit 3 – DSU: DSU AHB Clock Mask

Value	Description
0	The AHB clock for the DSU is stopped.
1	The AHB clock for the DSU is enabled.

Bit 2 – HPB2: HPB2 AHB Clock Mask

Value	Description
0	The AHB clock for the HPB2 is stopped.
1	The AHB clock for the HPB2 is enabled.

Bit 1 – HPB1: HPB1 AHB Clock Mask

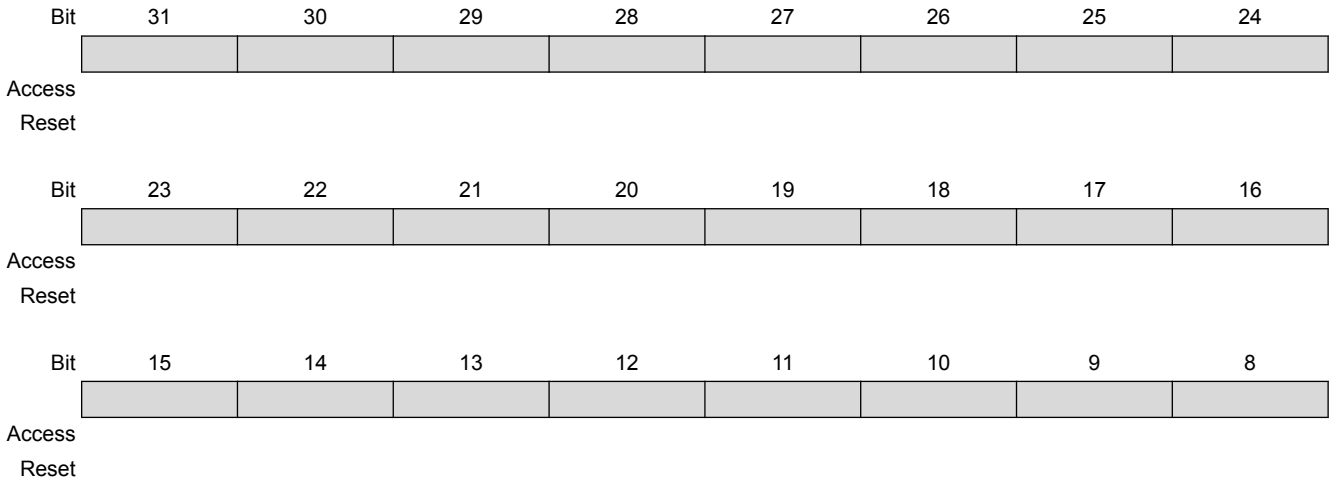
Value	Description
0	The AHB clock for the HPB1 is stopped.
1	The AHB clock for the HPB1 is enabled.

Bit 0 – HPB0: HPB0 AHB Clock Mask

Value	Description
0	The AHB clock for the HPB0 is stopped.
1	The AHB clock for the HPB0 is enabled.

16.8.8 APBA Mask

Name: APBAMASK
Offset: 0x18
Reset: 0x0000007F
Property: Write-Protected



Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	PAC0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bit 6 – EIC: EIC APB Clock Enable

Value	Description
0	The APBA clock for the EIC is stopped.
1	The APBA clock for the EIC is enabled.

Bit 5 – RTC: RTC APB Clock Enable

Value	Description
0	The APBA clock for the RTC is stopped.
1	The APBA clock for the RTC is enabled.

Bit 4 – WDT: WDT APB Clock Enable

Value	Description
0	The APBA clock for the WDT is stopped.
1	The APBA clock for the WDT is enabled.

Bit 3 – GCLK: GCLK APB Clock Enable

Value	Description
0	The APBA clock for the GCLK is stopped.
1	The APBA clock for the GCLK is enabled.

Bit 2 – SYSCTRL: SYSCTRL APB Clock Enable

Value	Description
0	The APBA clock for the SYSCTRL is stopped.
1	The APBA clock for the SYSCTRL is enabled.

Bit 1 – PM: PM APB Clock Enable

Value	Description
0	The APBA clock for the PM is stopped.
1	The APBA clock for the PM is enabled.

Bit 0 – PAC0: PAC0 APB Clock Enable

Value	Description
0	The APBA clock for the PAC0 is stopped.
1	The APBA clock for the PAC0 is enabled.

16.8.9 APBB Mask

Name: APBBMASK
Offset: 0x1C
Reset: 0x0000007F

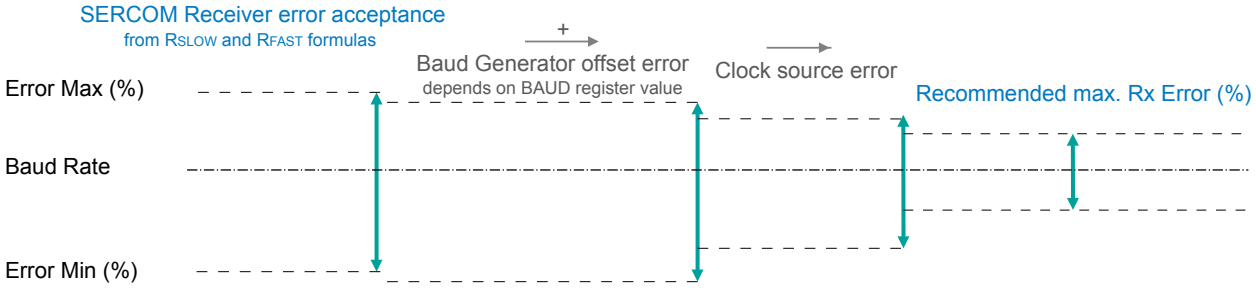
The following equations calculate the ratio of the incoming data rate and internal receiver baud rate:

$$R_{SLOW} = \frac{(D + 1)S}{S - 1 + D \cdot S + S_F} \quad , \quad R_{FAST} = \frac{(D + 2)S}{(D + 1)S + S_M}$$

- R_{SLOW} is the ratio of the slowest incoming data rate that can be accepted in relation to the receiver baud rate
- R_{FAST} is the ratio of the fastest incoming data rate that can be accepted in relation to the receiver baud rate
- D is the sum of character size and parity size (D = 5 to 10 bits)
- S is the number of samples per bit (S = 16, 8 or 3)
- S_F is the first sample number used for majority voting (S_F = 7, 3, or 2) when CTRLA.SAMPA=0.
- S_M is the middle sample number used for majority voting (S_M = 8, 4, or 2) when CTRLA.SAMPA=0.

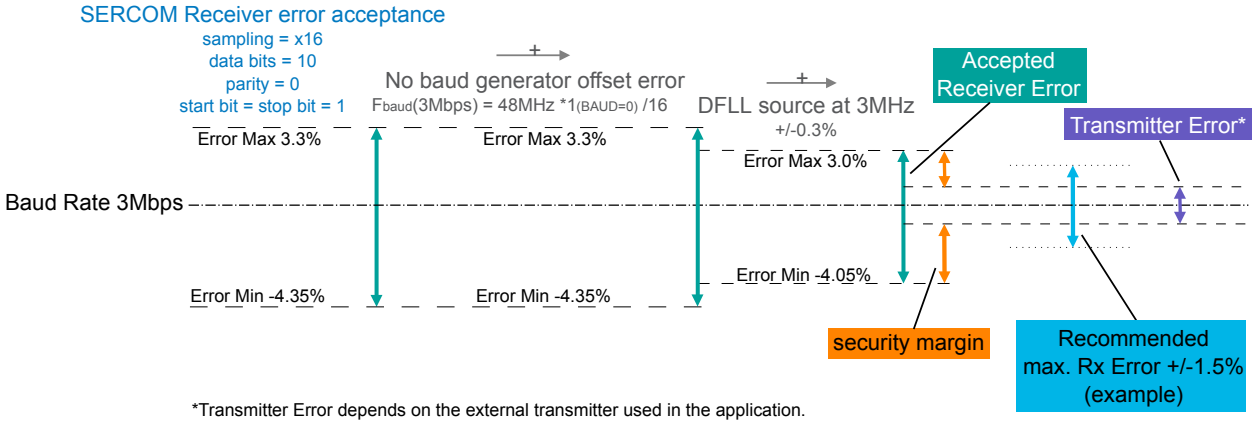
The recommended maximum Rx Error assumes that the receiver and transmitter equally divide the maximum total error. Its connection to the SERCOM Receiver error acceptance is depicted in this figure:

Figure 26-5. USART Rx Error Calculation



The recommendation values in the table above accommodate errors of the clock source and the baud generator. The following figure gives an example for a baud rate of 3Mbps:

Figure 26-6. USART Rx Error Calculation Example



*Transmitter Error depends on the external transmitter used in the application.
It is advised that it is within the Recommended max. Rx Error (+/-1.5% in this example).
Larger Transmitter Errors are acceptable but must lie within the Accepted Receiver Error.

Related Links

Clock Generation – Baud-Rate Generator

Asynchronous Arithmetic Mode BAUD Value Selection

26.6.3 Additional Features

26.6.3.1 Parity

Even or odd parity can be selected for error checking by writing 0x1 to the Frame Format bit field in the Control A register (CTRLA.FORM).

Value	Description
0	The transmitter is disabled or being enabled.
1	The transmitter is enabled or will be enabled when the USART is enabled.

Bit 13 – PMODE: Parity Mode
This bit selects the type of parity used when parity is enabled (CTRLA.FORM is '1'). The transmitter will automatically generate and send the parity of the transmitted data bits within each frame. The receiver will generate a parity value for the incoming data and parity bit, compare it to the parity mode and, if a mismatch is detected, STATUS.PERR will be set.

This bit is not synchronized.

Value	Description
0	Even parity.
1	Odd parity.

Bit 10 – ENC: Encoding Format
This bit selects the data encoding format.

This bit is not synchronized.

Value	Description
0	Data is not encoded.
1	Data is IrDA encoded.

Bit 9 – SFDE: Start of Frame Detection Enable
This bit controls whether the start-of-frame detector will wake up the device when a start bit is detected on the RxD line.

This bit is not synchronized.

SFDE	INTENSET.RXS	INTENSET.RXC	Description
0	X	X	Start-of-frame detection disabled.
1	0	0	Reserved
1	0	1	Start-of-frame detection enabled. RXC wakes up the device from all sleep modes.
1	1	0	Start-of-frame detection enabled. RXS wakes up the device from all sleep modes.
1	1	1	Start-of-frame detection enabled. Both RXC and RXS wake up the device from all sleep modes.

Bit 8 – COLDEN: Collision Detection Enable
This bit enables collision detection.

This bit is not synchronized.

Value	Description
0	Collision detection is not enabled.
1	Collision detection is enabled.

28. SERCOM I²C – SERCOM Inter-Integrated Circuit

28.1 Overview

The inter-integrated circuit (I²C) interface is one of the available modes in the serial communication interface (SERCOM).

The I²C interface uses the SERCOM transmitter and receiver configured as shown in Figure 28-1. Labels in capital letters are registers accessible by the CPU, while lowercase labels are internal to the SERCOM. Each master and slave have a separate I²C interface containing a shift register, a transmit buffer and a receive buffer. In addition, the I²C master uses the SERCOM baud-rate generator, while the I²C slave uses the SERCOM address match logic.

Related Links

SERCOM – Serial Communication Interface

28.2 Features

SERCOM I²C includes the following features:

- Master or slave operation
- Can be used with DMA
- Philips I²C compatible
- SMBus™ compatible
- PMBus compatible
- Support of 100kHz and 400kHz, 1MHz and 3.4MHz I²C mode low system clock frequencies
- Physical interface includes:
  - Slew-rate limited outputs
  - Filtered inputs
- Slave operation:
  - Operation in all sleep modes
  - Wake-up on address match
  - 7-bit and 10-bit Address match in hardware for:
  -
    - Unique address and/or 7-bit general call address
    - Address range
    - Two unique addresses can be used with DMA

Related Links

Features

In mono format, Transmit mode, data written to the left channel is duplicated to the right output channel. In mono format, Receiver mode, data received from the right channel is ignored and data received from the left channel is duplicated in to the right channel.

In mono format, TDM Transmit mode with more than two slots, data written to the even-numbered slots is duplicated in to the following odd-numbered slot.

In mono format, TDM Receiver mode with more than two slots, data received from the even-numbered slots is duplicated in to the following odd-numbered slot.

Mono format can be enabled by writing a '1' to the MONO bit in the Serializer m Control register (SERCTRLm.MONO).

I^2S support different data frame formats:

- 2-channel I^2S with Word Select
- 1- to 8-slot Time Division Multiplexed (TDM) with Frame Sync and individually enabled slots
- 1- or 2-channel Pulse Density Modulation (PDM) reception for MEMS microphones
- 1-channel burst transfer with non-periodic Frame Sync

In 2 channel I^2S mode, number of slots configured is one or two and successive data words corresponds to left and right channel. Left and right channel are identified by polarity of Word Select signal (FSn signal). Each frame consists of one or two data word(s). In the case of compact stereo format, the number of slots can be one. When 32-bit slot size is used, the number of slots can be two.

In TDM format, number slots can be configured up to 8 slots. If 4 slots are configured, each frame consists of 4 data words.

In PDM format, continuous 1-bit data samples are available on the SDm line for each SCKn rising and SCKn falling edge as in case of a MEMS microphone with PDM interface.

1-channel burst transfer with non-periodic Frame Sync mode is useful typically for passing control non-auto data as in case of DSP. In Burst mode, a single Data transfer starts at each Frame Sync pulse, and these pulses are 1-bit wide and occur only when a Data transfer is requested.

Sections I2S Format - Reception and Transmission Sequence with Word Select, TDM Format - Reception and Transmission Sequence and I2S Application Examples describe more about frame/data formats and register settings required for different I^2S applications.

enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the I²S is reset. See INTFLAG register for details on how to clear interrupt flags. All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. Refer to *Nested Vector Interrupt Controller* for details. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

29.6.8.3 Events

Not applicable.

29.6.9 Sleep Mode Operation

The I²S continues to operate in all sleep modes that still provide its clocks.

29.6.10 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

When executing an operation that requires synchronization, the corresponding Synchronization Busy bit in the Synchronization Busy register (SYNCBUSY) will be set immediately, and cleared when synchronization is complete.

If an operation that requires synchronization is executed while the corresponding SYNCBUSY bit is '1', a peripheral bus error is generated.

The following bits are synchronized when written:

- Software Reset bit in the Control A register (CTRLA.SWRST). SYNCBUSY.SWRST is set to '1' while synchronization is in progress.
- Enable bit in the Control A register (CTRLA.ENABLE). SYNCBUSY.ENABLE is set to '1' while synchronization is in progress.
- Clock Unit x Enable bits in the Control A register (CTRLA.CKENx). SYNCBUSY.CKENx is set to '1' while synchronization is in progress.
- Serializer x Enable bits in the Control A register (CTRLA.SERENx). SYNCBUSY.SERENx is set to '1' while synchronization is in progress.

The following registers require synchronization when read or written:

- Data n registers (DATAn), Read-Synchronized when Serializer n is in Rx mode or Write-Synchronized when in Tx mode. SYNCBUSY.DATAn is set to '1' while synchronization is in progress.

Synchronization is denoted by the Read-Synchronized or Write-Synchronized property in the register description.

Related Links

Register Synchronization

29.6.11 Loop-Back Mode

For debugging purposes, the I²S can be configured to loop back the Transmitter to the Receiver. Writing a '1' to the Loop-Back Test Mode bit in the Serializer m Control register (SERCTRLm.RXLOOP) configures SDm as input and the remaining SD as output. Both SD will be connected internally, so the transmitted

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the TC is reset. on how to clear interrupt flags.

The TC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller

30.6.4.3 Events

The TC can generate the following output events:

- Overflow/Underflow (OVF)
- Match or Capture (MC)

Writing a '1' to an Event Output bit in the Event Control register (EVCTRL.MCEOx) enables the corresponding output event. The output event is disabled by writing EVCTRL.MCEOx=0.

One of the following event actions can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT):

- Start TC (START)
- Re-trigger TC (RETRIGGER)
- Increment or decrement counter (depends on counter direction)
- Count on event (COUNT)
- Capture Period (PPW and PWP)
- Capture Pulse Width (PW)

Writing a '1' to the TC Event Input bit in the Event Control register (EVCTRL.TCEI) enables input events to the TC. Writing a '0' to this bit disables input events to the TC. The TC requires only asynchronous event inputs. For further details on how configuring the asynchronous events, refer to *EVSYS - Event System*.

Related Links

EVSYS – Event System

30.6.5 Sleep Mode Operation

The TC can be configured to operate in any sleep mode. To be able to run in standby, the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be written to one. The TC can wake up the device using interrupts from any sleep mode or perform actions through the Event System.

30.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in the Control A register (CTRLA.SWRST)

Bit 1 – ERR: Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF: Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

30.8.11 Status

Name: STATUS
Offset: 0x0F
Reset: 0x08
Property: -

Bit	7	6	5	4	3	2	1	0
	SYNCBUSY			SLAVE	STOP			
Access	R			R	R			
Reset	0			0	1			

Bit 7 – SYNCBUSY: Synchronization Busy
This bit is cleared when the synchronization of registers between the clock domains is complete.

This bit is set when the synchronization of registers between clock domains is started.

Bit 4 – SLAVE: Slave Status Flag
This bit is only available in 32-bit mode on the slave TC (i.e., TC1 and/or TC3). The bit is set when the associated master TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 3 – STOP: Stop Status Flag
This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

30.8.12 Counter Value

30.8.12.1 Counter Value, 8-bit Mode

Name: COUNT
Offset: 0x10
Reset: 0x00

The Bank Select flag in EPSTATUS.CURBK indicates which bank data will be used in the next transaction, and is updated after each transaction. According to EPSTATUS.CURBK, EPINTFLAG.TRCPT0 or EPINTFLAG.TRFAIL0 or EPINTFLAG.TRCPT1 or EPINTFLAG.TRFAIL1 in EPINTFLAG and Data Buffer 0/1 ready (EPSTATUS.BK0RDY and EPSTATUS.BK1RDY) are set. The EPSTATUS.DTGLOUT and EPSTATUS.DTGLIN are updated for the enabled endpoint direction only.

32.6.2.12 Feedback Operation

Feedback endpoints are endpoints with same the address but in different directions. This is usually used in explicit feedback mechanism in USB Audio, where a feedback endpoint is associated to one or more isochronous data endpoints to which it provides feedback service. The feedback endpoint always has the opposite direction from the data endpoint.

The feedback endpoint always has the opposite direction from the data endpoint(s). The feedback endpoint has the same endpoint number as the first (lower) data endpoint. A feedback endpoint can be created by configuring an endpoint with different endpoint size (PCKSIZE.SIZE) and different endpoint type (EPCFG.EPTYPE0/1) for the IN and OUT direction.

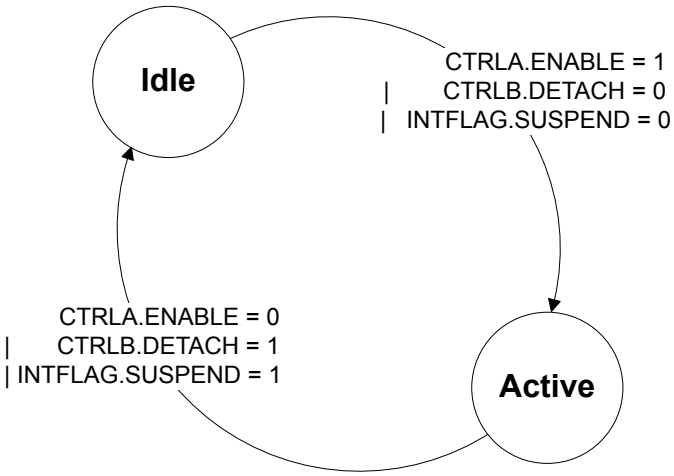
Example Configuration for Feedback Operation:

- Endpoint n / IN: EPCFG.EPTYPE1 = Interrupt IN, PCKSIZE.SIZE = 64.
- Endpoint n / OUT: EPCFG.EPTYPE0= Isochronous OUT, PCKSIZE.SIZE = 512.

32.6.2.13 Suspend State and Pad Behavior

The following figure, Pad Behavior, illustrates the behavior of the USB pad in device mode.

Figure 32-7. Pad Behavior



In Idle state, the pad is in low power consumption mode.

In Active state, the pad is active.

The following figure, Pad Events, illustrates the pad events leading to a PAD state change.

Bit	7	6	5	4	3	2	1	0
							ERRORFLOW	CRCERR
Access							R/W	R/W
Reset							x	x

Bit 1 – ERRORFLOW: Error Flow Status
This bit defines the Error Flow Status.

This bit is set when a Error Flow has been detected during transfer from/towards this bank.

For OUT transfer, a NAK handshake has been sent.

For Isochronous OUT transfer, an overrun condition has occurred.

For IN transfer, this bit is not valid. EPSTATUS.TRFAIL0 and EPSTATUS.TRFAIL1 should reflect the flow errors.

Value	Description
0	No Error Flow detected.
1	A Error Flow has been detected.

Bit 0 – CRCERR: CRC Error
This bit defines the CRC Error Status.

This bit is set when a CRC error has been detected in an isochronous OUT endpoint bank.

0.2.5 Host Registers - Common

Value	Description
0	No CRC Error.
1	CRC Error detected.

32.8.5 Host Registers - Common

32.8.5.1 Control B

Name: CTRLB
Offset: 0x08
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
					L1RESUME	VBUSOK	BUSRESET	SOFE
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
					SPDCONF[1:0]		RESUME	
Access					R/W	R/W	R/W	
Reset					0	0	0	

Bit 11 – L1RESUME: Send USB L1 Resume
Writing 0 to this bit has no effect.
1: Generates a USB L1 Resume on the USB bus. This bit should only be set when the Start-of-Frame

Bit	15	14	13	12	11	10	9	8
					OFFSETCORR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OFFSETCORR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – OFFSETCORR[11:0]: Offset Correction Value
If the CTRLB.CORREN bit is one, these bits define how the ADC conversion result is compensated for offset error before being written to the Result register. This OFFSETCORR value is in two's complement format.

33.8.19 Calibration

Name: CALIB
Offset: 0x28
Reset: 0x0000
Property: Write-Protected

Bit	15	14	13	12	11	10	9	8
						BIAS_CAL[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
	LINEARITY_CAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 10:8 – BIAS_CAL[2:0]: Bias Calibration Value
This value from production test must be loaded from the NVM software calibration area into the CALIB register by software to achieve the specified accuracy.

The value must be copied only, and must not be changed.

Bits 7:0 – LINEARITY_CAL[7:0]: Linearity Calibration Value
This value from production test must be loaded from the NVM software calibration area into the CALIB register by software to achieve the specified accuracy.

The value must be copied only, and must not be changed.

33.8.20 Debug Control

Name: DBGCTRL
Offset: 0x2A
Reset: 0x00
Property: Write-Protected

37. Electrical Characteristics

37.1 Disclaimer

All typical values are measured at T = 25°C unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

37.2 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 37-1. Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Units
V_{DD}	Power supply voltage	0	3.8	V
I_{VDD}	Current into a V_{DD} pin	-	92(1)	mA
I_{GND}	Current out of a GND pin	-	130(1)	mA
V_{PIN}	Pin voltage with respect to GND and V_{DD}	GND-0.6V	V_{DD}+0.6V	V
$T_{storage}$	Storage temperature	-60	150	°C

1. Maximum source current is 46mA and maximum sink current is 65mA per cluster. A cluster is a group of GPIOs as shown in the table below. Also note that each VDD/GND pair is connected to two clusters so current consumption through the pair will be a sum of the clusters source/sink currents.

Caution: This device is sensitive to electrostatic discharges (ESD). Improper handling may lead to permanent performance degradation or malfunctioning.
Handle the device following best practice ESD protection rules: Be aware that the human body can accumulate charges large enough to impair functionality or destroy the device.

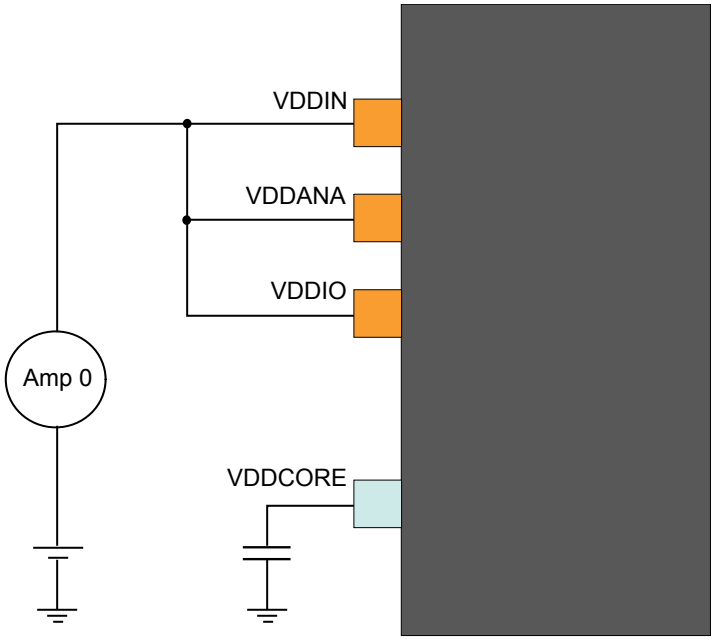
Caution: In debugger cold-plugging mode, NVM erase operations are not protected by the BOD33 and BOD12. NVM erase operation at supply voltages below specified minimum can cause corruption of NVM areas that are mandatory for correct device behavior.

Related Links
GPIO Clusters

37.3 General Operating Ratings

The device must operate within the ratings in order for all other electrical characteristics and typical characteristics of the device to be valid.

Figure 37-1. Measurement Schematic



37.7 Peripheral Power Consumption

Since USB peripheral complies with the Universal Serial Bus (USB) v2.0 standard, USB peripheral power consumption is described a specific section

37.7.1 All peripheral except USB

Default conditions, except where noted:

- Operating conditions
  - V_{VDDIN} = 3.3 V
- Oscillators
  - XOSC (crystal oscillator) stopped
  - XOSC32K (32 kHz crystal oscillator) running with external 32kHz crystal
  - OSC8M at 8MHz
- Clocks
  - OSC8M used as main clock source
  - CPU, AHB and APBn clocks undivided
- The following AHB module clocks are running: NVMCTRL, HPB2 bridge, HPB1 bridge, HPB0 bridge
  - All other AHB clocks stopped
- The following peripheral clocks running: PM, SYSCTRL
  - All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU in IDLE0 mode
- Cache enabled

Table 37-28. Averaging Feature (Device Variant B and C)

Average Number	Conditions	SNR (dB)	SINAD (dB)	SFDR (dB)	ENOB (bits)
1	In differential mode, 1x gain, V_{DDANA}=3.0V, V_{REF}=1.0V, 350kSps at 25°C	66.0	65.0	72.8	10.5
8		67.6	65.8	75.1	10.62
32		69.7	67.1	75.3	10.85
128		70.4	67.5	75.5	10.91

37.10.4.2 Performance with the hardware offset and gain correction

Inherent gain and offset errors affect the absolute accuracy of the ADC. The offset error cancellation is handled by the Offset Correction register (OFFSETCORR) and the gain error cancellation, by the Gain Correction register (GAINCORR). The offset and gain correction value is subtracted from the converted data before writing the Result register (RESULT).

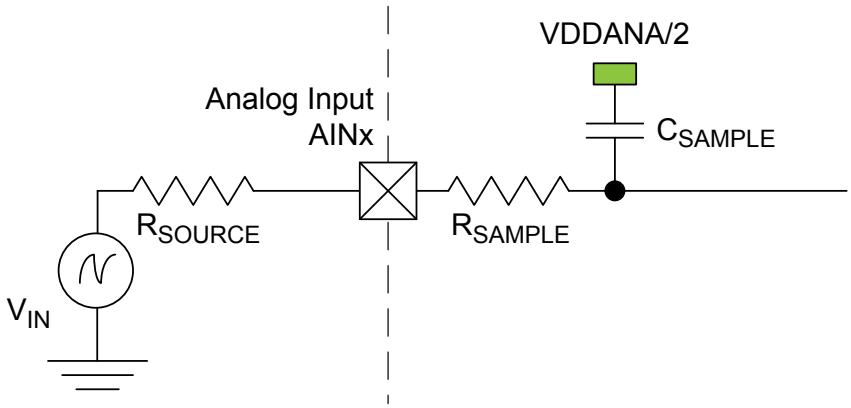
Table 37-29. Offset and Gain correction feature

Gain Factor	Conditions	Offset Error (mV)	Gain Error (mV)	Total Unadjusted Error (LSB)
0.5x	In differential mode, 1x gain, V_{DDANA}=3.0V, V_{REF}=1.0V, 350kSps at 25°C	0.25	1.0	2.4
1x		0.20	0.10	1.5
2x		0.15	-0.15	2.7
8x		-0.05	0.05	3.2
16x		0.10	-0.05	6.1

37.10.4.3 Inputs and Sample and Hold Acquisition Times

The analog voltage source must be able to charge the sample and hold (S/H) capacitor in the ADC in order to achieve maximum accuracy. Seen externally the ADC input consists of a resistor (R_{SAMPLE}) and a capacitor (C_{SAMPLE}). In addition, the source resistance (R_{SOURCE}) must be taken into account when calculating the required sample and hold time. The next figure shows the ADC input channel equivalent circuit.

Figure 37-5. ADC Input



To achieve n bits of accuracy, the C_{SAMPLE} capacitor must be charged at least to a voltage of

40. Errata

40.1 Device Variant A

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

40.1.1 Die Revision A

40.1.1.1 Device

1 – When VDDIN is lower than the POR threshold during power rise or fall, an internal pull-up resistor is enabled on pins with PTC functionality (see PORT Function Multiplexing). Note that this behavior will be present even if PTC functionality is not enabled on the pin. The POR level is defined in the "Power-On Reset (POR) Characteristics" chapter.
Errata reference: 12117
Fix/Workaround:
Use a pin without PTC functionality if the pull-up could damage your application during power up.

2 – In single shot mode and at 125°C, the ADC conversions have linearity errors.
Errata reference: 13277
Fix/Workaround:
- Workaround 1: At 125°C, do not use the ADC in single shot mode; use the ADC in free running mode only.
- Workaround 2: At 125°C, use the ADC in single shot mode only with VDDANA > 3V.

3 – TCC0/WO[6] on PA16 and TCC0/WO[7] on PA17 are not available.
Errata reference: 11622
Fix/Workaround:
None

4 – On pin PA24 and PA25 the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled except for USB.
Errata reference: 12368
Fix/Workaround:
For pin PA24 and PA25, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

5 – If APB clock is stopped and GCLK clock is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, as a consequence debug operation is impossible.
Errata reference: 10416
Fix/Workaround:

2 – The DFLL status bits in the PCLKSR register during the USB clock recovery mode can be wrong after a USB suspend state.
Errata reference: 11938
Fix/Workaround:
Do not monitor the DFLL status bits in the PCLKSR register during the USB clock recovery mode.

3 – If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.
Errata reference: 10669
Fix/Workaround:
Check that the lockbits: DFLLLCKC and DFLLLCKF in the SYSCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

40.1.1.5 XOSC32K

1 – The automatic amplitude control of the XOSC32K does not work.
Errata reference: 10933
Fix/Workaround:
Use the XOSC32K with Automatic Amplitude control disabled (XOSC32K.AAMPEN = 0)

40.1.1.6 FDPLL

1 – The lock flag (DPLLSTATUS.LOCK) may clear randomly. When the lock flag randomly clears, DPLLLCKR and DPLLLCKF interrupts will also trigger, and the DPLL output is masked.
Errata reference: 11791
Fix/Workaround:
Set DPLLCTRLB.LBYPASS to 1 to disable masking of the DPLL output by the lock status.

2 – FDPLL lock time-out values are different from the parameters in the datasheet.
Errata reference: 12145
Fix/Workaround:
The time-out values are:
- DPLLCTRLB.LTIME[2:0] = 4 : 10ms
- DPLLCTRLB.LTIME[2:0] = 5 : 10ms
- DPLLCTRLB.LTIME[2:0] = 6 : 11ms
- DPLLCTRLB.LTIME[2:0] = 7 : 11ms

3 – When changing on-the-fly the FDPLL ratio in DPLLnRATIO register, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.
Errata reference: 15753
Fix/Workaround:
Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

6 – In two ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.
Errata reference: 12224
Fix/Workaround:
None

7 – If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.
Errata reference: 12107
Fix/Workaround:
None

8 – When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.
Errata reference: 12477
Fix/Workaround:
None.

9 – TCC fault filtering on inverted fault is not working.
Errata reference: 12512
Fix/Workaround:
Use only non-inverted faults.

10 – When waking up from the STANDBY power save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to 1.
Errata reference: 12227
Fix/Workaround:
After waking up from STANDBY power save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits

11 – When the Peripheral Access Controller (PAC) protection is enabled, writing to WAVE or WAVEB registers will not cause a hardware exception.
Errata reference: 11468
Fix/Workaround:
None

12 – If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.
Errata reference: 12155
Fix/Workaround:
None

40.1.4.14 PTC

1 – WCOMP interrupt flag is not stable. The WCOMP interrupt flag will not always be set as described in the datasheet.
Errata reference: 12860