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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j15b-aft

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32-bit ARM-Based Microcontrollers

	Pin ⁽¹⁾		I/O Pin	Supply	A		B	(2)(3)			с	D	E	F	G	н
SAMD21E	SAMD21G	SAMD21J			EIC	REF	ADC	AC	РТС	DAC	SERCOM ⁽²⁾⁽³⁾	SERCOM-ALT	тс ⁽⁴⁾ /тсс	тсс	сом	AC/ GCLK
		28	PB15	VDDIO	EXTINT[15]				X[15]		SERCOM4/ PAD[3]		TC5/WO[1]			GCLK_IO[1]
	21	29	PA12	VDDIO	EXTINT[12]						SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TCC2/WO[0]	TCC0/ WO[6]		AC/CMP[0]
	22	30	PA13	VDDIO	EXTINT[13]						SERCOM2/ PAD[1]	SERCOM4/ PAD[1]	TCC2/WO[1]	TCC0/ WO[7]		AC/CMP[1]
15	23	31	PA14	VDDIO	EXTINT[14]						SERCOM2/ PAD[2]	SERCOM4/ PAD[2]	TC3/WO[0]	TCC0/ WO[4]		GCLK_IO[0]
16	24	32	PA15	VDDIO	EXTINT[15]						SERCOM2/ PAD[3]	SERCOM4/ PAD[3]	TC3/WO[1]	TCC0/ WO[5]		GCLK_IO[1]
17	25	35	PA16	VDDIO	EXTINT[0]				X[4]		SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/WO[0]	TCC0/ WO[6]		GCLK_IO[2]
18	26	36	PA17	VDDIO	EXTINT[1]				X[5]		SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/WO[1]	TCC0/ WO[7]		GCLK_IO[3]
19	27	37	PA18	VDDIO	EXTINT[2]				X[6]		SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/ WO[2]		AC/CMP[0]
20	28	38	PA19	VDDIO	EXTINT[3]				X[7]		SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC3/WO[1]	TCC0/ WO[3]	I2S/SD[0]	AC/CMP[1]
		39	PB16	VDDIO	EXTINT[0]						SERCOM5/ PAD[0]		TC6/WO[0]	TCC0/ WO[4]	I2S/SD[1]	GCLK_IO[2]
		40	PB17	VDDIO	EXTINT[1]						SERCOM5/ PAD[1]		TC6/WO[1]	TCC0/ WO[5]	12S/ MCK[0]	GCLK_IO[3]
	29	41	PA20	VDDIO	EXTINT[4]				X[8]		SERCOM5/ PAD[2]	SERCOM3/ PAD[2]	TC7/WO[0]	TCC0/ WO[6]	12S/ SCK[0]	GCLK_IO[4]
	30	42	PA21	VDDIO	EXTINT[5]				X[9]		SERCOM5/ PAD[3]	SERCOM3/ PAD[3]	TC7/WO[1]	TCC0/ WO[7]	I2S/FS[0]	GCLK_IO[5]
21	31	43	PA22	VDDIO	EXTINT[6]				X[10]		SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC4/WO[0]	TCC0/ WO[4]		GCLK_IO[6]
22	32	44	PA23	VDDIO	EXTINT[7]				X[11]		SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC4/WO[1]	TCC0/ WO[5]	USB/SOF 1kHz	GCLK_IO[7]
23	33	45	PA24 ⁽⁶⁾	VDDIO	EXTINT[12]						SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC5/WO[0]	TCC1/ WO[2]	USB/DM	
24	34	46	PA25 ⁽⁶⁾	VDDIO	EXTINT[13]						SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC5/WO[1]	TCC1/ WO[3]	USB/DP	
	37	49	PB22	VDDIO	EXTINT[6]							SERCOM5/ PAD[2]	TC7/WO[0]			GCLK_IO[0]
	38	50	PB23	VDDIO	EXTINT[7]							SERCOM5/ PAD[3]	TC7/WO[1]			GCLK_IO[1]
25	39	51	PA27	VDDIO	EXTINT[15]											GCLK_IO[0]
27	41	53	PA28	VDDIO	EXTINT[8]											GCLK_IO[0]
31	45	57	PA30	VDDIO	EXTINT[10]							SERCOM1/ PAD[2]	TCC1/WO[0]		SWCLK	GCLK_IO[0]
32	46	58	PA31	VDDIO	EXTINT[11]							SERCOM1/ PAD[3]	TCC1/WO[1]		SWDIO ⁽⁵⁾	
		59	PB30	VDDIO	EXTINT[14]							SERCOM5/ PAD[0]	TCC0/WO[0]	TCC1/ WO[2]		
		60	PB31	VDDIO	EXTINT[15]							SERCOM5/ PAD[1]	TCC0/WO[1]	TCC1/ WO[3]		
		61	PB00	VDDANA	EXTINT[0]		AIN[8]		Y[6]			SERCOM5/ PAD[2]	TC7/WO[0]			
		62	PB01	VDDANA	EXTINT[1]		AIN[9]		Y[7]			SERCOM5/ PAD[3]	TC7/WO[1]			
	47	63	PB02	VDDANA	EXTINT[2]		AIN[10]		Y[8]			SERCOM5/ PAD[0]	TC6/WO[0]			
	48	64	PB03	VDDANA	EXTINT[3]		AIN[11]		Y[9]			SERCOM5/ PAD[1]	TC6/WO[1]			

- 1. Use the SAMD21J pinout muxing for WLCSP45 package.
- 2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
- 3. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.

This bit is set when Hot-Plugging is enabled.

This bit is cleared when Hot-Plugging is disabled. This is the case when the SWCLK function is changed. Only a power-reset or a external reset can set it again.

Bits 3,2 – DCCDx: Debug Communication Channel x Dirty [x=1..0]

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when DCCx is written.

This bit is cleared when DCCx is read.

Bit 1 – DBGPRES: Debugger Present

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set when a debugger probe is detected.

This bit is never cleared.

Bit 0 – PROT: Protected

Writing a '0' to this bit has no effect.

Writing a '1' to this bit has no effect.

This bit is set at power-up when the device is protected.

This bit is never cleared.

13.13.4 Address

Name:ADDROffset:0x0004Reset:0x0000000Property:PAC Write-Protection

Bit	31	30	29	28	27	26	25	24	
	ADDR[29:22]								
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	23	22	21	20	19	18	17	16	
				ADDR	[21:14]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	
				ADDF	R[13:6]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	

Writing a one to this bit will clear the OSC8M Ready Interrupt Enable bit, which disables the OSC8M Ready interrupt.

Value	Description
0	The OSC8M Ready interrupt is disabled.
1	The OSC8M Ready interrupt is enabled, and an interrupt request will be generated when the
	OSC8M Ready Interrupt flag is set.

Bit 2 – OSC32KRDY: OSC32K Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the OSC32K Ready Interrupt Enable bit, which disables the OSC32K Ready interrupt.

Value	Description
0	The OSC32K Ready interrupt is disabled.
1	The OSC32K Ready interrupt is enabled, and an interrupt request will be generated when
	the OSC32K Ready Interrupt flag is set.

Bit 1 – XOSC32KRDY: XOSC32K Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the XOSC32K Ready Interrupt Enable bit, which disables the XOSC32K Ready interrupt.

Value	Description
0	The XOSC32K Ready interrupt is disabled.
1	The XOSC32K Ready interrupt is enabled, and an interrupt request will be generated when
	the XOSC32K Ready Interrupt flag is set.

Bit 0 – XOSCRDY: XOSC Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the XOSC Ready Interrupt Enable bit, which disables the XOSC Ready interrupt.

Value	Description
0	The XOSC Ready interrupt is disabled.
1	The XOSC Ready interrupt is enabled, and an interrupt request will be generated when the
	XOSC Ready Interrupt flag is set.

17.8.2 Interrupt Enable Set

Name:	INTENSET
Offset:	0x04
Reset:	0x00000000
Property:	Write-Protected

Bit	31	30	29	28	27	26	25	24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 - MUL[15:0]: DFLL Multiply Factor

This field determines the ratio of the CLK_DFLL output frequency to the CLK_DFLL_REF input frequency. Writing to the MUL bits will cause locks to be lost and the fine calibration value to be reset to its midpoint.

17.8.13 DFLL48M Synchronization

Name:DFLLSYNCOffset:0x30Reset:0x00Property:Write-Protected

Bit	7	6	5	4	3	2	1	0
	READREQ							
Access	W							
Reset	0							

Bit 7 – READREQ: Read Request

To be able to read the current value of DFLLVAL in closed-loop mode, this bit should be written to one. The updated value is available in DFLLVAL when PCLKSR.DFLLRDY is set.

17.8.14 3.3V Brown-Out Detector (BOD33) Control

Name:BOD33Offset:0x34Reset:0x00XX00XXProperty:Write-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					LEVE	L[5:0]		
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			x	x	x	x	x	x
Bit	15	14	13	12	11	10	9	8
		PSEI	_[3:0]				CEN	MODE
Access	R/W	R/W	R/W	R/W			R/W	R/W
Reset	0	0	0	0			0	0
Bit	7	6	5	4	3	2	1	0
		RUNSTDBY		ACTIC	N[1:0]	HYST	ENABLE	
Access		R/W		R/W	R/W	R/W	R/W	
Reset		0		х	х	х	х	

18. WDT – Watchdog Timer

18.1 Overview

The Watchdog Timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is configured to a predefined time-out period, and is constantly running when enabled. If the WDT is not cleared within the time-out period, it will issue a system reset. An early-warning interrupt is available to indicate an upcoming watchdog time-out condition.

The window mode makes it possible to define a time slot (or window) inside the total time-out period during which the WDT must be cleared. If the WDT is cleared outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes the WDT to be cleared frequently.

When enabled, the WDT will run in active mode and all sleep modes. It is asynchronous and runs from a CPU-independent clock source. The WDT will continue operation and issue a system reset or interrupt even if the main clocks fail.

18.2 Features

- Issues a system reset if the Watchdog Timer is not cleared before its time-out period
- Early Warning interrupt generation
- Asynchronous operation from dedicated oscillator
- Two types of operation:
 - Normal mode
 - Window mode
- Selectable time-out periods
 - From 8 cycles to 16,000 cycles in normal mode
 - From 16 cycles to 32,000 cycles in window mode
- Always-on capability

- 5.1. Configure the address match configuration by writing the Address Mode value in the CTRLB register (CTRLB.AMODE).
- 5.2. Set the Address and Address Mask value in the Address register (ADDR.ADDR and ADDR.ADDRMASK) according to the address configuration.

28.6.2.2 Enabling, Disabling, and Resetting

This peripheral is enabled by writing '1' to the Enable bit in the Control A register (CTRLA.ENABLE), and disabled by writing '0' to it.

Refer to CTRLA for details.

28.6.2.3 I²C Bus State Logic

The bus state logic includes several logic blocks that continuously monitor the activity on the l²C bus lines in all sleep modes. The start and stop detectors and the bit counter are all essential in the process of determining the current bus state. The bus state is determined according to Bus State Diagram. Software can get the current bus state by reading the Master Bus State bits in the Status register (STATUS.BUSSTATE). The value of STATUS.BUSSTATE in the figure is shown in binary.

Figure 28-3. Bus State Diagram



The bus state machine is active when the I^2C master is enabled.

After the I²C master has been enabled, the bus state is UNKNOWN (0b00). From the UNKNOWN state, the bus will transition to IDLE (0b01) by either:

- Forcing by by writing 0b01 to STATUS.BUSSTATE
- A stop condition is detected on the bus
- If the inactive bus time-out is configured for SMBus compatibility (CTRLA.INACTOUT) and a timeout occurs.

Note: Once a known bus state is established, the bus state logic will not re-enter the UNKNOWN state.

When the bus is IDLE it is ready for a new transaction. If a start condition is issued on the bus by another I²C master in a multi-master setup, the bus becomes BUSY (0b11). The bus will re-enter IDLE either

Condition	Request			
	DMA	Interrupt	Event	
Data needed for transmit (TX) (Master transmit mode)	Yes (request cleared when data is written)		NA	
Data needed for transmit (RX) (Master transmit mode)	Yes (request cleared when data is read)			
Master on Bus (MB)		Yes		
Stop received (SB)		Yes		
Error (ERROR)		Yes		

28.6.4.1 DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

Slave DMA

When using the I²C slave with DMA, an address match will cause the address interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

28.6.4.2 Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

Error (ERROR)

29.9.7 Serializer n Control

Name:SERCTRLnOffset:0x20 + n*0x04 [n=0..1]Reset:0x00000000Property:Enable-Protected, PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
ſ						RXLOOP	DMA	MONO
Access						R/W	R/W	R/W
Reset						0	0	0
Dit	00	00	04	00	10	40	47	10
BIL	23	22	21	20	19	18	17	10
	SLOTDIS8	SLOTDIS7	SLOTDIS6	SLOTDIS5	SLOTDIS4	SLOTDIS3	SLOTDIS1	SLOTDIS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	٥	8
БК	15	14	15	12	11	10	3	
	BITREV	EXTEN	ND[1:0]	WORDADJ		DATASIZE[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0
5.4	_		_	_				
Bit	1	6	5	4	3	2	1	0
	SLOTADJ		CLKSEL	TXSAME	TXDEFA	TXDEFAULT[1:0] SERMO		DE[1:0]
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit 26 – RXLOOP: Loop-back Test Mode

This bit enables a loop-back test mode:

Value	Description
0	Each Receiver uses its SDn pin as input (default mode).
1	Receiver uses as input the transmitter output of the other Serializer in the pair: e.g. SD1 for
	SD0 or SD0 for SD1.

Bit 25 – DMA: Single or Multiple DMA Channels

This bit selects whether even- and odd-numbered slots use separate DMA channels or the same DMA channel.

DMA	Name	Description
0x0	SINGLE	Single DMA channel
0x1	MULTIPLE	One DMA channel per data channel

Bit 24 – MONO: Mono Mode.

MONO	Name	Description
0x0	STEREO	Normal mode
0x1	MONO	Left channel data is duplicated to right channel

31.6.4.2 Interrupts

The TCC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Retrigger (TRG)
- Count (CNT) refer also to description of EVCTRL.CNTSEL.
- Capture Overflow Error (ERR)
- Debug Fault State (DFS)
- Recoverable Faults (FAULTn)
- Non-recoverable Faults (FAULTx)
- Compare Match or Capture Channels (MCx)

These interrupts are asynchronous wake-up sources. See Sleep Mode Entry and Exit Table in PM/Sleep Mode Controller section for details.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the TCC is reset. See INTFLAG for details on how to clear interrupt flags. The TCC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note: Interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller Sleep Mode Controller IDLE Mode STANDBY Mode

31.6.4.3 Events

The TCC can generate the following output events:

- Overflow/Underflow (OVF)
- Trigger (TRG)
- Counter (CNT) For further details, refer to EVCTRL.CNTSEL description.
- Compare Match or Capture on compare/capture channels: MCx

Writing a '1' ('0') to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables (disables) the corresponding output event. Refer also to *EVSYS – Event System*.

The TCC can take the following actions on a channel input event (MCx):

- Capture event
- Generate a recoverable or non-recoverable fault

The TCC can take the following actions on counter Event 1 (TCCx EV1):

- Counter re-trigger
- Counter direction control
- Stop the counter

Name: CTRLA

- Offset: 0x00
- Reset: 0x0000000

Property: PAC Write-Protection, Enable-Protected, Write-Synchronized (ENABLE, SWRST)

Bit	31	30	29	28	27	26	25	24
					CPTEN3	CPTEN2	CPTEN1	CPTEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
		ALOCK	PRESCY	YNC[1:0]	RUNSTDBY	F	PRESCALER[2:0]
		ALCON						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Access Reset		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
Access Reset		R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0	R/W 0
Access Reset Bit	7	R/W 0 6	R/W 0 5	R/W 0 4	R/W 0 3	R/W 0 2	R/W 0 1	R/W 0 0
Access Reset Bit	7	R/W 0 6 RESOLU	R/W 0 5 TION[1:0]	R/W 0 4	R/W 0 3	R/W 0 2	R/W 0 1 ENABLE	R/W 0 0 SWRST
Access Reset Bit Access	7	R/W 0 6 RESOLU R/W	R/W 0 5 TION[1:0] R/W	R/W 0 4	R/W 0 3	R/W 0 2	R/W 0 1 ENABLE R/W	R/W 0 0 SWRST R/W
Access Reset Bit Access Reset	7	R/W 0 6 RESOLU R/W 0	R/W 0 5 TION[1:0] R/W 0	R/W 0 4	R/W 0 3	R/W 0 2	R/W 0 1 ENABLE R/W 0	R/W 0 0 SWRST R/W 0

Bits 24, 25, 26, 27 – CPTEN0, CPTEN1, CPTEN2, CPTEN3: Capture Channel x Enable

These bits are used to select the capture or compare operation on channel x.

Writing a '1' to CPTENx enables capture on channel x.

Writing a '0' to CPTENx disables capture on channel x.

Bit 14 – ALOCK: Auto Lock

This bit is not synchronized.

Value	Description
0	The Lock Update bit in the Control B register (CTRLB.LUPD) is not affected by overflow/
	underflow, and re-trigger events
1	CTRLB.LUPD is set to '1' on each overflow/underflow or re-trigger event.

Bits 13:12 – PRESCYNC[1:0]: Prescaler and Counter Synchronization

These bits select if on re-trigger event, the Counter is cleared or reloaded on either the next GCLK_TCCx clock, or on the next prescaled GCLK_TCCx clock. It is also possible to reset the prescaler on re-trigger event.

These bits are not synchronized.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on
	channel x.

Bits 19,18,17,16 – MCEIx: Match or Capture Channel x Event Input Enable

These bits indicate if the Match/capture x incoming event is enabled

These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 15,14 – TCEIx: Timer/Counter Event Input x Enable

This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 13,12 – TCINVx: Timer/Counter Event x Invert Enable

This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.
1	Input event source x is inverted.

Bit 10 – CNTEO: Timer/Counter Event Output Enable

This bit is used to enable the counter cycle event. When enabled, an event will be generated on begin or end of counter cycle depending of CNTSEL[1:0] settings.

Value	Description
0	Counter cycle output event is disabled and will not be generated.
1	Counter cycle output event is enabled and will be generated depend of CNTSEL[1:0] value.

Bit 9 – TRGEO: Retrigger Event Output Enable

This bit is used to enable the counter retrigger event. When enabled, an event will be generated when the counter retriggers operation.

Value	Description
0	Counter retrigger event is disabled and will not be generated.
1	Counter retrigger event is enabled and will be generated for every counter retrigger.

Bit 8 – OVFEO: Overflow/Underflow Event Output Enable

This bit is used to enable the overflow/underflow event. When enabled an event will be generated when the counter reaches the TOP or the ZERO value.

Value	Description
0	Overflow/underflow counter event is disabled and will not be generated.
1	Overflow/underflow counter event is enabled and will be generated for every counter
	overflow/underflow.

Offset: 0x28 Reset: 0x00000000 Property: PAC Write-Protection



Bits 19,18,17,16 – MCx: Match or Capture Channel x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bits 15,14 – FAULTx: Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Non-Recoverable Fault x Interrupt Disable/Enable bit, which enables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB: Recoverable Fault B Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Recoverable Fault B Interrupt Disable/Enable bit, which enables the Recoverable Fault B interrupt.

Bit	7	6	5	4	3	2	1	0

```
Access
```

Reset

Bit 31 – AUTO_ZLP: Automatic Zero Length Packet

This bit defines the automatic Zero Length Packet mode of the pipe.

When enabled, the USB module will manage the ZLP handshake by hardware. This bit is for OUT pipes only. When disabled the handshake should be managed by firmware.

Value	Description
0	Automatic Zero Length Packet is disabled.
1	Automatic Zero Length Packet is enabled.

Bits 30:28 – SIZE[2:0]: Pipe size

These bits contains the size of the pipe.

Theses bits are cleared upon sending a USB reset.

SIZE[2:0]	Description
0x0	8 Byte
0x1	16 Byte
0x2	32 Byte
0x3	64 Byte
0x4	128 Byte ⁽¹⁾
0x5	256 Byte ⁽¹⁾
0x6	512 Byte ⁽¹⁾
0x7	1024 Byte in HS mode ⁽¹⁾ 1023 Byte in FS mode ⁽¹⁾

1. For Isochronous pipe only.

Bits 27:14 – MULTI_PACKET_SIZE[13:0]: Multi Packet IN or OUT size

These bits define the 14-bit value that is used for multi-packet transfers.

For IN pipes, MULTI_PACKET_SIZE holds the total number of bytes sent. MULTI_PACKET_SIZE should be written to zero when setting up a new transfer.

For OUT pipes, MULTI_PACKET_SIZE holds the total data size for the complete transfer. This value must be a multiple of the maximum packet size.

Bits 13:8 – BYTE_COUNT[5:0]: Byte Count

These bits define the 14-bit value that contains number of bytes sent in the last OUT or SETUP transaction for an OUT pipe, or of the number of bytes to be received in the next IN transaction for an input pipe.

32.8.7.4 Extended Register

Name: EXTREG

Value	Description
0	The ADC is halted during standby sleep mode.
1	The ADC continues normal operation during standby sleep mode.

Bit 1 – ENABLE: Enable

Due to synchronization, there is a delay from writing CTRLA.ENABLE until the peripheral is enabled/ disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY) will be set. STATUS.SYNCBUSY will be cleared when the operation is complete.

Value	Description
0	The ADC is disabled.
1	The ADC is enabled.

Bit 0 – SWRST: Software Reset

Writing a zero to this bit has no effect.

Writing a one to this bit resets all registers in the ADC, except DBGCTRL, to their initial state, and the ADC will be disabled.

Writing a one to CTRL.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and STATUS.SYNCBUSY will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

33.8.2 Reference Control

Name: REFCTRL Offset: 0x01 Reset: 0x00 Property: Write-Protected

Bit	7	6	5	4	3	2	1	0
	REFCOMP					REFSI	EL[3:0]	
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – REFCOMP: Reference Buffer Offset Compensation Enable

The accuracy of the gain stage can be increased by enabling the reference buffer offset compensation. This will decrease the input impedance and thus increase the start-up time of the reference.

Value	Description
0	Reference buffer offset compensation is disabled.
1	Reference buffer offset compensation is enabled.

Bits 3:0 – REFSEL[3:0]: Reference Selection

These bits select the reference for the ADC.



During sleep modes, filtering is supported only for single-shot measurements. Filtering must be disabled if continuous measurements will be done during sleep modes, or the resulting interrupt/event may be generated incorrectly.

34.6.10 Comparator Output

The output of each comparator can be routed to an I/O pin by setting the Output bit group in the Comparator Control x register (COMPCTRLx.OUT). This allows the comparator to be used by external circuitry. Either the raw, non-synchronized output of the comparator or the CLK_AC-synchronized version, including filtering, can be used as the I/O signal source. The output appears on the corresponding CMP[x] pin.

34.6.11 Offset Compensation

The Swap bit in the Comparator Control registers (COMPCTRLx.SWAP) controls switching of the input signals to a comparator's positive and negative terminals. When the comparator terminals are swapped, the output signal from the comparator is also inverted, as shown in Figure 34-8. This allows the user to measure or compensate for the comparator input offset voltage. As part of the input selection, COMPCTRLx.SWAP can be changed only while the comparator is disabled.





34.6.12 Interrupts

The AC has the following interrupt sources:

Bit 19 – HYST: Hysteresis Enable

This bit indicates the hysteresis mode of comparator n. Hysteresis is available only for continuous mode (COMPCTRLn. SINGLE=0). COMPCTRLn.HYST can be written only while COMPCTRLn.ENABLE is zero.

This bit is not synchronized.

These bits are not synchronized.

Value	Name
0	Hysteresis is disabled.
1	Hysteresis is enabled.

Bits 17:16 – OUT[1:0]: Output

These bits configure the output selection for comparator n. COMPCTRLn.OUT can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	OFF	The output of COMPn is not routed to the COMPn I/O port
0x1	ASYNC	The asynchronous output of COMPn is routed to the COMPn I/O port
0x2	SYNC	The synchronous output (including filtering) of COMPn is routed to the COMPn I/O port
0x3	N/A	Reserved

Bit 15 – SWAP: Swap Inputs and Invert

This bit swaps the positive and negative inputs to COMPn and inverts the output. This function can be used for offset cancellation. COMPCTRLn.SWAP can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Description	
0	The output of MUXPOS connects to the positive input, and the output of MUXNEG connects	
	to the negative input.	
1	The output of MUXNEG connects to the positive input, and the output of MUXPOS connects	
	to the negative input.	

Bits 13:12 – MUXPOS[1:0]: Positive Input Mux Selection

These bits select which input will be connected to the positive input of comparator n. COMPCTRLn.MUXPOS can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3

Bits 10:8 – MUXNEG[2:0]: Negative Input Mux Selection

These bits select which input will be connected to the negative input of comparator n. COMPCTRLn.MUXNEG can only be written while COMPCTRLn.ENABLE is zero.

if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_PREC; SERCOM - INTFLAG.reg = SERCOM I2CS INTFLAG AMATCH;

7 – PA24 and PA25 cannot be used as input when configured as GPIO with continuous sampling (cannot be read by PORT). Errata reference: 12005

Fix/Workaround:

- Use PA24 and PA25 for peripherals or only as output pins.

- Or configure PA31 to PA24 for on-demand sampling (CTRL[31:24] all zeroes) and access the IN register through the APB (not the IOBUS), to allow waiting for on-demand sampling.

8 – The SYSTICK calibration value is incorrect. Errata reference: 14154 Fix/Workaround:

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the Systick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

9 – In Standby, Idle1 and Idle2 sleep modes the device might not wake up from sleep. An External Reset, Power on Reset or Watch Dog Reset will start the device again.

Errata reference: 13140

Fix/Workaround:

the SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20uA compared to numbers in the electrical characteristics chapter.

10 – While the internal startup is not completed, PA07 pin is driven low by the chip. Then as all the other pins it is configured as an High Impedance pin.

Errata reference: 12118 Fix/Workaround: None

11 – Digital pin outputs from Timer/Counters, AC (Analog Comparator), GCLK (Generic Clock Controller), and SERCOM (I2C and SPI) do not change value during standby sleep mode.

Errata reference: 12537

Fix/Workaround:

Set the voltage regulator in Normal mode before entering STANDBY sleep mode in order to keep digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

12 – The I2S is non-functional. Errata reference: 12275 Fix/Workaround: None

13 – Pulldown functionality is not available on GPIO pin PA24 and PA25 Errata reference: 13883

Errata reference: 12368

Fix/Workaround:

For pin PA24 and PA25, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

5 – If APB clock is stopped and GCLK clock is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, as a consequence debug operation is impossible.

Errata reference: 10416

Fix/Workaround:

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

6 – In I2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

Errata reference: 13574

Fix/Workaround:

Write CTRLB.ACKACT to 0 using the following sequence:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = 0;

// Re-enable interrupts if applicable.

Write CTRLB.ACKACT to 1 using the following sequence:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit

position.

Code replacements examples:

Current:

SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;

Change to:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Current:

SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;

Change to:

// If higher priority interrupts exist, then disable so that the

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

5 – In I2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.

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// following two writes are atomic.

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SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit position.

Code replacements examples:

Current:

SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;

Change to:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;

// Re-enable interrupts if applicable.

Current:

SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT; Change to:

// If higher priority interrupts exist, then disable so that the

// following two writes are atomic.

SERCOM - STATUS.reg = 0;

SERCOM - CTRLB.reg = 0;

// Re-enable interrupts if applicable.

Current:

/* ACK or NACK address */

SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);

Change to:

// CMD=0x3 clears all interrupts, so to keep the result similar,

// PREC is cleared if it was set.

43.12 Rev. E - 02/2015

Description:			
	CoreMark score updated from 2.14 to 2.46 CoreMark/MHz.		
Ordering Info	Ordering Information:		
	Added Ordering codes for Device Variant B. Added 125°C ordering codes for QFN and TQFP package options: SAM D21E, SAM D21G and SAM D21J.		
	Added WLCSP package option for SAM D21G.		
	Added UFBGA package option for SAM D21J.		
Pinout:			
	Added pinout figures for UFBGA64 and WLCSP45.		
Product Mapping:			
	Updated Product Mapping figure with Internal RWW section block for Device Variant B.		
Memories:			
	Physical Memory Map: Added start address for Internal Read While Write (RWW) section for Device Variant B.		
Processor And Architecture:			
	Cortex M0+ Configuration: Removed green connection dots between DMAC Data and AHB-APB Bridge A and Bridge B.		
NVMCTRL -	- Non-Volatile Memory Controller:		
	Introducing Read While Write (RWW) feature for Device Variant B. Updated and New sections:		
	Overview		
	Features		
	Block Diagram		
	NVM Read		
	RWWEE Read		
	NVM Write		
	Erase Row		
	Memory Organization: Figure 22-2 updated.		
	Register Summary and Register Description: PARAM: Added RWWEEP[12:0] bits for Device Variant B.		
PORT - I/O I	Pin Controller:		