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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j15b-aut

2. Clock representation must be selected by writing the Clock Representation bit in the Control register (CTRL.CLKREP)
3. Prescaler value must be selected by writing the Prescaler bit group in the Control register (CTRL.PRESCALER)

The RTC prescaler divides the source clock for the RTC counter.
Note: In Clock/Calendar mode, the prescaler must be configured to provide a 1Hz clock to the counter for correct operation.

The frequency of the RTC clock (CLK_RTC_CNT) is given by the following formula:

$$f_{\mathrm{CLK\_RTC\_CNT}} = \frac{f_{\mathrm{GCLK\_RTC}}}{2^{\mathrm{PRESCALER}}}$$

The frequency of the generic clock, GCLK_RTC, is given by f_{GCLK_RTC}, and $f_{CLK\_RTC\_CNT}$ is the frequency of the internal prescaled RTC clock, CLK_RTC_CNT.

19.6.2.2 Enabling, Disabling and Resetting

The RTC is enabled by setting the Enable bit in the Control register (CTRL.ENABLE=1). The RTC is disabled by writing CTRL.ENABLE=0.

The RTC is reset by setting the Software Reset bit in the Control register (CTRL.SWRST=1). All registers in the RTC, except DEBUG, will be reset to their initial state, and the RTC will be disabled. The RTC must be disabled before resetting it.

19.6.3 Operating Modes

The RTC counter supports three RTC operating modes: 32-bit Counter, 16-bit Counter and Clock/ Calendar. The operating mode is selected by writing to the Operating Mode bit group in the Control register (CTRL.MODE).

19.6.3.1 32-Bit Counter (Mode 0)

When the RTC Operating Mode bits in the Control register are zero (CTRL.MODE=00), the counter operates in 32-bit Counter mode. The block diagram of this mode is shown in Figure 19-1. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The counter will increment until it reaches the top value of 0xFFFFFFFF, and then wrap to 0x00000000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 32-bit format.

The counter value is continuously compared with the 32-bit Compare register (COMP0). When a compare match occurs, the Compare 0interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMP0) is set on the next 0-to-1 transition of CLK_RTC_CNT.

If the Clear on Match bit in the Control register (CTRL.MATCHCLR) is '1', the counter is cleared on the next counter cycle when a compare match with COMP0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than are possible with the prescaler events. Note that when CTRL.MATCHCLR is '1', INTFLAG.CMP0 and INTFLAG.OVF will both be set simultaneously on a compare match with COMP0.

19.6.3.2 16-Bit Counter (Mode 1)

When the RTC Operating Mode bits in the Control register (CTRL.MODE) are 1, the counter operates in 16-bit Counter mode as shown in Figure 19-2. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. In 16-bit Counter mode, the 16-bit Period register (PER) holds the maximum value of the counter. The counter will increment until it reaches the PER value, and then

wrap to 0x0000. This sets the Overflow interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 16-bit format.

The counter value is continuously compared with the 16-bit Compare registers (COMPn, n=0–1). When a compare match occurs, the Compare n interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn, n=0–1) is set on the next 0-to-1 transition of CLK_RTC_CNT.

19.6.3.3 Clock/Calendar (Mode 2)

When CTRL.MODE is two, the counter operates in Clock/Calendar mode, as shown in Figure 19-3. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The selected clock source and RTC prescaler must be configured to provide a 1Hz clock to the counter for correct operation in this mode.

The time and date can be read from or written to the Clock Value register (CLOCK) in a 32-bit time/date format. Time is represented as:

- Seconds
- Minutes
- Hours

Hours can be represented in either 12- or 24-hour format, selected by the Clock Representation bit in the Control register (CTRL.CLKREP). This bit can be changed only while the RTC is disabled.

Date is represented as:

- Day as the numeric day of the month (starting at 1)
- Month as the numeric month of the year (1 = January, 2 = February, etc.)
- Year as a value counting the offset from a reference value that must be defined in software

The date is automatically adjusted for leap years, assuming every year divisible by 4 is a leap year. Therefore, the reference value must be a leap year, e.g. 2000. The RTC will increment until it reaches the top value of 23:59:59 December 31st of year 63, and then wrap to 00:00:00 January 1st of year 0. This will set the Overflow interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.OVF).

The clock value is continuously compared with the 32-bit Alarm register (ALARM0). When an alarm match occurs, the Alarm 0 Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.ALARMn0) is set on the next 0-to-1 transition of CLK_RTC_CNT. E.g. For a 1Hz clock counter, it means the Alarm 0 Interrupt flag is set with a delay of 1s after the occurrence of alarm match. A valid alarm match depends on the setting of the Alarm Mask Selection bits in the Alarm

A valid alarm match depends on the setting of the Alarm Mask Selection bits in the Alarm 0 Mask register (MASK0.SEL). These bits determine which time/date fields of the clock and alarm values are valid for comparison and which are ignored.

If the Clear on Match bit in the Control register (CTRL.MATCHCLR) is one, the counter is cleared on the next counter cycle when an alarm match with ALARM0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than are possible with the prescaler events (see Periodic Events). Note that when CTRL.MATCHCLR is '1', INTFLAG.ALARM0 and INTFLAG.OVF will both be set simultaneously on an alarm match with ALARM0.

19.6.4 DMA Operation

Not applicable.

Offset	Name	Bit Pos.									
0x18	ALARM0	7:0	MINUTE[1:0]		SECOND[5:0]						
0x19		15:8	HOUR[3:0]				MINUTE[5:2]				
0x1A		23:16	MONTH[1:0]		DAY[4:0]					HOUR[4]	
0x1B		31:24	YEAR[5:0]						MONTH[3:2]		
0x1C	MASK	7:0						SEL[2:0]			

19.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

19.8.1 Control - MODE0

Name: CTRL
Offset: 0x00
Reset: 0x0000
Property: Enable-Protected, Write-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
					PRESCALER[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MATCHCLR				MODE[1:0]		ENABLE	SWRST
Access	R/W				R/W	R/W	R/W	W
Reset	0				0	0	0	0

Bits 11:8 – PRESCALER[3:0]: Prescaler
These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT).

These bits are not synchronized.

PRESCALER[3:0]	Name	Description
0x0	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV2	CLK_RTC_CNT = GCLK_RTC/2

CMD[6:0]	Group Configuration	Description
0x05	EAR	Erase Auxiliary Row - Erases the auxiliary row addressed by the ADDR register. This command can be given only when the security bit is not set and only to the User Configuration Row.
0x06	WAP	Write Auxiliary Page - Writes the contents of the page buffer to the page addressed by the ADDR register. This command can be given only when the security bit is not set and only to the User Configuration Row.
0x07-0x0E	-	Reserved
0x0F	WL	Write Lockbits- write the LOCK register
0x1A-0x19	-	Reserved
0x1A	RWWEEER	RWWEE Erase Row - Erases the row addressed by the ADDR register in the RWWEE array.
0x1B	-	Reserved
0x1C	RWWEEWP	RWWEE Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register in the RWWEE array.
0x1D-0x3F	-	Reserved
0x40	LR	Lock Region - Locks the region containing the address location in the ADDR register.
0x41	UR	Unlock Region - Unlocks the region containing the address location in the ADDR register.
0x42	SPRM	Sets the Power Reduction Mode.
0x43	CPRM	Clears the Power Reduction Mode.
0x44	PBC	Page Buffer Clear - Clears the page buffer.
0x45	SSB	Set Security Bit - Sets the security bit by writing 0x00 to the first byte in the lockbit row.
0x46	INVALL	Invalidates all cache lines.
0x47	LDR	Lock Data Region - Locks the data region containing the address location in the ADDR register. When the Security Extension is enabled, only secure access can lock secure regions.
0x48	UDR	Unlock Data Region - Unlocks the data region containing the address location in the ADDR register. When the Security Extension is enabled, only secure access can unlock secure regions.
0x47-0x7F	-	Reserved

22.8.2 Control B

Bit	7	6	5	4	3	2	1	0
	SAMPLING[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SAMPLING[31:0]: Input Sampling Mode
Configures the input sampling functionality of the I/O pin input samplers, for pins configured as inputs via the Data Direction register (DIR).

The input samplers are enabled and disabled in sub-groups of eight. Thus if any pins within a byte request continuous sampling, all pins in that eight pin sub-group will be continuously sampled.

Value	Description
0	The I/O pin input synchronizer is disabled.
1	The I/O pin input synchronizer is enabled.

23.8.11 Write Configuration

This write-only register is used to configure several pins simultaneously with the same configuration and/or peripheral multiplexing.

In order to avoid side effect of non-atomic access, 8-bit or 16-bit writes to this register will have no effect. Reading this register always returns zero.

Name: WRCONFIG
Offset: 0x28
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	HWSEL	WRPINCFG		WRPMUX	PMUX[3:0]			
Access	W	W		W	W	W	W	W
Reset	0	0		0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		DRVSTR				PULLEN	INEN	PMUXEN
Access		W				W	W	W
Reset		0				0	0	0

Bit	15	14	13	12	11	10	9	8
	PINMASK[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PINMASK[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 31 – HWSEL: Half-Word Select
This bit selects the half-word field of a 32-PORT group to be reconfigured in the atomic write operation.

This bit will always read as zero.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if the received character had a frame error, i.e., when the first stop bit is zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 0 – PERR: Parity Error
Reading this bit before reading the Data register will indicate the error status of the next character to be read.

This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set if parity checking is enabled (CTRLA.FORM is 0x1, 0x5) and a parity error is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

26.8.9 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

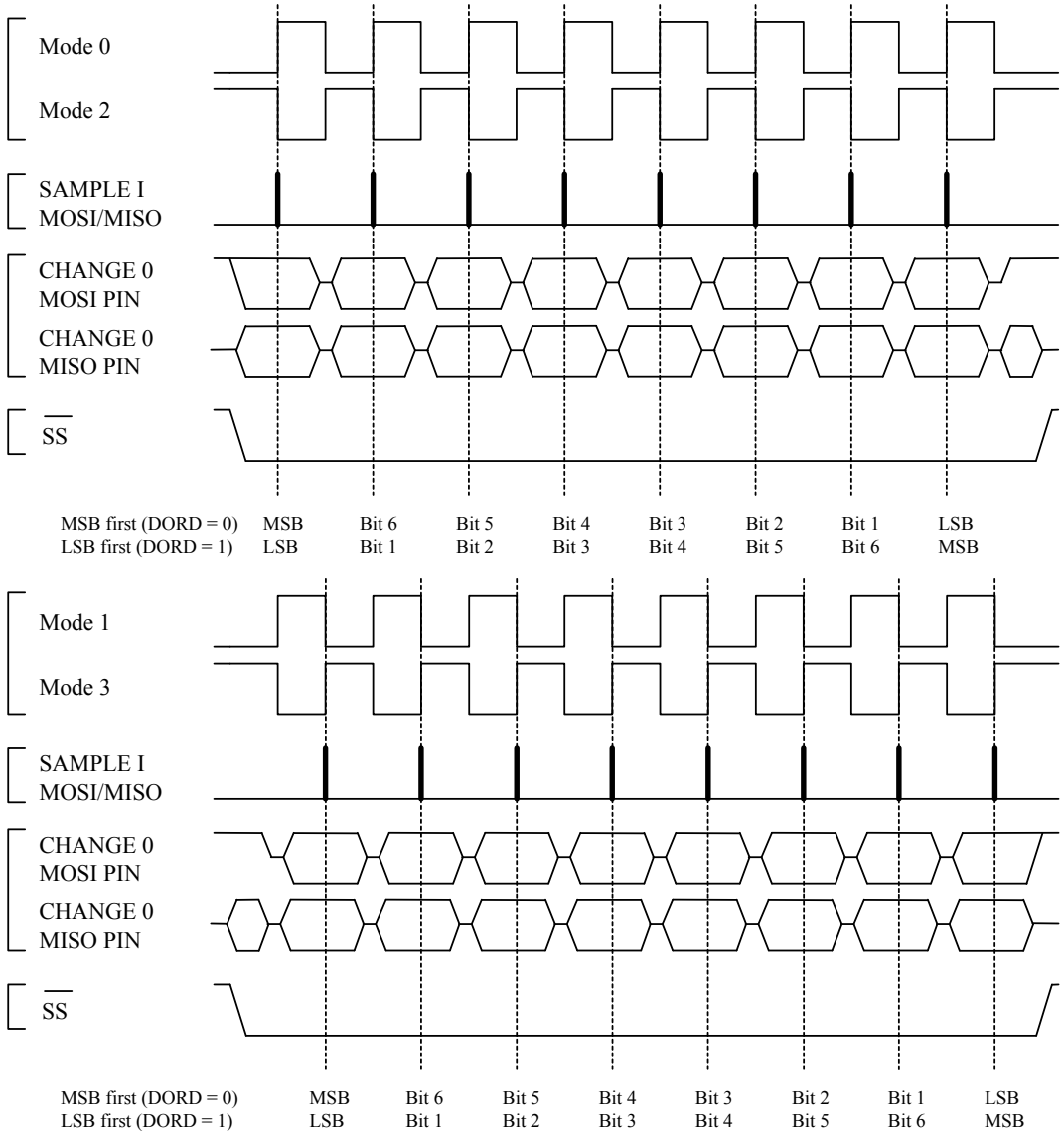
Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						CTRLB	ENABLE	SWRST
Access						R	R	R
Reset						0	0	0

Bit 2 – CTRLB: CTRLB Synchronization Busy
Writing to the CTRLB register when the SERCOM is enabled requires synchronization. When writing to CTRLB the SYNCBUSY.CTRLB bit will be set until synchronization is complete. If CTRLB is written while SYNCBUSY.CTRLB is asserted, an APB error will be generated.

Figure 27-3. SPI Transfer Modes



27.6.2.6 Transferring Data

Master

In master mode (CTRLA.MODE=0x3), when Master Slave Enable Select (CTRLB.MSSEN) is ‘1’, hardware will control the $\overline{SS}$ line.

When Master Slave Select Enable (CTRLB.MSSEN) is '0', the $\overline{SS}$ line must be configured as an output. $\overline{SS}$ can be assigned to any general purpose I/O pin. When the SPI is ready for a data transaction, software must pull the $\overline{SS}$ line low.

When writing a character to the Data register (DATA), the character will be transferred to the shift register. Once the content of TxDATA has been transferred to the shift register, the Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) will be set. And a new character can be written to DATA.

Each time one character is shifted out from the master, another character will be shifted in from the slave simultaneously. If the receiver is enabled (CTRLA.RXEN=1), the contents of the shift register will be transferred to the two-level receive buffer. The transfer takes place in the same clock cycle as the last

arbitration is lost during the transmission. In this case, a lost arbitration will prevent setting INTFLAG.SB. Instead, INTFLAG.MB will indicate a change in arbitration. Handling of lost arbitration is the same as for data bit transmission.

Receiving Data Packets (SCLSM=1)

When INTFLAG.SB is set, the I^2C master will already have received one data packet and transmitted an ACK or NACK, depending on CTRLB.ACKACT. At this point, CTRLB.ACKACT must be set to the correct value for the next ACK bit, and the transaction can continue by reading DATA and issuing a command if not in the smart mode.

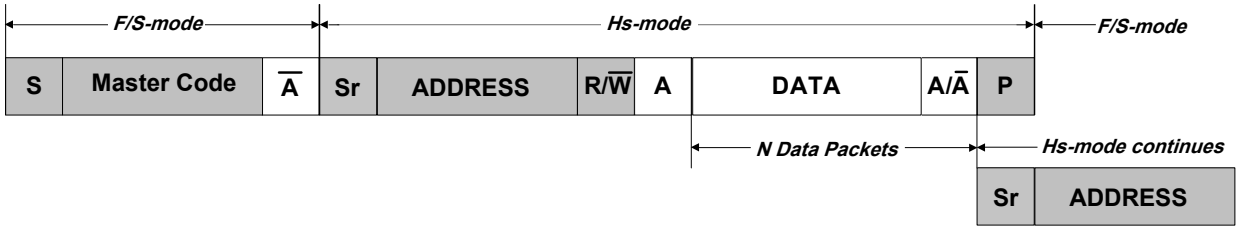
High-Speed Mode

High-speed transfers are a multi-step process, see High Speed Transfer.

First, a master code (0b00001nnn, where 'nnn' is a unique master code) is transmitted in Full-speed mode, followed by a NACK since no slaveshould acknowledge. Arbitration is performed only during the Full-speed Master Code phase. The master code is transmitted by writing the master code to the address register (ADDR.ADDR) and writing the high-speed bit (ADDR.HS) to '0'.

After the master code and NACK have been transmitted, the master write interrupt will be asserted. In the meanwhile, the slave address can be written to the ADDR.ADDR register together with ADDR.HS=1. Now in High-speed mode, the master will generate a repeated start, followed by the slave address with RW-direction. The bus will remain in High-speed mode until a stop is generated. If a repeated start is desired, the ADDR.HS bit must again be written to '1', along with the new address ADDR.ADDR to be transmitted.

Figure 28-7. High Speed Transfer



Transmitting in High-speed mode requires the I^2C master to be configured in High-speed mode (CTRLA.SPEED=0x2) and the SCL clock stretch mode (CTRLA.SCLSM) bit set to '1'.

10-Bit Addressing

When 10-bit addressing is enabled by the Ten Bit Addressing Enable bit in the Address register (ADDR.TENBITEN=1) and the Address bit field ADDR.ADDR is written, the two address bytes will be transmitted, see 10-bit Address Transmission for a Read Transaction. The addressed slave acknowledges the two address bytes, and the transaction continues. Regardless of whether the transaction is a read or write, the master must start by sending the 10-bit address with the direction bit (ADDR.ADDR[0]) being zero.

If the master receives a NACK after the first byte, the write interrupt flag will be raised and the STATUS.RXNACK bit will be set. If the first byte is acknowledged by one or more slaves, then the master will proceed to transmit the second address byte and the master will first see the write interrupt flag after the second byte is transmitted. If the transaction direction is read-from-slave, the 10-bit address transmission must be followed by a repeated start and the first 7 bits of the address with the read/write bit equal to '1'.

29.4 Signal Description

Table 29-1. Master Mode

Pin Name	Pin Description	Type
MCKn	Master Clock for Clock Unit n	Input/Output
SCKn	Serial Clock for Clock Unit n	Input/Output
FSn	I^2S Word Select or TDM Frame Sync for Clock Unit n	Input/Output
SDm	Serial Data Input or Output for Serializer m	Input/Output

Table 29-2. Slave Mode

Pin Name	Pin Description	Type
MCKn	Master Clock	Input
SCKn	Serial Clock for Clock Unit n	Input
FSn	I^2S Word Select or TDM Frame Sync	Input
SDm	Serial Data Input or Output for Serializer m	Input/Output

Table 29-3. Controller Mode

Pin Name	Pin Description	Type
MCKn	Master Clock for Clock Unit n	Output
SCKn	Serial Clock for Clock Unit n	Output
FSn	I^2S Word Select or TDM Frame Sync	Output
SDm	Not Applicable	Not Applicable

Note: One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations

29.5 Product Dependencies

In order to use this module, other parts of the system must be configured correctly, as described below.

29.5.1 I/O Lines

Using the I^2S I/O lines requires the I/O pins to be configured.

The I^2S pins may be multiplexed with I/O Controller lines. The user must first program the I/O Controller to assign the desired I^2S pins to their peripheral function. If the I^2S I/O lines are not used by the application, they can be used for other purposes by the I/O Controller. It is required to enable only the I^2S inputs and outputs actually in use.

Related Links

PORT - I/O Pin Controller

Value	Description
0	The Receive Ready interrupt is disabled.
1	The Receive Ready interrupt is enabled.

29.9.5 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x14
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
			TXUR1	TXUR0			TXRDY1	TXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
			RXOR1	RXOR0			RXRDY1	RXRDY0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 13,12 – TXURx : Transmit Underrun x [x=1..0]
This flag is cleared by writing a '1' to it.

This flag is set when a Transmit Underrun condition occurs in Sequencer x, and will generate an interrupt request if INTENCLR/SET.TXURx is set to '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Underrun x interrupt flag.

Bits 9,8 – TXRDYx : Transmit Ready x [x=1..0]
This flag is cleared by writing to DATAx register or writing a '1' to it.

This flag is set when Sequencer x is ready to accept a new data word to be transmitted, and will generate an interrupt request if INTENCLR/SET.TXRDYx is set to '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Transmit Ready x interrupt flag.

Bits 4,5 – RXORx : Receive Overrun x [x=1..0]
This flag is cleared by writing a '1' to it.

This flag is set when a Receive Overrun condition occurs in Sequencer x, and will generate an interrupt request if INTENCLR/SET.RXORx is set to '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Receive Overrun x interrupt flag.

Bits 1,0 – RXRDYx : Receive Ready x [x=1..0]
This flag is cleared by reading from DATAx register or writing a '1' to it.

Bits 23,22,21,20,18,19,18,17,16 – SLOTDISx : Slot x Disabled for this Serializer [x=7..0]
This field allows disabling some slots in each transmit frame:

Value	Description
0	Slot x is used for data transfer.
1	Slot x is not used for data transfer and will be output as specified in the TXDEFAULT field.

Bit 15 – BITREV: Data Formatting Bit Reverse
This bit allows changing the order of data bits in the word in the Formatting Unit.

BITREV	Name	Description
0x0	MSBIT	Transfer Data Most Significant Bit (MSB) first (default for I2S protocol)
0x1	LSBIT	Transfer Data Least Significant Bit (LSB) first

Bits 14:13 – EXTEND[1:0]: Data Formatting Bit Extension
This field defines the bit value used to extend data samples in the Formatting Unit.

EXTEND[1:0]	Name	Description
0x0	ZERO	Extend with zeros
0x1	ONE	Extend with ones
0x2	MSBIT	Extend with Most Significant Bit
0x3	LSBIT	Extend with Least Significant Bit

Bit 12 – WORDADJ: Data Word Formatting Adjust
This field defines left or right adjustment of data samples in the word in the Formatting Unit. for details.

WORDADJ	Name	Description
0x0	RIGHT	Data is right adjusted in word
0x1	LEFT	Data is left adjusted in word

Bits 10:8 – DATASIZE[2:0]: Data Word Size
This field defines the number of bits in each data sample. For 8-bit compact stereo, two 8-bit data samples are packed in bits 15 to 0 of the DATAm register. For 16-bit compact stereo, two 16-bit data samples are packed in bits 31 to 0 of the DATAm register.

DATASIZE[2:0]	Name	Description
0x0	32	32 bits
0x1	24	24 bits
0x2	20	20 bits
0x3	18	18 bits
0x4	16	16 bits
0x5	16C	16 bits compact stereo

– If the prescaler is used, select a prescaler synchronization operation via the Prescaler and Counter Synchronization bit group in the Control A register (CTRLA.PRESYNC).

5. Select one-shot operation by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT).
6. If desired, configure the counting direction 'down' (starting from the TOP value) by writing a '1' to the Counter Direction bit in the Control B register (CTRLBSET.DIR).
7. For capture operation, enable the individual channels to capture in the Capture Channel x Enable bit group in the Control C register (CTRLC.CAPTEN).
8. If desired, enable inversion of the waveform output or IO pin input signal for individual channels via the Waveform Output Invert Enable bit group in the Control C register (CTRLC.INVEN).

30.6.2.2 Enabling, Disabling and Resetting

The TC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TC is disbled by writing a zero to CTRLA.ENABLE.

The TC is reset by writing a one to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TC, except DBGCTRL, will be reset to their initial state, and the TC will be disabled. Refer to the CTRLA register for details.

The TC should be disabled before the TC is reset in order to avoid undefined behavior.

30.6.2.3 Prescaler Selection

The GCLK_TCx is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

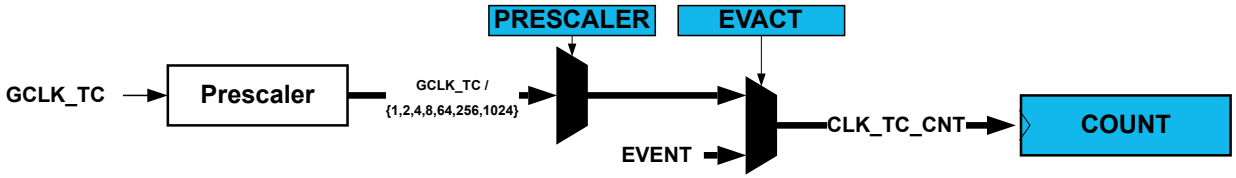
If the prescaler value is higher than one, the counter update condition can be optionally executed on the next GCLK_TCx clock pulse or the next prescaled clock pulse. For further details, refer to Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) description.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TC_CNT.

Figure 30-2. Prescaler



30.6.2.4 Counter Mode

The counter mode is selected by the Mode bit group in the Control A register (CTRLA.MODE). By default, the counter is enabled in the 16-bit counter resolution. Three counter resolutions are available:

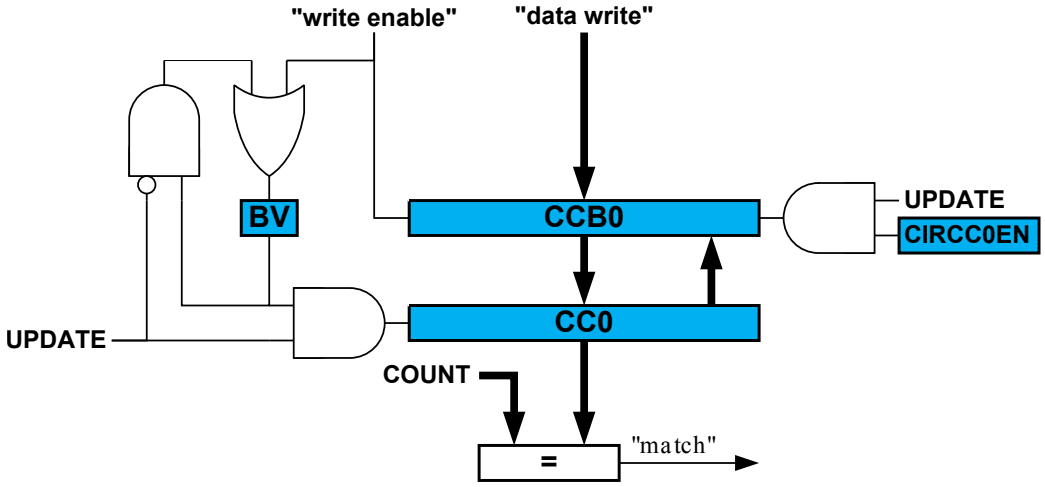
- COUNT8: The 8-bit TC has its own Period register (PER). This register is used to store the period value that can be used as the top value for waveform generation.
- COUNT16: 16-bit is the default counter mode. There is no dedicated period register in this mode.
- COUNT32: This mode is achieved by pairing two 16-bit TC peripherals. TC3 is paired with TC4, and TC5 is paired with TC6. TC7 does not support 32-bit resolution.

One-shot operation can be enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TCC will count until an overflow or underflow occurs and stop counting. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

31.6.3.2 Circular Buffer

The Period register (PER) and the compare channels register (CC0 to CC3) support circular buffer operation. When circular buffer operation is enabled, the PER or CCx values are copied into the corresponding buffer registers at each update condition. Circular buffering is dedicated to RAMP2, RAMP2A, and DSBOTH operations.

Figure 31-17. Circular Buffer on Channel 0



31.6.3.3 Dithering Operation

The TCC supports dithering on Pulse-width or Period on a 16, 32 or 64 PWM cycles frame.

Dithering consists in adding some extra clocks cycles in a frame of several PWM cycles, and can improve the accuracy of the *average* output pulse width and period. The extra clock cycles are added on some of the compare match signals, one at a time, through a "blue noise" process that minimizes the flickering on the resulting dither patterns.

Dithering is enabled by writing the corresponding configuration in the Enhanced Resolution bits in CTRLA register (CTRLA.RESOLUTION):

- DITH4 enable dithering every 16 PWM frames
- DITH5 enable dithering every 32 PWM frames
- DITH6 enable dithering every 64 PWM frames

The DITHERCY bits of COUNT, PER and CCx define the number of extra cycles to add into the frame (DITHERCY bits from the respective COUNT, PER or CCx registers). The remaining bits of COUNT, PER, CCx define the compare value itself.

The pseudo code, giving the extra cycles insertion regarding the cycle is:

```
int extra_cycle(resolution, dithercy, cycle){
  int MASK;
  int value
  switch (resolution){
    DITH4: MASK = 0x0f;
    DITH5: MASK = 0x1f;
    DITH6: MASK = 0x3f;
  }
```

Value	Name	Description	
		Counter Reloaded	Prescaler
0x0	GCLK	Reload or reset Counter on next GCLK	-
0x1	PRESC	Reload or reset Counter on next prescaler clock	-
0x2	RESYNC	Reload or reset Counter on next GCLK	Reset prescaler counter
0x3	Reserved		

Bit 11 – RUNSTDBY: Run in Standby
This bit is used to keep the TCC running in standby mode.

This bit is not synchronized.

Value	Description
0	The TCC is halted in standby.
1	The TCC continues to run in standby.

Bits 10:8 – PRESCALER[2:0]: Prescaler
These bits select the Counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TCC
0x1	DIV2	Prescaler: GCLK_TCC/2
0x2	DIV4	Prescaler: GCLK_TCC/4
0x3	DIV8	Prescaler: GCLK_TCC/8
0x4	DIV16	Prescaler: GCLK_TCC/16
0x5	DIV64	Prescaler: GCLK_TCC/64
0x6	DIV256	Prescaler: GCLK_TCC/256
0x7	DIV1024	Prescaler: GCLK_TCC/1024

Bits 6:5 – RESOLUTION[1:0]: Dithering Resolution
These bits increase the TCC resolution by enabling the dithering options.

These bits are not synchronized.

Table 31-7. Dithering

Value	Name	Description
0x0	NONE	The dithering is disabled.
0x1	DITH4	Dithering is done every 16 PWM frames. PER[3:0] and CCx[3:0] contain dithering pattern selection.

When the endpoint is enabled, the USB module then checks the Endpoint Configuration register (EPCFG) of the addressed output endpoint. If the type of the endpoint (EPCFG.EPTYPE0) is not set to OUT, the USB module returns to idle and waits for the next token packet.

The USB module then fetches the Data Buffer Address (ADDR) from the addressed endpoint's descriptor, and waits for a DATA0 or DATA1 packet. If a PID error or any other PID than DATA0 or DATA1 is detected, the USB module returns to idle and waits for the next token packet.

If EPSTATUS.STALLRQ0 in EPSTATUS is set, the incoming data is discarded. If the endpoint is not isochronous, a STALL handshake is returned to the host and the Transmit Stall Bank 0 interrupt bit in EPINTFLAG (EPINTFLAG.STALL0) is set.

For isochronous endpoints, data from both a DATA0 and DATA1 packet will be accepted. For other endpoint types the PID is checked against EPSTATUS.DTGLOUT. If a PID mismatch occurs, the incoming data is discarded, and an ACK handshake is returned to the host.

If EPSTATUS.BK0RDY is set, the incoming data is discarded, the bit Transmit Fail 0 interrupt bit in EPINTFLAG (EPINTFLAG.TRFAIL0) and the status bit STATUS_BK.ERRORFLOW are set. If the endpoint is not isochronous, a NAK handshake is returned to the host.

The incoming data is written to the data buffer pointed to by the Data Buffer Address (ADDR). If the number of received data bytes exceeds the maximum data payload specified as PCKSIZE.SIZE, the remainders of the received data bytes are discarded. The packet will still be checked for bit-stuff and CRC errors. If a bit-stuff or CRC error is detected in the packet, the USB module returns to idle and waits for the next token packet.

If the endpoint is isochronous and a bit-stuff or CRC error in the incoming data, the number of received data bytes, excluding CRC, is written to PCKSIZE.BYTE_COUNT. Finally the EPINTFLAG.TRFAIL0 and CRC Error bit in the Device Bank Status register (STATUS_BK.CRCERR) is set for the addressed endpoint.

If data was successfully received, an ACK handshake is returned to the host if the endpoint is not isochronous, and the number of received data bytes, excluding CRC, is written to PCKSIZE.BYTE_COUNT. If the number of received data bytes is the maximum data payload specified by PCKSIZE.SIZE no CRC data bytes are written to the data buffer. If the number of received data bytes is the maximum data payload specified by PCKSIZE.SIZE minus one, only the first CRC data byte is written to the data buffer If the number of received data is equal or less than the data payload specified by PCKSIZE.SIZE minus two, both CRC data bytes are written to the data buffer.

Finally in EPSTATUS for the addressed output endpoint, EPSTATUS.BK0RDY is set and EPSTATUS.DTGLOUT is toggled if the endpoint is not isochronous. The flag Transmit Complete 0 interrupt bit in EPINTFLAG (EPINTFLAG.TRCPT0) is set for the addressed endpoint.

32.6.2.8 Multi-Packet Transfers for OUT Endpoint

The number of data bytes received is stored in endpoint PCKSIZE.BYTE_COUNT as for normal operation. Since PCKSIZE.BYTE_COUNT is updated after each transaction, it must be set to zero when setting up a new transfer. The total number of bytes to be received must be written to PCKSIZE.MULTI_PACKET_SIZE. This value must be a multiple of PCKSIZE.SIZE, otherwise excess data may be written to SRAM locations used by other parts of the application.

EPSTATUS.DTGLOUT management for non-isochronous packets and EPINTFLAG.BK1RDY/BK0RDY management are as for normal operation.

If a maximum payload size packet is received, PCKSIZE.BYTE_COUNT will be incremented by PCKSIZE.SIZE after the transaction has completed, and EPSTATUS.DTGLOUT will be toggled if the endpoint is not isochronous. If the updated PCKSIZE.BYTE_COUNT is equal to

Table 37-32. Accuracy Characteristics(1) (Device Variant A)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
RES	Input resolution			-	-	10	Bits
INL	Integral non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	0.75	1.1	2.5	LSB
			V_{DD} = 3.6V	0.6	1.2	1.5	
		V_{REF} = V_{DDANA}	V_{DD} = 1.6V	1.4	2.2	2.5	
			V_{DD} = 3.6V	0.9	1.4	1.5	
		V_{REF}= INT1V	V_{DD} = 1.6V	0.75	1.3	1.5	
			V_{DD} = 3.6V	0.8	1.2	1.5	
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.9	+/-1.2	+/-1.5	LSB
			V_{DD} = 3.6V	+/-0.9	+/-1.1	+/-1.2	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-1.1	+/-1.5	+/-1.7	
			V_{DD} = 3.6V	+/-1.0	+/-1.1	+/-1.2	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-1.1	+/-1.4	+/-1.5	
			V_{DD} = 3.6V	+/-1.0	+/-1.5	+/-1.6	
	Gain error	Ext. V_{REF}		+/-1.5	+/-5	+/-10	mV
	Offset error	Ext. V_{REF}		+/-2	+/-3	+/-6	mV

Table 37-33. Accuracy Characteristics(1) (Device Variant B and C)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
RES	Input resolution			-	-	10	Bits
INL	Integral non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	0.7	0.75	2	LSB
			V_{DD} = 3.6V	0.6	0.65	1.5	
		V_{REF} = V_{DDANA}	V_{DD} = 1.6V	0.6	0.85	2	
			V_{DD} = 3.6V	0.5	0.8	1.5	
		V_{REF}= INT1V	V_{DD} = 1.6V	0.5	0.75	1.5	
			V_{DD} = 3.6V	0.7	0.8	1.5	
DNL	Differential non-linearity	V_{REF}= Ext 1.0V	V_{DD} = 1.6V	+/-0.3	+/-0.4	+/-1.0	LSB
			V_{DD} = 3.6V	+/-0.25	+/-0.4	+/-0.75	
		V_{REF}= V_{DDANA}	V_{DD} = 1.6V	+/-0.4	+/-0.55	+/-1.5	
			V_{DD} = 3.6V	+/-0.2	+/-0.3	+/-0.75	
		V_{REF}= INT1V	V_{DD} = 1.6V	+/-0.5	+/-0.7	+/-1.5	
			V_{DD} = 3.6V	+/-0.4	+/-0.7	+/-1.5	

40.1.1.7 DMAC

1 – When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.
This happens if the channel number of the channel being enabled is lower than the channel already active.
Errata reference: 15683
Fix/Workaround:
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

2 – If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.
Errata reference: 13507
Fix/Workaround:
Add a NOP instruction between each write to CRCDATAIN register.

40.1.1.8 EIC

1 – When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using CTRLA ENABLE bit.
Errata reference: 15341
Fix/Workaround:
Clear the INTFLAG bit once the EIC enabled and before enabling the interrupts.

40.1.1.9 NVMCTRL

1 – Default value of MANW in NVM.CTRLB is 0.
This can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to NVM area.
Errata reference: 13134
Fix/Workaround:
Set MANW in the NVM.CTRLB to 1 at startup

2 – When external reset is active it causes a high leakage current on VDDIO.
Errata reference: 13446
Fix/Workaround:
Minimize the time external reset is active.

3 – When the part is secured and EEPROM emulation area configured to none, the CRC32 is not executed on the entire flash area but up to the on-chip flash size minus half a row.
Errata reference: 11988
Fix/Workaround:
When using CRC32 on a protected device with EEPROM emulation area configured to none, compute the reference CRC32 value to the full chip flash size minus half row.

descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.
This happens if the channel number of the channel being enabled is lower than the channel already active.
Errata reference: 15683
Fix/Workaround:
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

2 – If data is written to CRCDATAIN in two consecutive instructions, the CRC computation may be incorrect.
Errata reference: 13507
Fix/Workaround:
Add a NOP instruction between each write to CRCDATAIN register.

40.2.1.6 EIC

1 – When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using CTRLA ENABLE bit.
Errata reference: 15341
Fix/Workaround:
Clear the INTFLAG bit once the EIC enabled and before enabling the interrupts.

40.2.1.7 NVMCTRL

1 – The NVMCTRL.INTFLAG.READY bit is not updated after a RWWEEER command and will keep holding a 1 value. If a new RWWEEER command is issued it can be accepted even if the previous RWWEEER command is ongoing. The ongoing NVM RWWEER will be aborted, the content of the row under erase will be unpredictable.
Errata reference: 13588
Fix/Workaround:
Perform a dummy write to the page buffer right before issuing a RWWEEER command. This will make the INTFLAG.READY bit behave as expected.

2 – Default value of MANW in NVM.CTRLB is 0.
This can lead to spurious writes to the NVM if a data write is done through a pointer with a wrong address corresponding to NVM area.
Errata reference: 13134
Fix/Workaround:
Set MANW in the NVM.CTRLB to 1 at startup

3 – When external reset is active it causes a high leakage current on VDDIO.
Errata reference: 13446
Fix/Workaround:
Minimize the time external reset is active.

44.6.3 Analog-to-Digital (ADC) characteristics

Table 44-13. Operating Conditions (Device Variant A)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
RES	Resolution		8	-	12	bits
f_{CLK_ADC}	ADC Clock frequency		30	-	2100	kHz
	Sample rate(1)	Single shot (with VDDANA > 3.0V) (4)	5	-	300	ksps
		Free running	5	-	350	ksps
	Sampling time(1)		0.5	-	-	cycles
	Conversion time(1)	1x Gain	-	6	-	cycles
V_{REF}	Voltage reference range		1.0	-	V_{DDANA}-0.6	V
$V_{REFINT1V}$	Internal 1V reference (2)		-	1.0	-	V
$V_{REFINTVCC0}$	Internal ratiometric reference 0(2)		-	V_{DDANA}/ 1.48	-	V
$V_{REFINTVCC0}$ Voltage Error	Internal ratiometric reference 0(2) error	2.0V < V_{DDANA}<3.63V	-1.0	-	+1.0	%
$V_{REFINTVCC1}$	Internal ratiometric reference 1(2)	V_{DDANA}>2.0V	-	V_{DDANA}/2	-	V
$V_{REFINTVCC1}$ Voltage Error	Internal ratiometric reference 1(2) error	2.0V < V_{DDANA}<3.63V	-1.0	-	+1.0	%
	Conversion range(1)	Differential mode	-V_{REF}/ GAIN	-	+V_{REF}/GAIN	V
		Single-ended mode	0.0	-	+V_{REF}/GAIN	V
C_{SAMPLE}	Sampling capacitance(2)		-	3.5	-	pF
R_{SAMPLE}	Input channel source resistance(2)		-	-	3.5	kΩ
I_{DD}	DC supply current(1)	f_{CLK_ADC} = 2.1MHz(3)	-	1.25	1.85	mA

Note:

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.
3. In this condition and for a sample rate of 350ksps, 1 Conversion at gain 1x takes 6 clock cycles of the ADC clock (conditions: 1X gain, 12-bit resolution, differential mode, free-running).