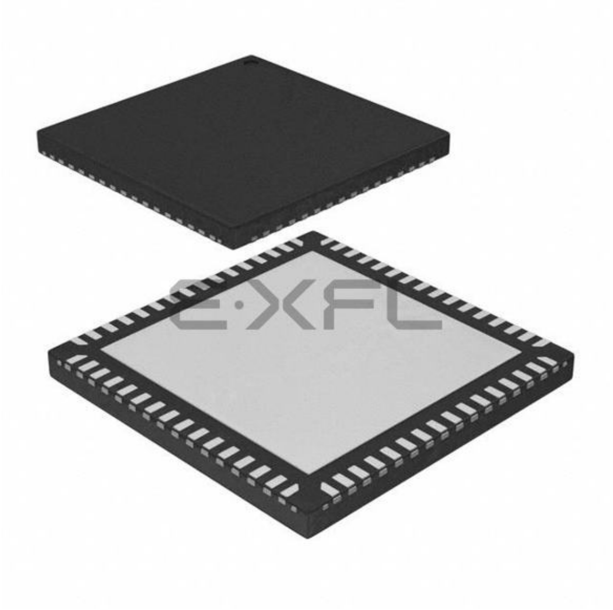

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j17a-mft

Device Variant	DID.DEVSEL	Device ID (DID)
Reserved	0x25	
SAMD21E16B	0x26	0x10011426 (die revision E) 0x10011526 (die revision F)
SAMD21E15B	0x27	0x10011427 (die revision E) 0x10011527 (die revision F)
Reserved	0x28-0x54	
SAMD21E16B (WLCSP)	0x55	0x10011455 (die revision E)
SAMD21E15B (WLCSP)	0x56	0x10011456 (die revision E)
Reserved	0x57 - 0x61	
SAMD21E16C (WLCSP)	0x62	0x10011562 (die revision F)
SAMD21E15C (WLCSP)	0x63	0x10011563 (die revision F)
Reserved	0x64-0xFF	

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

Related Links

DID

Pin[1]			I/O Pin	Supply	A	B[2][3]					C	D	E	F	G	H
SAMD21E	SAMD21G	SAMD21J			EIC	REF	ADC	AC	PTC	DAC	SERCOM[2][3]	SERCOM-ALT	TC[4] /TCC	TCC	COM	AC/ GCLK
		28	PB15	VDDIO	EXTINT[15]				X[15]		SERCOM4/PAD[3]		TC5/WO[1]			GCLK_IO[1]
	21	29	PA12	VDDIO	EXTINT[12]						SERCOM2/PAD[0]	SERCOM4/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		AC/CMP[0]
	22	30	PA13	VDDIO	EXTINT[13]						SERCOM2/PAD[1]	SERCOM4/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		AC/CMP[1]
15	23	31	PA14	VDDIO	EXTINT[14]						SERCOM2/PAD[2]	SERCOM4/PAD[2]	TC3/WO[0]	TCC0/WO[4]		GCLK_IO[0]
16	24	32	PA15	VDDIO	EXTINT[15]						SERCOM2/PAD[3]	SERCOM4/PAD[3]	TC3/WO[1]	TCC0/WO[5]		GCLK_IO[1]
17	25	35	PA16	VDDIO	EXTINT[0]				X[4]		SERCOM1/PAD[0]	SERCOM3/PAD[0]	TCC2/WO[0]	TCC0/WO[6]		GCLK_IO[2]
18	26	36	PA17	VDDIO	EXTINT[1]				X[5]		SERCOM1/PAD[1]	SERCOM3/PAD[1]	TCC2/WO[1]	TCC0/WO[7]		GCLK_IO[3]
19	27	37	PA18	VDDIO	EXTINT[2]				X[6]		SERCOM1/PAD[2]	SERCOM3/PAD[2]	TC3/WO[0]	TCC0/WO[2]		AC/CMP[0]
20	28	38	PA19	VDDIO	EXTINT[3]				X[7]		SERCOM1/PAD[3]	SERCOM3/PAD[3]	TC3/WO[1]	TCC0/WO[3]	I2S/SD[0]	AC/CMP[1]
		39	PB16	VDDIO	EXTINT[0]						SERCOM5/PAD[0]		TC6/WO[0]	TCC0/WO[4]	I2S/SD[1]	GCLK_IO[2]
		40	PB17	VDDIO	EXTINT[1]						SERCOM5/PAD[1]		TC6/WO[1]	TCC0/WO[5]	I2S/MCK[0]	GCLK_IO[3]
	29	41	PA20	VDDIO	EXTINT[4]				X[8]		SERCOM5/PAD[2]	SERCOM3/PAD[2]	TC7/WO[0]	TCC0/WO[6]	I2S/SCK[0]	GCLK_IO[4]
	30	42	PA21	VDDIO	EXTINT[5]				X[9]		SERCOM5/PAD[3]	SERCOM3/PAD[3]	TC7/WO[1]	TCC0/WO[7]	I2S/FS[0]	GCLK_IO[5]
21	31	43	PA22	VDDIO	EXTINT[6]				X[10]		SERCOM3/PAD[0]	SERCOM5/PAD[0]	TC4/WO[0]	TCC0/WO[4]		GCLK_IO[6]
22	32	44	PA23	VDDIO	EXTINT[7]				X[11]		SERCOM3/PAD[1]	SERCOM5/PAD[1]	TC4/WO[1]	TCC0/WO[5]	USB/SOF 1kHz	GCLK_IO[7]
23	33	45	PA24[6]	VDDIO	EXTINT[12]						SERCOM3/PAD[2]	SERCOM5/PAD[2]	TC5/WO[0]	TCC1/WO[2]	USB/DM	
24	34	46	PA25[6]	VDDIO	EXTINT[13]						SERCOM3/PAD[3]	SERCOM5/PAD[3]	TC5/WO[1]	TCC1/WO[3]	USB/DP	
	37	49	PB22	VDDIO	EXTINT[6]							SERCOM5/PAD[2]	TC7/WO[0]			GCLK_IO[0]
	38	50	PB23	VDDIO	EXTINT[7]							SERCOM5/PAD[3]	TC7/WO[1]			GCLK_IO[1]
25	39	51	PA27	VDDIO	EXTINT[15]											GCLK_IO[0]
27	41	53	PA28	VDDIO	EXTINT[8]											GCLK_IO[0]
31	45	57	PA30	VDDIO	EXTINT[10]							SERCOM1/PAD[2]	TCC1/WO[0]		SWCLK	GCLK_IO[0]
32	46	58	PA31	VDDIO	EXTINT[11]							SERCOM1/PAD[3]	TCC1/WO[1]		SWDIO[5]	
		59	PB30	VDDIO	EXTINT[14]							SERCOM5/PAD[0]	TCC0/WO[0]	TCC1/WO[2]		
		60	PB31	VDDIO	EXTINT[15]							SERCOM5/PAD[1]	TCC0/WO[1]	TCC1/WO[3]		
		61	PB00	VDDANA	EXTINT[0]		AIN[8]		Y[6]			SERCOM5/PAD[2]	TC7/WO[0]			
		62	PB01	VDDANA	EXTINT[1]		AIN[9]		Y[7]			SERCOM5/PAD[3]	TC7/WO[1]			
	47	63	PB02	VDDANA	EXTINT[2]		AIN[10]		Y[8]			SERCOM5/PAD[0]	TC6/WO[0]			
	48	64	PB03	VDDANA	EXTINT[3]		AIN[11]		Y[9]			SERCOM5/PAD[1]	TC6/WO[1]			

1. Use the SAMD21J pinout muxing for WLCSP45 package.
2. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
3. Only some pins can be used in SERCOM I2C mode. Refer to SERCOM I2C Pins.

Related Links

NVMCTRL – Non-Volatile Memory Controller

BOD33

CTRL

10.3.2 NVM Software Calibration Area Mapping

The NVM Software Calibration Area contains calibration data that are measured and written during production test. These calibration values should be read by the application software and written back to the corresponding register.

The NVM Software Calibration Area can be read at address 0x806020.

The NVM Software Calibration Area can not be written.

Table 10-5. NVM Software Calibration Area Mapping

Bit Position	Name	Description
2:0	Reserved	
14:3	Reserved	
26:15	Reserved	
34:27	ADC LINEARITY	ADC Linearity Calibration. Should be written to ADC CALIB register.
37:35	ADC BIASCAL	ADC Bias Calibration. Should be written to ADC CALIB register.
44:38	OSC32K CAL	OSC32KCalibration. Should be written to SYSCTRL OSC32K register.
49:45	USB TRANSN	USB TRANSN calibration value. Should be written to USB PADCAL register.
54:50	USB TRANSP	USB TRANSP calibration value. Should be written to USB PADCAL register.
57:55	USB TRIM	USB TRIM calibration value. Should be written to the USB PADCAL register.
63:58	DFLL48M COARSE CAL	DFLL48M Coarse calibration value. Should be written to SYSCTRL DFLLVAL register.
73:64	Reserved	
127:74	Reserved	

10.3.3 Serial Number

Each device has a unique 128-bit serial number which is a concatenation of four 32-bit words contained at the following addresses:

Word 0: 0x0080A00C

Word 1: 0x0080A040

Word 2: 0x0080A044

Word 3: 0x0080A048

Bit 5 – USB
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 4 – DMAC:
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 3 – PORT
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 2 – NVMCTRL
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Bit 1 – DSU
Writing a zero to these bits has no effect.

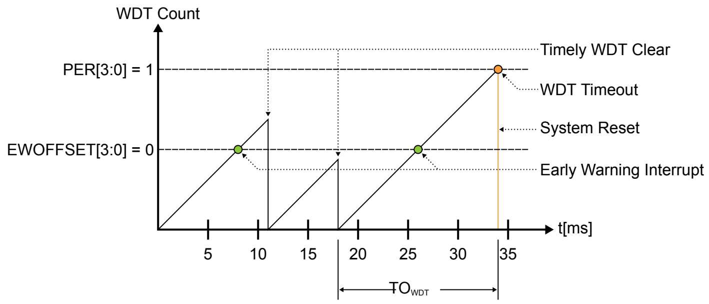
Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

Value	Description
0	Write-protection is disabled.
1	Write-protection is enabled.

Write Protect Set

Name: WPSET
Offset: 0x04
Reset: 0x000002
Property: –

Figure 18-2. Normal-Mode Operation

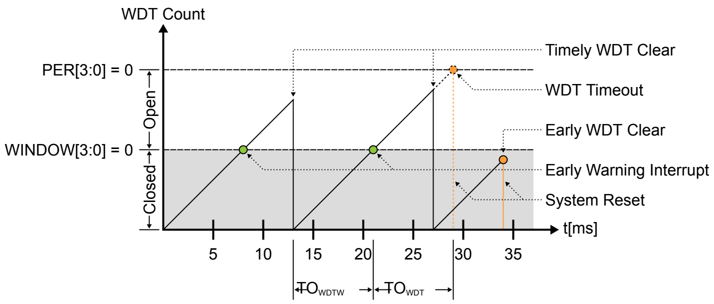


18.6.2.5 Window Mode

In Window mode operation, the WDT uses two different time specifications: the WDT can only be cleared by writing 0xA5 to the CLEAR register *after* the closed window time-out period (TO_{WDTW}), during the subsequent Normal time-out period (TO_{WDTW}). If the WDT is cleared before the time window opens (before TO_{WDTW} is over), the WDT will issue a system reset. Both parameters TO_{WDTW} and TO_{WDT} are periods in a range from 8ms to 16s, so the total duration of the WDT time-out period is the sum of the two parameters. The closed window period is defined by the Window Period bits in the Configuration register (CONFIG.WINDOW), and the open window period is defined by the Period bits in the Configuration register (CONFIG.PER).

By default, the Early Warning interrupt is disabled. If it is desired, the Early Warning Interrupt Enable bit in the Interrupt Enable register (INTENSET.EW) must be written to '1'. The Early Warning Interrupt is disabled again by writing a '1' to the Early Warning Interrupt bit in the Interrupt Enable Clear (INTENCLR.EW) register. If the Early Warning interrupt is enabled in Window mode, the interrupt is generated at the start of the open window period, i.e. after TO_{WDTW}. The Window mode operation is illustrated in figure Window-Mode Operation.

Figure 18-3. Window-Mode Operation



18.6.3 Additional Features

18.6.3.1 Always-On Mode

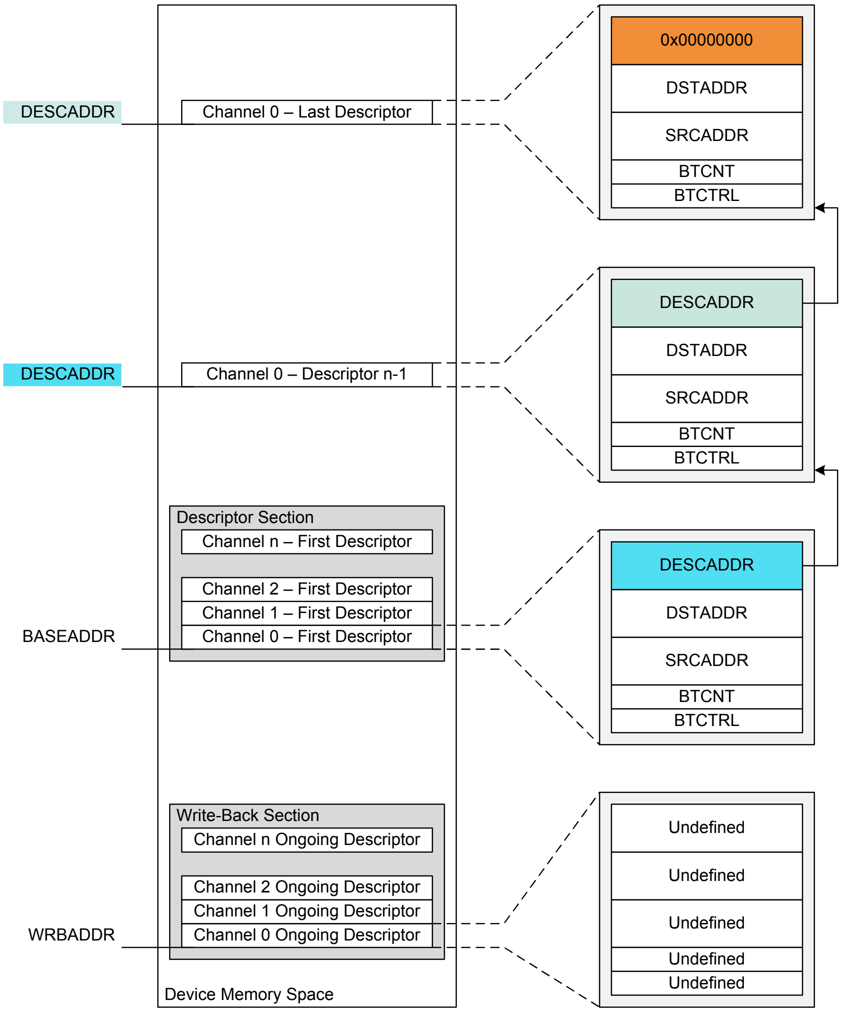
The Always-On mode is enabled by setting the Always-On bit in the Control register (CTRLA.ALWAYSON=1). When the Always-On mode is enabled, the WDT runs continuously, regardless of the state of CTRL.ENABLE. Once written, the Always-On bit can only be cleared by a power-on reset. The Configuration (CONFIG) and Early Warning Control (EWCTRL) registers are read-only registers while the CTRL.ALWAYSON bit is set. Thus, the time period configuration bits (CONFIG.PER, CONFIG.WINDOW, EWCTRL.EWOFFSET) of the WDT cannot be changed.

Enabling or disabling Window mode operation by writing the Window Enable bit (CTRLA.WEN) is allowed while in Always-On mode, but note that CONFIG.PER cannot be changed.

  - Enable 12 independent transfers
  - Automatic descriptor fetch for each channel
  - Suspend/resume operation support for each channel
- Flexible arbitration scheme
  - 4 configurable priority levels for each channel
  - Fixed or round-robin priority scheme within each priority level
- From 1 to 256KB data transfer in a single block transfer
- Multiple addressing modes
  - Static
  - Configurable increment scheme
- Optional interrupt generation
  - On block transfer complete
  - On error detection
  - On channel suspend
- 4 event inputs
  - One event input for each of the 4 least significant DMA channels
  - Can be selected to trigger normal transfers, periodic transfers or conditional transfers
  - Can be selected to suspend or resume channel operation
- 4 event outputs
  - One output event for each of the 4 least significant DMA channels
  - Selectable generation on AHB, block, or transaction transfer complete
- Error management supported by write-back function
  - Dedicated Write-Back memory section for each channel to store ongoing descriptor transfer
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE® 802.3)

ordered according to their channel number. The figure below shows an example of linked descriptors on DMA channel 0. For further details on linked descriptors, refer to Linked Descriptors.

Figure 20-3. Memory Sections


DESCADDR
Channel 0 – Last Descriptor
DESCADDR
Channel 0 – Descriptor n-1
Descriptor Section
Channel n – First Descriptor
Channel 2 – First Descriptor
Channel 1 – First Descriptor
Channel 0 – First Descriptor
BASEADDR
Write-Back Section
Channel n Ongoing Descriptor
Channel 2 Ongoing Descriptor
Channel 1 Ongoing Descriptor
Channel 0 Ongoing Descriptor
WRBADDR
Device Memory Space
0x00000000
DSTADDR
SRCADDR
BTCNT
BTCTRL
DESCADDR
DSTADDR
SRCADDR
BTCNT
BTCTRL
DESCADDR
DSTADDR
SRCADDR
BTCNT
BTCTRL
Undefined
Undefined
Undefined
Undefined
Undefined

The size of the descriptor and write-back memory sections is dependent on the number of the most significant enabled DMA channel *m*, as shown below:

$$Size = 128\text{bits} \cdot (m + 1)$$

For memory optimization, it is recommended to always use the less significant DMA channels if not all channels are required.

The descriptor and write-back memory sections can either be two separate memory sections, or they can share memory section (BASEADDR=WRBADDR). The benefit of having them in two separate sections, is that the same transaction for a channel can be repeated without having to modify the first transfer descriptor. The benefit of having descriptor memory and write-back memory in the same section is that it requires less SRAM. In addition, the latency from fetching the first descriptor of a transaction to the first burst transfer is executed, is reduced.

20.6.2.4 Arbitration

If a DMA channel is enabled and not suspended when it receives a transfer trigger, it will send a transfer request to the arbiter. When the arbiter receives the transfer request it will include the DMA channel in the queue of channels having pending transfers, and the corresponding Pending Channel x bit in the Pending Channels registers (PENDCH.PENDCHx) will be set. Depending on the arbitration scheme, the arbiter

Name: ACTIVE
Offset: 0x30
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	BTCNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	BTCNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ABUSY			ID[4:0]				
Access	R			R	R	R	R	R
Reset	0			0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
					LVLEX3	LVLEX2	LVLEX1	LVLEX0
Access					R	R	R	R
Reset					0	0	0	0

Bits 31:16 – BTCNT[15:0]: Active Channel Block Transfer Count
These bits hold the 16-bit block transfer count of the ongoing transfer. This value is stored in the active channel and written back in the corresponding Write-Back channel memory location when the arbiter grants a new channel access. The value is valid only when the active channel active busy flag (ABUSY) is set.

Bit 15 – ABUSY: Active Channel Busy
This bit is cleared when the active transfer count is written back in the write-back memory section.

This bit is set when the next descriptor transfer count is read from the write-back memory section.

Bits 12:8 – ID[4:0]: Active Channel ID
These bits hold the channel index currently stored in the active channel registers. The value is updated each time the arbiter grants a new channel transfer access request.

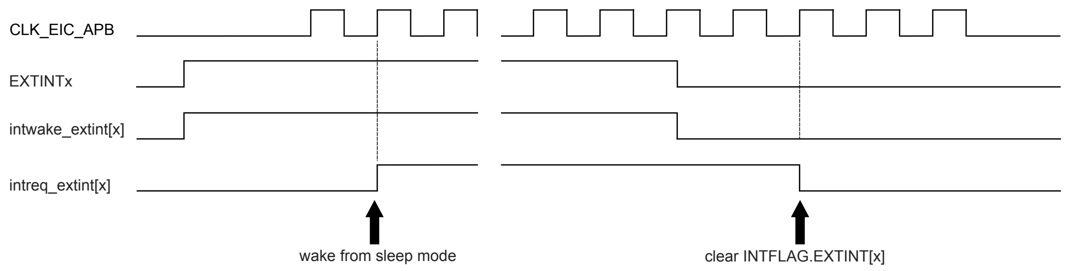
Bits 3,2,1,0 – LVLEXx: Level x Channel Trigger Request Executing [x=3..0]
This bit is set when a level-x channel trigger request is executing or pending.

This bit is cleared when no request is pending or being executed.

20.8.15 Descriptor Memory Section Base Address

Name: BASEADDR
Offset: 0x34
Reset: 0x00000000

Figure 21-3. Wake-Up Operation Example (High-Level Detection, No Filter, WAKEUPEN[x]=1)



21.6.9 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

When executing an operation that requires synchronization, the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY) will be set immediately, and cleared when synchronization is complete.

If an operation that requires synchronization is executed while STATUS.SYNCBUSY is one, the bus will be stalled. All operations will complete successfully, but the CPU will be stalled, and interrupts will be pending as long as the bus is stalled.

The following bits are synchronized when written:

- Software Reset bit in the Control register (CTRL.SWRST)
- Enable bit in the Control register (CTRL.ENABLE)

Related Links

Register Synchronization

21.7 Register Summary

Offset	Name	Bit Pos.								
0x00	CTRL	7:0							ENABLE	SWRST
0x01	STATUS	7:0	SYNCBUSY							
0x02	NMICTRL	7:0					NMIFILTEN	NMISENSE[2:0]		
0x03	NMIFLAG	7:0								NMI
0x04	EVCTRL	7:0	EXTINTEO7	EXTINTEO6	EXTINTEO5	EXTINTEO4	EXTINTEO3	EXTINTEO2	EXTINTEO1	EXTINTEO0
0x05		15:8	EXTINTEO15	EXTINTEO14	EXTINTEO13	EXTINTEO12	EXTINTEO11	EXTINTEO10	EXTINTEO9	EXTINTEO8
0x06		23:16							EXTINTEO17	EXTINTEO16
0x07		31:24								
0x08	INTENCLR	7:0	EXTINT7	EXTINT6	EXTINT5	EXTINT4	EXTINT3	EXTINT2	EXTINT1	EXTINT0
0x09		15:8	EXTINT15	EXTINT14	EXTINT13	EXTINT12	EXTINT11	EXTINT10	EXTINT9	EXTINT8
0x0A		23:16							EXTINT17	EXTINT16
0x0B		31:24								
0x0C	INTENSET	7:0	EXTINT7	EXTINT6	EXTINT5	EXTINT4	EXTINT3	EXTINT2	EXTINT1	EXTINT0
0x0D		15:8	EXTINT15	EXTINT14	EXTINT13	EXTINT12	EXTINT11	EXTINT10	EXTINT9	EXTINT8
0x0E		23:16							EXTINT17	EXTINT16
0x0F		31:24								

Figure 23-6. I/O Configuration - Totem-Pole Output with Disabled Input

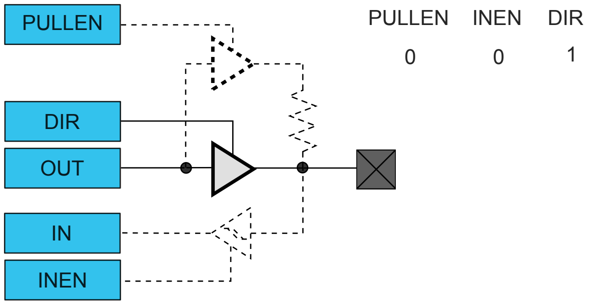


Figure 23-7. I/O Configuration - Totem-Pole Output with Enabled Input

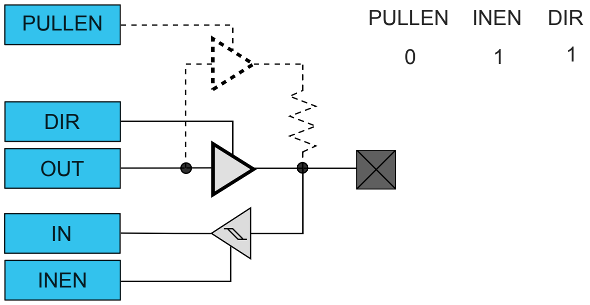
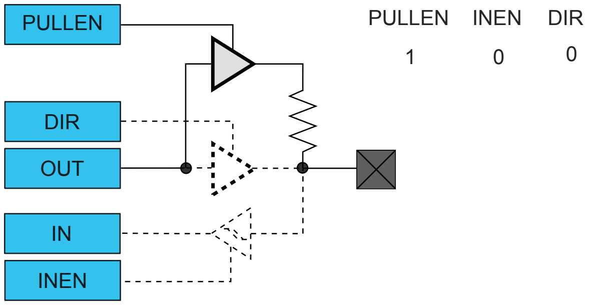


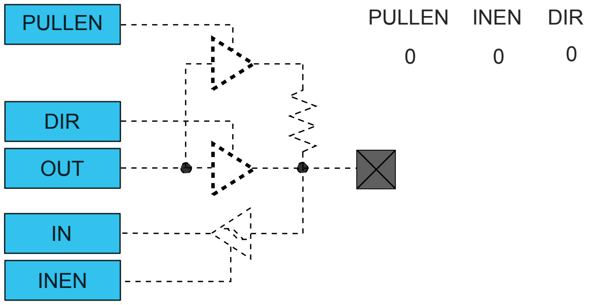
Figure 23-8. I/O Configuration - Output with Pull



23.6.3.4 Digital Functionality Disabled

Neither Input nor Output functionality are enabled.

Figure 23-9. I/O Configuration - Reset or Analog I/O: Digital Output, Input and Pull Disabled



23.6.4 PORT Access Priority

The PORT is accessed by different systems:

- The ARM® CPU through the ARM® single-cycle I/O port (IOBUS)
- The ARM® CPU through the high-speed matrix and the AHB/APB bridge (APB)

The following priority is adopted:

25. SERCOM – Serial Communication Interface

25.1 Overview

There are up to six instances of the serial communication interface (SERCOM) peripheral.

A SERCOM can be configured to support a number of modes: I^{2}C, SPI, and USART. When SERCOM is configured and enabled, all SERCOM resources will be dedicated to the selected mode.

The SERCOM serial engine consists of a transmitter and receiver, baud-rate generator and address matching functionality. It can use the internal generic clock or an external clock to operate in all sleep modes.

Related Links

SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter

SERCOM SPI – SERCOM Serial Peripheral Interface

SERCOM I2C – SERCOM Inter-Integrated Circuit

25.2 Features

- Interface for configuring into one of the following:
  - I^{2}C – Two-wire serial interface
    SMBus™ compatible
  - SPI – Serial peripheral interface
  - USART – Universal synchronous and asynchronous serial receiver and transmitter
- Single transmit buffer and double receive buffer
- Baud-rate generator
- Address match/mask logic
- Operational in all sleep modes
- Can be used with DMA

See the Related Links for full feature lists of the interface configurations.

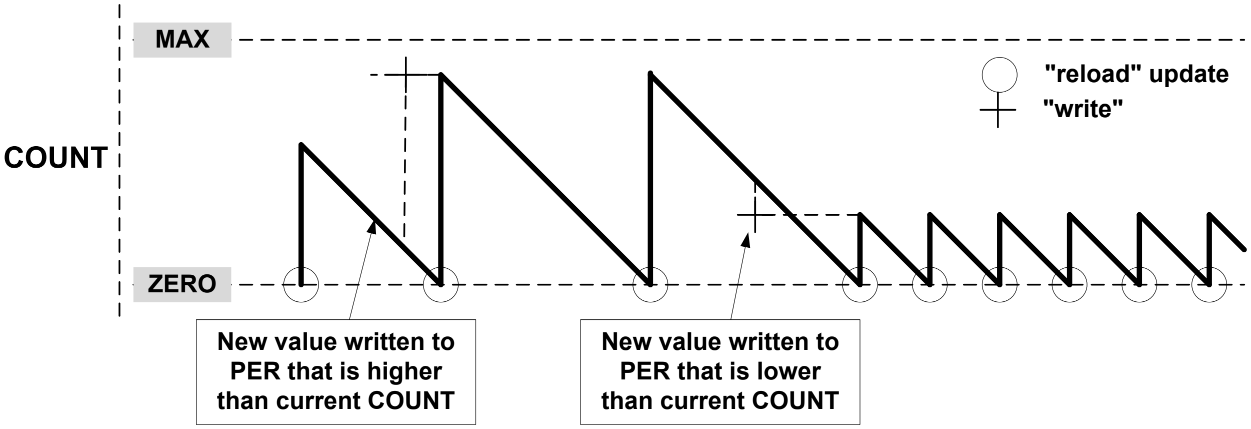
Related Links

SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter

SERCOM SPI – SERCOM Serial Peripheral Interface

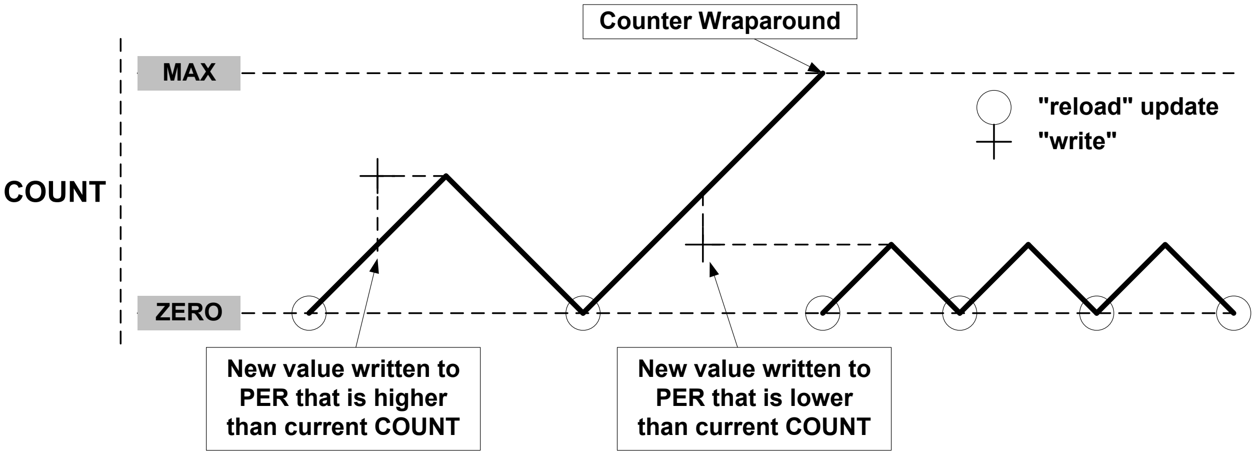
SERCOM I2C – SERCOM Inter-Integrated Circuit

Figure 31-11. Unbuffered Single-Slope Down-Counting Operation


MAX
COUNT
ZERO
"reload" update
"write"
New value written to PER that is higher than current COUNT
New value written to PER that is lower than current COUNT

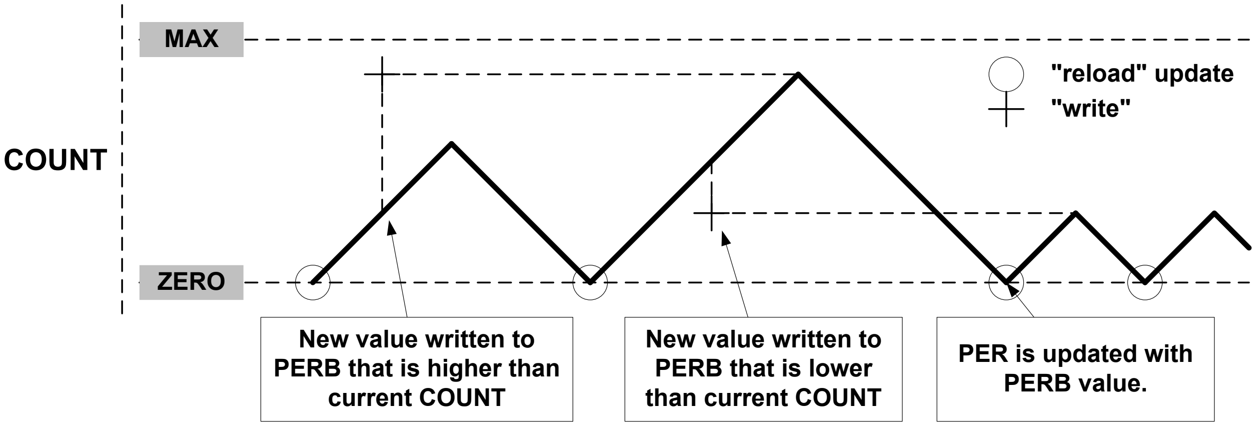
A counter wraparound can occur in any operation mode when up-counting without buffering, see Figure 31-10. COUNT and TOP are continuously compared, so when a new value that is lower than the current COUNT is written to TOP, COUNT will wrap before a compare match.

Figure 31-12. Unbuffered Dual-Slope Operation


Counter Wraparound
MAX
COUNT
ZERO
"reload" update
"write"
New value written to PER that is higher than current COUNT
New value written to PER that is lower than current COUNT

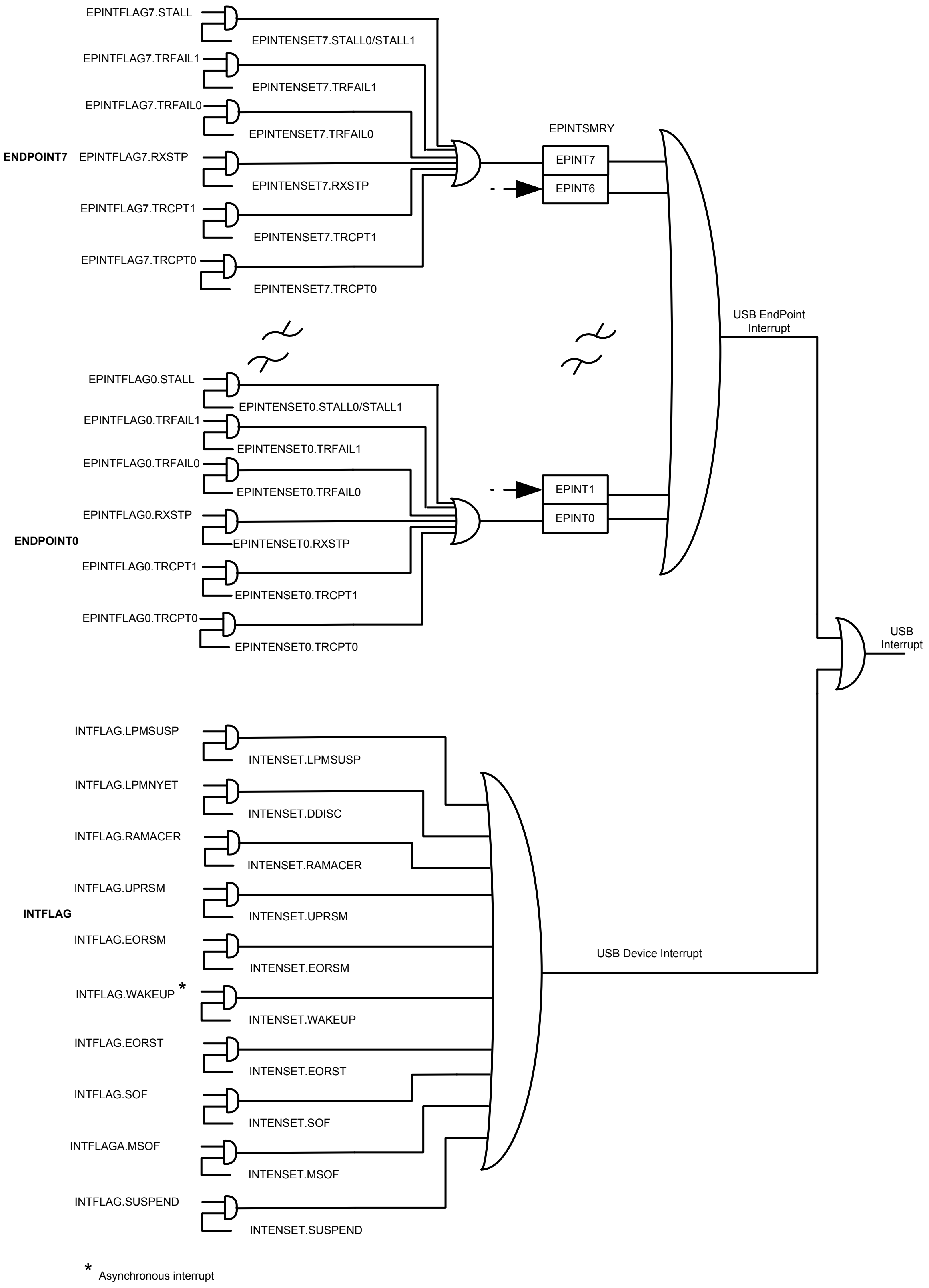
When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as shown in Figure 31-13. This prevents wraparound and the generation of odd waveforms.

Figure 31-13. Changing the Period Using Buffering


MAX
COUNT
ZERO
"reload" update
"write"
New value written to PERB that is higher than current COUNT
New value written to PERB that is lower than current COUNT
PER is updated with PERB value.

32.6.2.16 USB Device Interrupt

Figure 32-9. Device Interrupt



The WAKEUP is an asynchronous interrupt and can be used to wake-up the device from any sleep mode.

PTOKEN[1:0](1)	Description
0x2	OUT
0x3	Reserved

1. PTOKEN field is ignored when PTYPE is configured as EXTENDED.
2. Available only when PTYPE is configured as CONTROL

Theses bits are cleared upon sending a USB reset.

32.8.6.2 Interval for the Bulk-Out/Ping Transaction

Name: BINTERVAL
Offset: 0x103 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	BINTERVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BINTERVAL[7:0]: BINTERVAL
These bits contains the Ping/Bulk-out period.

These bits are cleared when a USB reset is sent or when PEN[n] is zero.

BINTERVAL	Description
=0	Multiple consecutive OUT token is sent in the same frame until it is acked by the peripheral
>0	One OUT token is sent every BINTERVAL frame until it is acked by the peripheral

Depending from the type of pipe the desired period is defined as:

PTYPE	Description
Interrupt	1 ms to 255 ms
Isochronous	2^(Binterval) * 1 ms
Bulk or control	1 ms to 255 ms
EXT LPM	bInterval ignored. Always 1 ms when a NYET is received.

32.8.6.3 Pipe Status Clear n

Name: PSTATUSCLR
Offset: 0x104 + (n x 0x20)
Reset: 0x00
Property: PAC Write-Protection

Property: NA

Bit	7	6	5	4	3	2	1	0
							ERRORFLOW	CRCERR
Access							R/W	R/W
Reset							x	x

Bit 1 – ERRORFLOW: Error Flow Status
This bit defines the Error Flow Status.

This bit is set when a Error Flow has been detected during transfer from/towards this bank.

For IN transfer, a NAK handshake has been received. For OUT transfer, a NAK handshake has been received. For Isochronous IN transfer, an overrun condition has occurred. For Isochronous OUT transfer, an underflow condition has occurred.

Value	Description
0	No Error Flow detected.
1	A Error Flow has been detected.

Bit 0 – CRCERR: CRC Error
This bit defines the CRC Error Status.

This bit is set when a CRC error has been detected in an isochronous IN endpoint bank.

Value	Description
0	No CRC Error.
1	CRC Error detected.

32.8.7.6 Host Control Pipe

Name: CTRL_PIPE
Offset: 0x0C
Reset: 0xXXXX
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

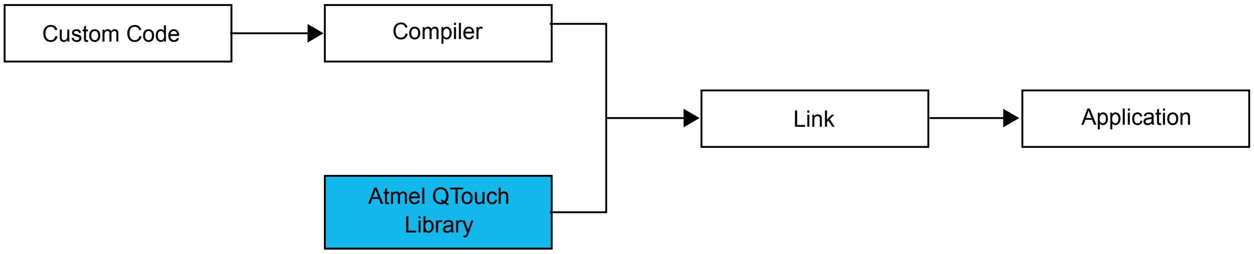
Bit	15	14	13	12	11	10	9	8
	PERMAX[3:0]				PEPNUM[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	x	0	0	0	x

Bit	7	6	5	4	3	2	1	0
		PDADDR[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	x

Bits 15:12 – PERMAX[3:0]: Pipe Error Max Number
These bits define the maximum number of error for this Pipe before freezing the pipe automatically.

Bits 11:8 – PEPNUM[3:0]: Pipe EndPoint Number
These bits define the number of endpoint for this Pipe.

Figure 36-5. QTouch Library Usage



For more information about QTouch Library, refer to the Atmel QTouch Library Peripheral Touch Controller User Guide.

Mode	Conditions	T_A	V_{CC}	Typ.	Max.	Units
IDLE0	Default operating conditions	25°C	3.3V	2.4	2.5	mA
		85°C	3.3V	2.5	2.6	
IDLE1	Default operating conditions	25°C	3.3V	1.8	1.9	
		85°C	3.3V	1.9	2	
IDLE2	Default operating conditions	25°C	3.3V	1.3	1.4	
		85°C	3.3V	1.4	1.5	
STANDBY	XOSC32K running, RTC running at 1kHz	25°C	3.3V	4.6	15.0	μA
		85°C	3.3V	43	102.0	
	XOSC32K and RTC stopped	25°C	3.3V	3.4	14.0	
		85°C	3.3V	42	100.0	

Table 37-10. Wake-up Time

Mode	Conditions	T_A	Min.	Typ.	Max.	Units
IDLE0	OSC8M used as main clock source, Cache disabled	25°C	-	4.0	-	μs
		85°C	-	4.0	-	
IDLE1	IOSC8M used as main clock source, Cache disabled	25°C	-	12.1	-	
		85°C	-	13.6	-	
IDLE2	IOSC8M used as main clock source, Cache disabled	25°C	-	13.0	-	
		85°C	-	14.5	-	
STANDBY	IOSC8M used as main clock source, Cache disabled	25°C	-	19.6	-	
		85°C	-	19.7	-	

Table 38-11. Device and Package Maximum Weight

140	mg

Table 38-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 38-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

6 – In I2C Slave mode, writing the CTRLB register when in the AMATCH or DRDY interrupt service routines can cause the state machine to reset.
Errata reference: 13574
Fix/Workaround:

Write CTRLB.ACKACT to 0 using the following sequence:

```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
```

Write CTRLB.ACKACT to 1 using the following sequence:

```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
// Re-enable interrupts if applicable.
```

Otherwise, only write to CTRLB in the AMATCH or DRDY interrupts if it is to close out a transaction.

When not closing a transaction, clear the AMATCH interrupt by writing a 1 to its bit position instead of using CTRLB.CMD. The DRDY interrupt is automatically cleared by reading/writing to the DATA register in smart mode. If not in smart mode, DRDY should be cleared by writing a 1 to its bit position.

Code replacements examples:

Current:

```
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_ACKACT;
```

Change to:

```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = SERCOM_I2CS_CTRLB_ACKACT;
// Re-enable interrupts if applicable.
```

Current:

```
SERCOM - CTRLB.reg &= ~SERCOM_I2CS_CTRLB_ACKACT;
```

Change to:

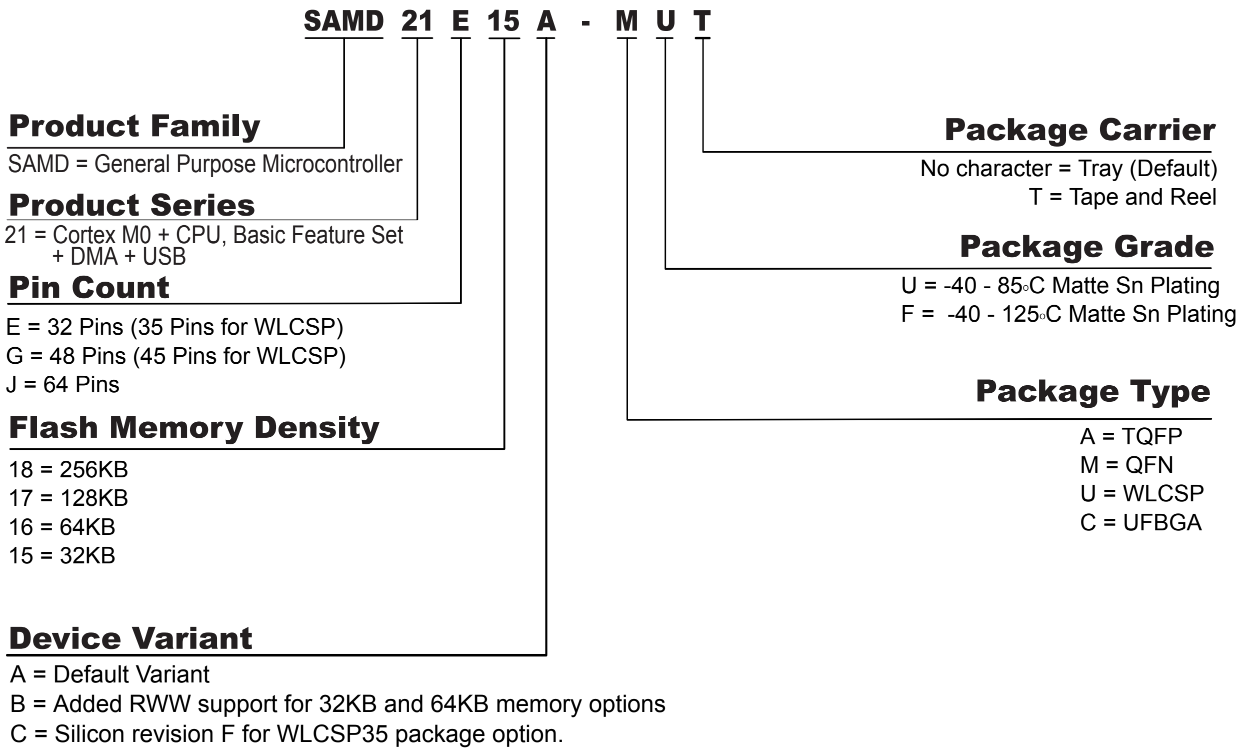
```
// If higher priority interrupts exist, then disable so that the
// following two writes are atomic.
SERCOM - STATUS.reg = 0;
SERCOM - CTRLB.reg = 0;
// Re-enable interrupts if applicable.
```

Current:

```
/* ACK or NACK address */
SERCOM - CTRLB.reg |= SERCOM_I2CS_CTRLB_CMD(0x3);
```

Change to:

```
// CMD=0x3 clears all interrupts, so to keep the result similar,
// PREC is cleared if it was set.
```



SAMD 21 E 15 A - M U T

Product Family

SAMD = General Purpose Microcontroller

Product Series

21 = Cortex M0 + CPU, Basic Feature Set
+ DMA + USB

Pin Count

E = 32 Pins (35 Pins for WLCSP)
G = 48 Pins (45 Pins for WLCSP)
J = 64 Pins

Flash Memory Density

18 = 256KB
17 = 128KB
16 = 64KB
15 = 32KB

Device Variant

A = Default Variant
B = Added RWW support for 32KB and 64KB memory options
C = Silicon revision F for WLCSP35 package option.

Package Carrier

No character = Tray (Default)
T = Tape and Reel

Package Grade

U = -40 - 85°C Matte Sn Plating
F = -40 - 125°C Matte Sn Plating

Package Type

A = TQFP
M = QFN
U = WLCSP
C = UFBGA

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check http://www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.