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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 20x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamd21j18a-au

32-bit ARM-Based Microcontrollers

Bit	7	6	5	4	3	2	1	0
		EIC	RTC	WDT	GCLK	SYSCTRL	PM	PAC0
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	1	1	1	1	1

Bit 6 – EIC: EIC APB Clock Enable

Value	Description
0	The APBA clock for the EIC is stopped.
1	The APBA clock for the EIC is enabled.

Bit 5 – RTC: RTC APB Clock Enable

Value	Description
0	The APBA clock for the RTC is stopped.
1	The APBA clock for the RTC is enabled.

Bit 4 – WDT: WDT APB Clock Enable

Value	Description
0	The APBA clock for the WDT is stopped.
1	The APBA clock for the WDT is enabled.

Bit 3 – GCLK: GCLK APB Clock Enable

Value	Description
0	The APBA clock for the GCLK is stopped.
1	The APBA clock for the GCLK is enabled.

Bit 2 – SYSCTRL: SYSCTRL APB Clock Enable

Value	Description
0	The APBA clock for the SYSCTRL is stopped.
1	The APBA clock for the SYSCTRL is enabled.

Bit 1 – PM: PM APB Clock Enable

Value	Description
0	The APBA clock for the PM is stopped.
1	The APBA clock for the PM is enabled.

Bit 0 – PAC0: PAC0 APB Clock Enable

Value	Description
0	The APBA clock for the PAC0 is stopped.
1	The APBA clock for the PAC0 is enabled.

16.8.9 APBB Mask

Name: APBBMASK
Offset: 0x1C
Reset: 0x0000007F

32-bit ARM-Based Microcontrollers

Bits 7,6,5,4,3,2,1,0 – PEREOx : Periodic Interval x Event Output Enable [x=7:0]

Value	Description
0	Periodic Interval x event is disabled and will not be generated.
1	Periodic Interval x event is enabled and will be generated.

19.8.7 Event Control - MODE2

Name: EVCTRL

Offset: 0x04

Reset: 0x0000

Property: Enable-Protected, Write-Protected

Bit	15	14	13	12	11	10	9	8
	OVFEO							ALARMEO0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PEREO7	PEREO6	PEREO5	PEREO4	PEREO3	PEREO2	PEREO1	PEREO0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVFEO: Overflow Event Output Enable

Value	Description
0	Overflow event is disabled and will not be generated.
1	Overflow event is enabled and will be generated for every overflow.

Bit 8 – ALARMEO0: Alarm 0 Event Output Enable

Value	Description
0	Alarm 0 event is disabled and will not be generated.
1	Alarm 0 event is enabled and will be generated for every alarm.

Bits 7,6,5,4,3,2,1,0 – PEREOx : Periodic Interval x Event Output Enable [x=7:0]

Value	Description
0	Periodic Interval x event is disabled and will not be generated.
1	Periodic Interval x event is enabled and will be generated.

19.8.8 Interrupt Enable Clear - MODE0

Name: INTENCLR

Offset: 0x06

Reset: 0x00

Property: Write-Protected

32-bit ARM-Based Microcontrollers

Bit	7	6	5	4	3	2	1	0
	OUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUT[31:0]: PORT Data Output Value

For pins configured as outputs via the Data Direction register (DIR), these bits set the logical output drive level.

For pins configured as inputs via the Data Direction register (DIR) and with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN), these bits will set the input pull direction.

Value	Description
0	The I/O pin output is driven low, or the input is connected to an internal pull-down.
1	The I/O pin output is driven high, or the input is connected to an internal pull-up.

23.8.6 Data Output Value Clear

This register allows the user to set one or more output I/O pin drive levels low, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Set (OUTSET) registers.

Name: OUTCLR

Offset: 0x14

Reset: 0x00000000

Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	OUTCLR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	OUTCLR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	OUTCLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	OUTCLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTCLR[31:0]: PORT Data Output Value Clear

Writing '0' to a bit has no effect.

Writing '1' to a bit will clear the corresponding bit in the OUT register. Pins configured as outputs via the Data Direction register (DIR) will be set to low output drive level. Pins configured as inputs via DIR and

with pull enabled via the Pull Enable bit in the Pin Configuration register (PINCFG.PULLEN) will set the input pull direction to an internal pull-down.

Value	Description
0	The corresponding I/O pin in the PORT group will keep its configuration.
1	The corresponding I/O pin output is driven low, or the input is connected to an internal pull-down.

23.8.7 Data Output Value Set

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

Name: OUTSET

Offset: 0x18

Reset: 0x00000000

Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	OUTSET[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	OUTSET[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	OUTSET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	OUTSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTSET[31:0]: PORT Data Output Value Set

Writing '0' to a bit has no effect.

Writing '1' to a bit will set the corresponding bit in the OUT register, which sets the output drive level high for I/O pins configured as outputs via the Data Direction register (DIR). For pins configured as inputs via Data Direction register (DIR) with pull enabled via the Pull Enable register (PULLEN), these bits will set the input pull direction to an internal pull-up.

Value	Description
0	The corresponding I/O pin in the group will keep its configuration.
1	The corresponding I/O pin output is driven high, or the input is connected to an internal pull-up.

Bit 1 – ERR: Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF: Overflow Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

30.8.10 Interrupt Flag Status and Clear

Name: INTFLAG

Offset: 0x0E

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0	SYNCRDY		ERR	OVF
Access			R/W	R/W	R/W		R/W	R/W
Reset			0	0	0		0	0

Bits 5,4 – MCx: Match or Capture Channel x [x = 1..0]

This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.

Writing a '0' to one of these bits has no effect.

Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag

In capture operation, this flag is automatically cleared when CCx register is read.

Bit 3 – SYNCRDY: Synchronization Ready Interrupt Enable

Writing a '0' to this bit has no effect.

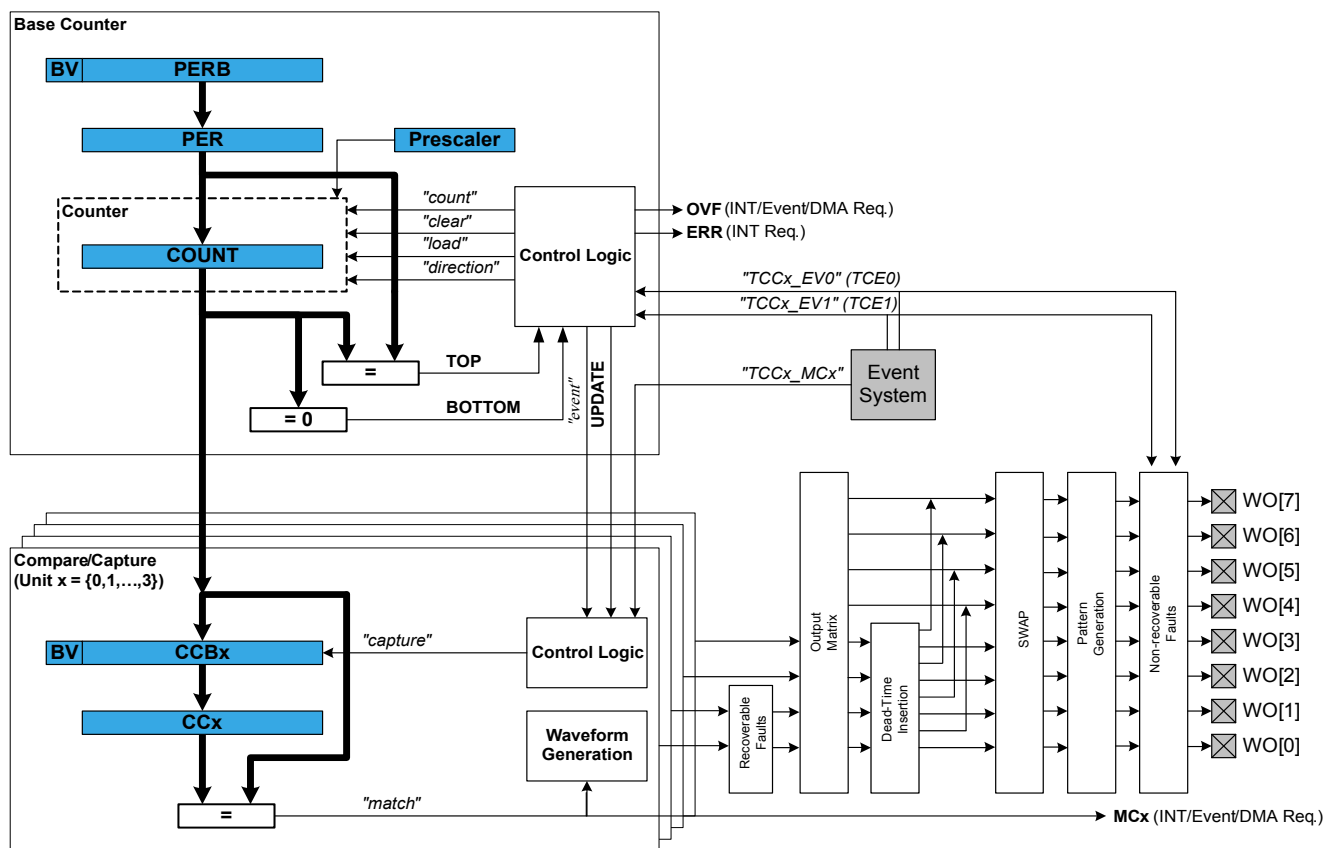
Writing a one to this bit will clear the Synchronization Ready Interrupt Disable/Enable bit, which disables the Synchronization Ready interrupt.

Value	Description
0	The Synchronization Ready interrupt is disabled.
1	The Synchronization Ready interrupt is enabled.

- Input events:
 - Two input events for counter
 - One input event for each channel
- Output events:
 - Three output events (Count, Re-Trigger and Overflow) available for counter
 - One Compare Match/Input Capture event output for each channel
- Interrupts:
 - Overflow and Re-Trigger interrupt
 - Compare Match/Input Capture interrupt
 - Interrupt on fault detection
- Can be used with DMA and can trigger DMA transactions

31.3 Block Diagram

Figure 31-1. Timer/Counter for Control Applications - Block Diagram



31.4 Signal Description

Pin Name	Type	Description
TCCx/WO[0]	Digital output	Compare channel 0 waveform output
TCCx/WO[1]	Digital output	Compare channel 1 waveform output

Table 31-1. Timer/Counter for Control Applications - Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the waveform generator mode in Waveform Output Generation Operations .
ZERO	The counter reaches ZERO when it contains all zeroes.
MAX	The counter reaches maximum when it contains all ones.
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source.
Counter	The clock control is handled externally (e.g. counting external events).
CC	For compare operations, the CC are referred to as "compare channels." For capture operations, the CC are referred to as "capture channels."

Each TCC instance has up to four compare/capture channels (CCx).

The counter register (COUNT), period registers with buffer (PER and PERB), and compare and capture registers with buffers (CCx and CCBx) are 16- or 24-bit registers, depending on each TCC instance. Each buffer register has a buffer valid (BUFV) flag that indicates when the buffer contains a new value.

Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached TOP or ZERO. In either case, the TCC can generate interrupt requests, request DMA transactions, or generate events for the Event System. In waveform generator mode, these comparisons are used to set the waveform period or pulse width.

A prescaled generic clock (GCLK_TCCx) and events from the event system can be used to control the counter. The event system is also used as a source to the input capture.

The Recoverable Fault Unit enables event controlled waveforms by acting directly on the generated waveforms of the TCC compare channels output. These events can restart, halt the timer/counter period, shorten the output pulse active time, or disable waveform output as long as the fault condition is present. This can typically be used for current sensing regulation, and zero-crossing and demagnetization re-triggering.

The MCE0 and MCE1 event sources are shared with the Recoverable Fault Unit. Only asynchronous events are used internally when fault unit extension is enabled. For further details on how to configure asynchronous events routing, refer to *EVSYS – Event System*.

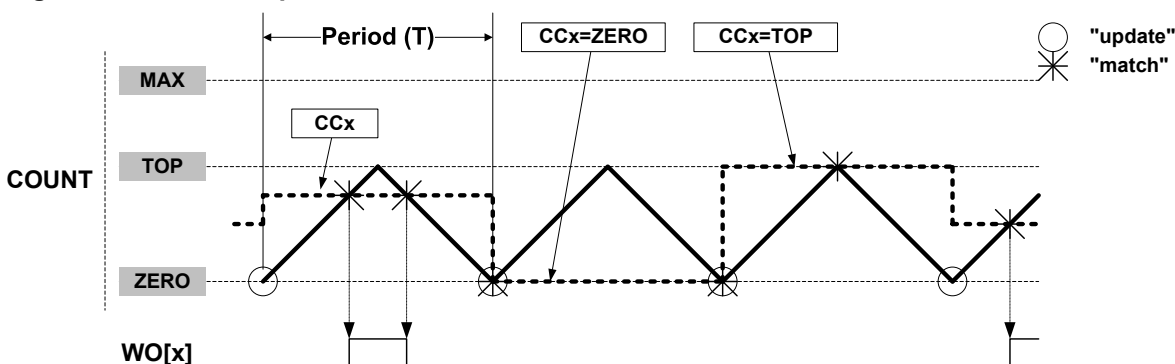
Recoverable fault sources can be filtered and/or windowed to avoid false triggering, for example from I/O pin glitches, by using digital filtering, input blanking, and qualification options. See also [Recoverable Faults](#).

In addition, six optional independent and successive units primarily intended for use with different types of motor control, ballast, LED, H-bridge, power converter, and other types of power switching applications, are implemented in some of TCC instances. See also [Figure 31-1](#).

The output matrix (OTMX) can distribute and route out the TCC waveform outputs across the port pins in different configurations, each optimized for different application types. The Dead-Time Insertion (DTI) unit splits the four lower OTMX outputs into two non-overlapping signals: the non-inverted low side (LS) and

In DSBOTH operation, a second update time occurs on TOP when circular buffer is enabled.

Figure 31-7. Dual-Slope Pulse Width Modulation



Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM (R_{PWM_DS}):

$$R_{PWM_DS} = \frac{\log(PER+1)}{\log(2)}.$$

The PWM frequency f_{PWM_DS} depends on the period setting (TOP) and the peripheral clock frequency f_{GCLK_TCC} , and can be calculated by the following equation:

$$f_{PWM_DS} = \frac{f_{GCLK_TCC}}{2N \cdot PER}$$

N represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency (f_{GCLK_TCC}) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width (P_{PWM_DS}) depends on the compare channel (CCx) register value and the peripheral clock frequency (f_{GCLK_TCC}), and can be calculated by the following equation:

$$P_{PWM_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK_TCC}}$$

N represents the prescaler divider used.

Note: In DSTOP, DSBOTTOM and DSBOTH operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB]=0, falling if CCx[MSB]=1.)

Related Links

[Circular Buffer](#)

Dual-Slope Critical PWM Generation

Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC_NUM/2) control the generated waveform output edge during down-counting.

32.6.3.15 PERR Error

This error exists for all pipes. It sets the PINTFLAG.PERR Interrupt, which triggers an interrupt if PINTFLAG.PERR is set. The user must check the PINTSMRY register to find out the pipe which can cause an interrupt.

A PERR error occurs if one of the error field in the STATUS_PIPE register in the Host pipe descriptor is set and the Error Count field in STATUS_PIPE (STATUS_PIPE.ERCNT) exceeds the maximum allowed number of Pipe error(s) as defined in Pipe Error Max Number field in CTRL_PIPE (CTRL_PIPE.PERMAX). Refer to section [STATUS_PIPE](#) register.

If one of the error field in the STATUS_PIPE register from the Host Pipe Descriptor is set and the STATUS_PIPE.ERCNT is less than the CTRL_PIPE.PERMAX, the STATUS_PIPE.ERCNT is incremented.

32.6.3.16 Link Power Management L1 (LPM-L1) Suspend State Entry and Exit as Host.

An EXTENDED LPM transaction can be transmitted by any enabled pipe. The PCFGn.PTYPE should be set to EXTENDED. Other fields as PCFG.PTOKEN, PCFG.BK and PCKSIZE.SIZE are irrelevant in this configuration. The user should also set the EXTREG.VARIABLE in the descriptor as described in [EXTREG](#) register.

When the pipe is configured and enabled, an EXTENDED TOKEN followed by a LPM TOKEN are transmitted. The device responds with a valid HANDSHAKE, corrupted HANDSHAKE or no HANDSHAKE (TIME-OUT).

If the valid HANDSHAKE is an ACK, the host will immediately proceed to L1 SLEEP and the PINTFLAG.TRCT0 is set. The minimum duration of the L1 SLEEP state will be the TL1RetryAndResidency as defined in the reference document "ENGINEERING CHANGE NOTICE, USB 2.0 Link Power Management Addendum". When entering the L1 SLEEP state, the CTRLB.SOFE is cleared, avoiding Start-of-Frame generation.

If the valid HANDSHAKE is a NYET PINTFLAG.TRFAIL is set.

If the valid HANDSHAKE is a STALL the PINTFLAG.STALL is set.

If there is no HANDSHAKE or corrupted HANDSHAKE, the EXTENDED/LPM pair of TOKENS will be transmitted again until reaching the maximum number of retries as defined by the CTRL_PIPE.PERMAX in the pipe descriptor.

If the last retry returns no valid HANDSHAKE, the PINTFLAGn.PERR is set, and the STATUS_BK is updated in the pipe descriptor.

All LPM transactions, should they end up with a ACK, a NYET, a STALL or a PERR, will set the PSTATUS.PFREEZE bit, freezing the pipe before a succeeding operation. The user should unfreeze the pipe to start a new LPM transaction.

To exit the L1 STATE, the user initiate a DOWNSTREAM RESUME by setting the bit CTRLB.RESUME or a L1 RESUME by setting the Send L1 Resume bit in CTRLB (CTRLB.L1RESUME). In the case of a L1 RESUME, the K STATE duration is given by the BESL bit field in the EXTREG.VARIABLE field. See [EXTREG](#).

When the host is in the L1 SLEEP state after a successful LPM transmitted, the device can initiate an UPSTREAM RESUME. This will set the Upstream Resume Interrupt bit in INTFLAG (INTFLAG.UPRSM). The host should proceed then to a L1 RESUME as described above.

After resuming from the L1 SLEEP state, the bit CTRLB.SOFE is set, allowing Start-of-Frame generation.

32-bit ARM-Based Microcontrollers

Bit	7	6	5	4	3	2	1	0
	BK1RDY	BK0RDY	STALLRQ1	STALLRQ0		CURBK	DTGLIN	DTGLOUT
Access	W	W	W	W		W	W	W
Reset	0	0	0	0		0	0	0

Bit 7 – BK1RDY: Bank 1 Ready Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.BK1RDY bit.

Bit 6 – BK0RDY: Bank 0 Ready Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.BK0RDY bit.

Bit 5 – STALLRQ1: STALL bank 1 Request Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.STALLRQ1 bit.

Bit 4 – STALLRQ0: STALL bank 0 Request Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.STALLRQ0 bit.

Bit 2 – CURBK: Current Bank Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.CURBK bit.

Bit 1 – DTGLIN: Data Toggle IN Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear EPSTATUS.DTGLIN bit.

Bit 0 – DTGLOUT: Data Toggle OUT Clear

Writing a zero to this bit has no effect.

Writing a one to this bit will clear the EPSTATUS.DTGLOUT bit.

32.8.3.3 EndPoint Status Set n

Name: EPSTATUSSETn

Offset: 0x105 + (n x 0x20)

Reset: 0x00

Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	BK1RDY	BK0RDY	STALLRQ1	STALLRQ0		CURBK	DTGLIN	DTGLOUT
Access	W	W	W	W		W	W	W
Reset	0	0	0	0		0	0	0

Bit 7 – BK1RDY: Bank 1 Ready Set

Writing a zero to this bit has no effect.

MUXPOS[4:0]	Group configuration	Description
0x03	PIN3	ADC AIN3 pin
0x04	PIN4	ADC AIN4 pin
0x05	PIN5	ADC AIN5 pin
0x06	PIN6	ADC AIN6 pin
0x07	PIN7	ADC AIN7 pin
0x08	PIN8	ADC AIN8 pin
0x09	PIN9	ADC AIN9 pin
0x0A	PIN10	ADC AIN10 pin
0x0B	PIN11	ADC AIN11 pin
0x0C	PIN12	ADC AIN12 pin
0x0D	PIN13	ADC AIN13 pin
0x0E	PIN14	ADC AIN14 pin
0x0F	PIN15	ADC AIN15 pin
0x10	PIN16	ADC AIN16 pin
0x11	PIN17	ADC AIN17 pin
0x12	PIN18	ADC AIN18 pin
0x13	PIN19	ADC AIN19 pin
0x14-0x17		Reserved
0x18	TEMP	Temperature reference
0x19	BANDGAP	Bandgap voltage
0x1A	SCALED COREVCC	1/4 scaled core supply
0x1B	SCALED IOVCC	1/4 scaled I/O supply
0x1C	DAC	DAC output
0x1D-0x1F		Reserved

33.8.9 Event Control

Name: EVCTRL

Offset: 0x14

Reset: 0x00

Property: Write-Protected

32-bit ARM-Based Microcontrollers

Writing a one to this bit will set the Synchronization Ready Interrupt Enable bit, which enables the Synchronization Ready interrupt.

Value	Description
0	The Synchronization Ready interrupt is disabled.
1	The Synchronization Ready interrupt is enabled.

Bit 2 – WINMON: Window Monitor Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the Window Monitor Interrupt bit and enable the Window Monitor interrupt.

Value	Description
0	The Window Monitor interrupt is disabled.
1	The Window Monitor interrupt is enabled.

Bit 1 – OVERRUN: Overrun Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the Overrun Interrupt bit and enable the Overrun interrupt.

Value	Description
0	The Overrun interrupt is disabled.
1	The Overrun interrupt is enabled.

Bit 0 – RESRDY: Result Ready Interrupt Enable

Writing a zero to this bit has no effect.

Writing a one to this bit will set the Result Ready Interrupt bit and enable the Result Ready interrupt.

Value	Description
0	The Result Ready interrupt is disabled.
1	The Result Ready interrupt is enabled.

33.8.12 Interrupt Flag Status and Clear

Name: INTFLAG

Offset: 0x18

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
					SYNCRDY	WINMON	OVERRUN	RESRDY
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – SYNCRDY: Synchronization Ready

This flag is cleared by writing a one to the flag.

This flag is set on a one-to-zero transition of the Synchronization Busy bit in the Status register (STATUS.SYNCBUSY), except when caused by an enable or software reset, and will generate an interrupt request if INTENCLR/SET.SYNCRDY is one.

Writing a zero to this bit has no effect.

Table 37-44. NVM Characteristics (Device Variant B and C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t _{FPP}	Page programming time	-	-	-	2.5	ms
t _{FRE}	Row erase time	-	-	-	1.2	ms
t _{FCE}	DSU chip erase time (CHIP_ERASE)	-	-	-	240	ms

37.12 Oscillators Characteristics

37.12.1 Crystal Oscillator (XOSC) Characteristics

37.12.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 37-45. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f _{CPXIN}	XIN clock frequency		-	-	32	MHz

37.12.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L + C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Table 37-46. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f _{OUT}	Crystal oscillator frequency		0.4	-	32	MHz
ESR	Crystal Equivalent Series Resistance Safety Factor = 3 The AGC doesn't have any noticeable impact on these measurements.	f = 0.455 MHz, C _L = 100pF XOSC.GAIN = 0	-	-	5.6K	Ω
		f = 2MHz, C _L = 20pF XOSC.GAIN = 0	-	-	416	
		f = 4MHz, C _L = 20pF XOSC.GAIN = 1	-	-	243	
		f = 8 MHz, C _L = 20pF XOSC.GAIN = 2	-	-	138	
		f = 16 MHz, C _L = 20pF XOSC.GAIN = 3	-	-	66	
		f = 32MHz, C _L = 18pF XOSC.GAIN = 4	-	-	56	
C _{XIN}	Parasitic capacitor load		-	5.9	-	pF

The SAM D21 oscillator is optimized for very low power consumption, hence close attention should be made when selecting crystals, see the table below for maximum ESR recommendations on 9pF and 12.5pF crystals.

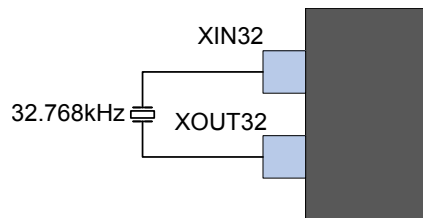
The Low-frequency Crystal Oscillator provides an internal load capacitance of typical values available in Table , *32kHz Crystal Oscillator Characteristics*. This internal load capacitance and PCB capacitance can allow to use a Crystal inferior to 12.5pF load capacitance without external capacitors as shown in the following figure.

Table 39-6. Maximum ESR Recommendation for 32.768kHz Crystal

Crystal C_L (pF)	Max ESR [k Ω]
12.5	313

Note: Maximum ESR is typical value based on characterization. These values are not covered by test limits in production.

Figure 39-7. External Real Time Oscillator without Load Capacitor



However, to improve Crystal accuracy and Safety Factor, it can be recommended by crystal datasheet to add external capacitors as shown in the next figure.

To find suitable load capacitance for a 32.768kHz crystal, consult the crystal datasheet.

Figure 39-8. External Real Time Oscillator with Load Capacitor

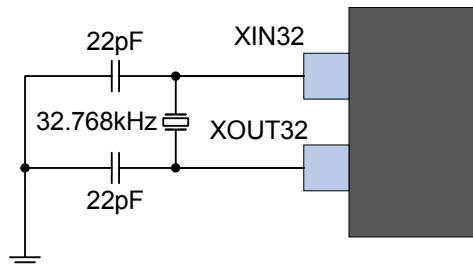


Table 39-7. External Real Time Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN32	Load capacitor 22pF ⁽¹⁾⁽²⁾	Timer oscillator input
XOUT32	Load capacitor 22pF ⁽¹⁾⁽²⁾	Timer oscillator output

1. These values are given only as typical examples.
2. Decoupling capacitor should be placed close to the device for each supply pin pair in the signal group.

Note: In order to minimize the cycle-to-cycle jitter of the external oscillator, keep the neighboring pins as steady as possible. For neighboring pin details, refer to the Oscillator Pinout section.

Related Links

if (SERCOM - INTFLAG.bit.PREC) SERCOM - INTFLAG.reg =
SERCOM_I2CS_INTFLAG_PREC;
SERCOM - INTFLAG.reg = SERCOM_I2CS_INTFLAG_AMATCH;

7 – PA24 and PA25 cannot be used as input when configured as GPIO with continuous sampling (cannot be read by PORT).

Errata reference: 12005

Fix/Workaround:

- Use PA24 and PA25 for peripherals or only as output pins.
- Or configure PA31 to PA24 for on-demand sampling (CTRL[31:24] all zeroes) and access the IN register through the APB (not the IOBUS), to allow waiting for on-demand sampling.

8 – The SYSTICK calibration value is incorrect.

Errata reference: 14154

Fix/Workaround:

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the SysTick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

9 – In Standby, Idle1 and Idle2 sleep modes the device might not wake up from sleep. An External Reset, Power on Reset or Watch Dog Reset will start the device again.

Errata reference: 13140

Fix/Workaround:

the SLEEPPRM bits in the NVMCTRL.CTRLB register must be written to 3 (NVMCTRL - CTRLB.bit.SLEEPPRM = 3) to ensure correct operation of the device. The average power consumption of the device will increase with 20uA compared to numbers in the electrical characteristics chapter.

10 – While the internal startup is not completed, PA07 pin is driven low by the chip. Then as all the other pins it is configured as an High Impedance pin.

Errata reference: 12118

Fix/Workaround:

None

11 – Digital pin outputs from Timer/Counters, AC (Analog Comparator), GCLK (Generic Clock Controller), and SERCOM (I2C and SPI) do not change value during standby sleep mode.

Errata reference: 12537

Fix/Workaround:

Set the voltage regulator in Normal mode before entering STANDBY sleep mode in order to keep digital pin output enabled. This is done by setting the RUNSTDBY bit in the VREG register.

12 – The I2S is non-functional.

Errata reference: 12275

Fix/Workaround:

None

13 – Pulldown functionality is not available on GPIO pin PA24 and PA25

Errata reference: 13883

6 – In two ramp mode, two events will be generated per cycle, one on each ramp's end. EVCTRL.CNTSEL.END cannot be used to identify the end of a double ramp cycle.

Errata reference: 12224

Fix/Workaround:

None

7 – If an input event triggered STOP action is performed at the same time as the counter overflows, the first pulse width of the subsequent counter start can be altered with one prescaled clock cycle.

Errata reference: 12107

Fix/Workaround:

None

8 – When the RUNSTDBY bit is written after the TCC is enabled, the respective TCC APB bus is stalled and the RUNDSTBY bit in the TCC CTRLA register is not enabled-protected.

Errata reference: 12477

Fix/Workaround:

None.

9 – TCC fault filtering on inverted fault is not working.

Errata reference: 12512

Fix/Workaround:

Use only non-inverted faults.

10 – When waking up from the STANDBY power save mode, the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER and SYNCBUSY.CCx bits may be locked to 1.

Errata reference: 12227

Fix/Workaround:

After waking up from STANDBY power save mode, perform a software reset of the TCC if you are using the SYNCBUSY.CTRLB, SYNCBUSY.STATUS, SYNCBUSY.COUNT, SYNCBUSY.PATT, SYNCBUSY.WAVE, SYNCBUSY.PER or SYNCBUSY.CCx bits

11 – When the Peripheral Access Controller (PAC) protection is enabled, writing to WAVE or WAVEB registers will not cause a hardware exception.

Errata reference: 11468

Fix/Workaround:

None

12 – If the MCx flag in the INTFLAG register is set when enabling the DMA, this will trigger an immediate DMA transfer and overwrite the current buffered value in the TCC register.

Errata reference: 12155

Fix/Workaround:

None

40.1.4.14 PTC

1 – WCOMP interrupt flag is not stable. The WCOMP interrupt flag will not always be set as described in the datasheet.

Errata reference: 12860

Fix/Workaround:

Do not use the WCOMP interrupt. Use the WCOMP event.

40.2 Device Variant B

The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

40.2.1 Die Revision E

40.2.1.1 Device

1 – The SYSTICK calibration value is incorrect.**Errata reference: 14155****Fix/Workaround:**

The correct SYSTICK calibration value is 0x40000000. This value should not be used to initialize the SysTick RELOAD value register, which should be initialized instead with a value depending on the main clock frequency and on the tick period required by the application. For a detailed description of the SYSTICK module, refer to the official ARM Cortex-M0+ documentation.

2 – Pulldown functionality is not available on GPIO pin PA24 and PA25**Errata reference: 15051****Fix/Workaround:**

None

3 – The TCC interrupt flags

INTFLAG.ERR,INTFLAG.DFS,INTFLAG.UFS,INTFLAG.CNT,INTFLAG.FAULTA,INTFLAG.FAULTB,INTFLAG.FAULT0,INTFLAG.FAULT1 are not always properly set when using asynchronous TCC features.

Errata reference: 15179**Fix/Workaround:**

Do not use these flags when using asynchronous TCC features.

4 – On pin PA24 and PA25 the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled except for USB.**Errata reference: 12368****Fix/Workaround:**

For pin PA24 and PA25, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

5 – If APB clock is stopped and GCLK clock is running, APB read access to read-synchronized registers will freeze the system. The CPU and the DAP AHB-AP are stalled, as a consequence debug operation is impossible.**Errata reference: 10416****Fix/Workaround:**

Do not make read access to read-synchronized registers when APB clock is stopped and GCLK is running. To recover from this situation, power cycle the device or reset the device using the RESETN pin.

32-bit ARM-Based Microcontrollers

Abbreviation	Description
INT	Interrupt
MBIST	Memory built-in self-test
MEM-AP	Memory Access Port
MTB	Micro Trace Buffer
NMI	Non-maskable interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
NVMCTRL	Non-Volatile Memory Controller
OSC	Oscillator
PAC	Peripheral Access Controller
PC	Program Counter
PER	Period
PM	Power Manager
POR	Power-on reset
PORT	I/O Pin Controller
PTC	Peripheral Touch Controller
PWM	Pulse Width Modulation
RAM	Random-Access Memory
REF	Reference
RTC	Real-Time Counter
RX	Receiver/Receive
SERCOM	Serial Communication Interface
SMBus™	System Management Bus
SP	Stack Pointer
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SUPC	Supply Controller
SWD	Serial Wire Debug
TC	Timer/Counter
TCC	Timer/Counter for Control Applications
TRNG	True Random Number Generator
TX	Transmitter/Transmit

43. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

43.1 Rev. A – 01/2017

General	<ul style="list-style-type: none"> • Template: Updated from Atmel to Microchip template. • Document number: Changed from the Atmel 42181 to Microchip xxxxx. • Document revision letter reset to A. • ISBN number added.
Electrical Characteristics	<ul style="list-style-type: none"> • Die Revision F final characterization added. • Power Consumption: Added Standby typical numbers for Device Variant C / Die Revision F. • Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics: Added characterization data for Device Variant C / Die Revision F.
Errata	<ul style="list-style-type: none"> • New errata added: <ul style="list-style-type: none"> – B – Device Variant A: Errata reference 15625, 15683, 15753 added. – Device Variant B: Errata reference 15625, 15683, 15753 added. – Device Variant C: Errata reference 15625, 15683, 15753 added.
Appendix A. Electrical Characteristics at 125°C	<ul style="list-style-type: none"> • Die Revision F final characterization is preliminary. • Power Consumption: Added Standby typical numbers for Device Variant C / Die Revision F. • Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics: Added characterization data for Device Variant C / Die Revision F.

43.2 Rev. O – 12/2016

General	<ul style="list-style-type: none"> • Introduced Device Variant C.
Electrical Characteristics	<ul style="list-style-type: none"> • Die Revision F characterization is preliminary. • Power Consumption: Added Standby typical numbers for Device Variant C / Die Revision F. • Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics: Added characterization data for Device Variant C / Die Revision F.
Appendix A. Electrical Characteristics at 125°C	<ul style="list-style-type: none"> • Die Revision F characterization is preliminary. • Power Consumption: Added Standby typical numbers for Device Variant C / Die Revision F. • Fractional Digital Phase Locked Loop (FDPLL96M) Characteristics: Added characterization data for Device Variant C / Die Revision F.

43.12 Rev. E – 02/2015

Description:	
	CoreMark score updated from 2.14 to 2.46 CoreMark/MHz.
Ordering Information:	
	<p>Added Ordering codes for Device Variant B.</p> <p>Added 125°C ordering codes for QFN and TQFP package options: SAM D21E, SAM D21G and SAM D21J.</p> <p>Added WLCSP package option for SAM D21G.</p> <p>Added UFBGA package option for SAM D21J.</p>
Pinout:	
	Added pinout figures for UFBGA64 and WLCSP45 .
Product Mapping:	
	Updated Product Mapping figure with Internal RWW section block for Device Variant B.
Memories:	
	Physical Memory Map : Added start address for Internal Read While Write (RWW) section for Device Variant B.
Processor And Architecture:	
	Cortex M0+ Configuration : Removed green connection dots between DMAC Data and AHB-APB Bridge A and Bridge B.
NVMCTRL – Non-Volatile Memory Controller:	
	<p>Introducing Read While Write (RWW) feature for Device Variant B.</p> <p>Updated and New sections:</p> <p>Overview</p> <p>Features</p> <p>Block Diagram</p> <p>NVM Read</p> <p>RWWEE Read</p> <p>NVM Write</p> <p>Erase Row</p> <p>Memory Organization: Figure 22-2 updated.</p> <p>Register Summary and Register Description: PARAM: Added RWWEEP[12:0] bits for Device Variant B.</p>
PORT - I/O Pin Controller:	