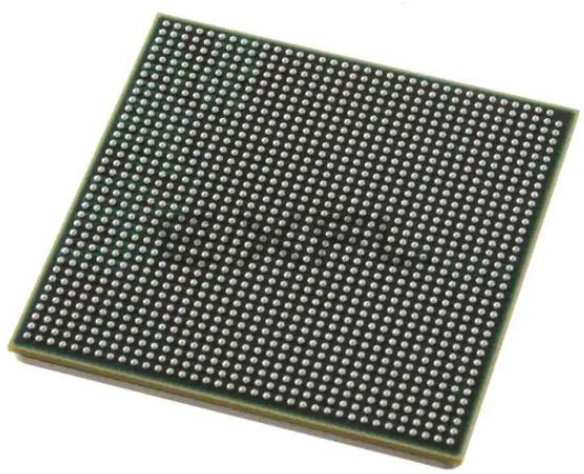

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500mc
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.5GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (5), 10Gbps (1)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.5V, 1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p3041nxn7pnc

Erratum A-007207: TBI LINK STATUS SGMII STAYS UP

PB #16224

Affected Devices: P2040 P2041 P3041 P4080 P5020 P5040

May 2014

Erratum – A-007207

Erratum – A-007207

TBI link status may stay “up” after SGMII electrical idle detected

Devices: P2040 P2041 P3041 P4080 P5020 P5040

Description:

The TBI Status Register (SR) contains a link status bit (TBI SR [Link Status]) that represents the current state of the SGMII link. If Auto-Negotiation (AN) is disabled, the TBI link status bit should become a b’1 indicating the link is up after recognizing IDLE sequences, and stay at b’1 as long as valid data is received & the TBI is not reset. TBI link status bit should become a b’0 indicating the link is down after several invalid characters are received or the TBI is reset. If AN is enabled, the TBI link status bit does not become set to b’1 until auto-negotiation is complete (TBI CR [AN DONE]=1), but the same conditions as AN disabled then apply for the TBI link status bit to get cleared to b’0.

An electrical idle (common mode) condition on the SGMII link results in the reception of invalid data, and should cause the TBI link status bit to get cleared. If the transition from active to common mode takes enough time that the Rx is able to recognize at least 4 more K28.5 characters (for IDLE sequences, 70-80 UI), the portion of the design intended to detect the link down condition may shut off before the link down condition is actually reflected in the TBI.

This premature shutdown may cause the TBI link status to remain set to a b’1 indicating the link is up. This 'stuck at 1' condition would persist until valid K28.5 characters are received again.

Erratum – A-007207

TBI link status may stay “up” after SGMII electrical idle detected (cont. 2 of 4)

Impact:

If the system never enters SGMII electrical idle, or if the transition from active to common mode takes less than 40 UI (~32 ns), then there is no impact and the false link up scenario does not occur.

If the system can generate an SGMII electrical idle condition as described above, then the TBI status may stay stuck at 1 while the link is down and does not transition to 0 until valid K28.5 characters are received again.

Erratum – A-007207

TBI link status may stay “up” after SGMII electrical idle detected (cont. 3 of 4)

Workaround:

If TBI SR[Link Status] = 0, the link is down.

For affected systems, in addition to examining the TBI link status, examine the SerDes electrical idle state. The link is actually down if either the TBI link status is cleared or the SerDes lane receive electrical idle is detected.

SerDes electrical idle detected is BnGCRm1[REIDL] = 1 for bank n, lane m.

Example pseudo-code:

```
if        (BnGCRm1[REIDL] == b'1)
          OR
          (TBI SR[LINK STATUS] == b'0)
{
          LINK is DOWN
}
```

Erratum – A-007207

TBI link status may stay “up” after SGMII electrical idle detected (cont. 4 of 4)

Disposition:

No plans to fix.

Steps to Read TBI Status and Receive Electrical Idle

Action	Register
write	MIIMCOM[Read Cycle] = 1
write	MIIMADD[PHY Address] = value from TBIPA for dTSEC used
write	MIIMADD[Register Address] = 1 for TBI Status Register (SR)
write	MIIMCOM[Read Cycle] = 0 to ensure 0 -> 1 transition for non-stale data
write	MIIMCOM[Read Cycle] = 1
read	MIIMSTAT[PHY Status] for value in TBI SR. Check TBI SR[Link Status]. ‘0’ means link is down.
read	BnGCRm1[REIDL]where *m* means bank and *n* means lane. ‘1’ means link is down. ‘0’ means non-electrical idle state but could be receiving invalid symbols which would result in a link down.


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