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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, PWM, WDT
Number of I/O	63
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51em256cllr

Table 1. MCF51EM256 Series Features by MCU and Package (continued)

Feature	MCF51EM256	MCF51EM128
MTIM1 (8-bit)	Yes	
MTIM2 (8-bit)	Yes	
MTIM3 (16-it)	Yes	
TPM channels	2	
PDB	Yes	
XOSC1[4]	Yes	
XOSC2[5]	Yes	

1 Each differential channel is comprised of 2 pin inputs
2 RGPIO is muxed with standard Port I/O
3 Port I/O count does not include the ouput only PTC2/BKGD/MS.
4 IRTC crystal input and possible crystal input to the ICS module
5 Main external crystal input for the ICS module

1.2 Block Diagram

Figure 1 shows the connections between the MCF51EM256 series pins and modules.

1.3 Features

Table 2 describes the functional units of the MCF51EM256 series.

Table 2. MCF51EM256 Series Functional Units

Unit	Function
ADC (analog-to-digital converter)	Measures analog voltages at up to 16 bits of resolution. Each ADC has up to four differential and 24 single-ended inputs.
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
CF1 CORE (V1 ColdFire core) with MAC unit	Executes programs, handles interrupts and containes multiply-accumulate hardware (MAC).
PRACMP1, PRACMP2 (comparators)	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (computer operating poperly)	Software watchdog
IRQ (interrupt request)	Single pin high priority interrupt (part of the V1 ColdFire core)
CRC (cyclic Redundancy Check)	High-speed CRC calculation
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
FLASH (flash memory)	Provides storage for program code, constants and variables
IIC (inter-integrated circuits)	Supports standard IIC communications protocol and SMBus
INTC (interrupt controller)	Controls and prioritizes all device interrupts
KBI1 & KBI2	Keyboard Interfaces 1 and 2
LCD	Liquid crystal display driver
LVD (low voltage detect)	Provides an interrupt to the CF1CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event
ICS (internal clock source)	Provides clocking options for the device, including a three frequency-locked loops (FLLs) for multiplying slower reference clock sources
IRTC (independent real-time clock)	The independent real time clock provides an independent time-base with optional interrupt, battery backup and tamper protection
VREF (voltage reference)	The voltage reference output is available for both on and off-chip use
MTIM1, MTIM2 (modulo timers)	8-bit modulo timers with configurable clock inputs and interrupt generation on overflow
MTIM3 (modulo timer)	16-bit modulo timer with configurable clock inputs and interrupt generation on overflow
PDB (programmable delay block)	This timer is optimized for scheduling ADC conversions
RAM (random-access memory)	Provides stack and variable storage
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds and is used to implement GPIO functionality for PTA and PTB.

  - 6 µs typical wakeup time from stop3 mode
- Clock source options
  - Two independent oscillators (XOSC1 and XOSC2) — loop-control Pierce oscillator; 32.768 kHz crystal or ceramic resonator. XOSC1 nominally supports the independent real time clock, and can be powered by a separate battery backup. XOSC2 is the primary external clock source for the ICS
  - Internal clock source (ICS) — internal clock source module containing a frequency-locked-loop (FLL) controlled by internal or external reference (XOSC1 or XOSC2); precision trimming of internal reference allowing 0.2% resolution and typical 0.5% to –1% deviation over temperature and voltage; supporting CPU frequencies from 4 kHz to 50 MHz
- System protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
  - Low voltage detection with reset or interrupt; selectable trip points; seperate low voltage warning with optional interrupt; selectable trip points
  - Illegal opcode and illegal address detection with reset
  - Flash block protection for each array to prevent accidental write/erasure
  - Hardware CRC module to support fast cyclic redundancy checks
- Development support
  - Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection supports same electrical interface used by the S08 family debug modules
  - Real-time debug support with six hardware breakpoints (4 PC, 1 address and 1 data)
  - On-chip trace buffer provides programmable start/stop recording conditions
- Peripherals
  - **ADC16** — 4 analog-to-digital converters; the 100 pin version of the device has 1 dedicated differential channel and 1 dedicated single-ended channel per ADC, along with 3 muxed single-ended channels per ADC. The ADCs have 16-bit resolution, range compare function, 1.7 mV/°C temperature sensor, internal bandgap reference channel, operate in stop3 and are fully functional from 3.6 V to 1.8 V
  - **PDB** — Programmable delay block with 16-bit counter and modulus and 3-bit prescaler; 8 trigger outputs for ADC16 modules (2 per ADC); provides periodic coordination of ADC sampling sequence with programmable sequence completion interrupt
  - **IRTC** — Ultra-low power independent real time clock with calendar features (IRTC); runs in all MCU modes; external clock source with trim capabilities (XOSC1); independent voltage source runs IRTC when MCU is powered-down; tamper detection and indicator; battery monitor output to ADC; unaffected by MCU resets
  - **PRACMPx** — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to programmable internal reference voltage; operation in stop3
  - **LCD** — up to 288 segments (8 × 36); 160 segments (4 × 40); internal charge pump and option to provide internal reference voltage that can be trimmed for contrast control; flexible

Table 3. Orderable Part Number Summary

Freescale Part Number	Flash / SRAM (KB)	Package	Temperature
MCF51EM256CLL	256/16	100-Pin LQFP	–40°C to 85°C
MCF51EM256CLK	256/16	80-Pin LQFP	–40°C to 85°C
MCF51EM128CLL	128/16	100-Pin LQFP	–40°C to 85°C
MCF51EM128CLK	128/16	80-Pin LQFP	–40°C to 85°C

1.5.2 Pinout: 100-Pin LQFP

Figure 3 shows the pinout configuration for the 100-pin LQFP. Pins which are blacked out do not have an equivalent pin on the 80-pin LQFP package.

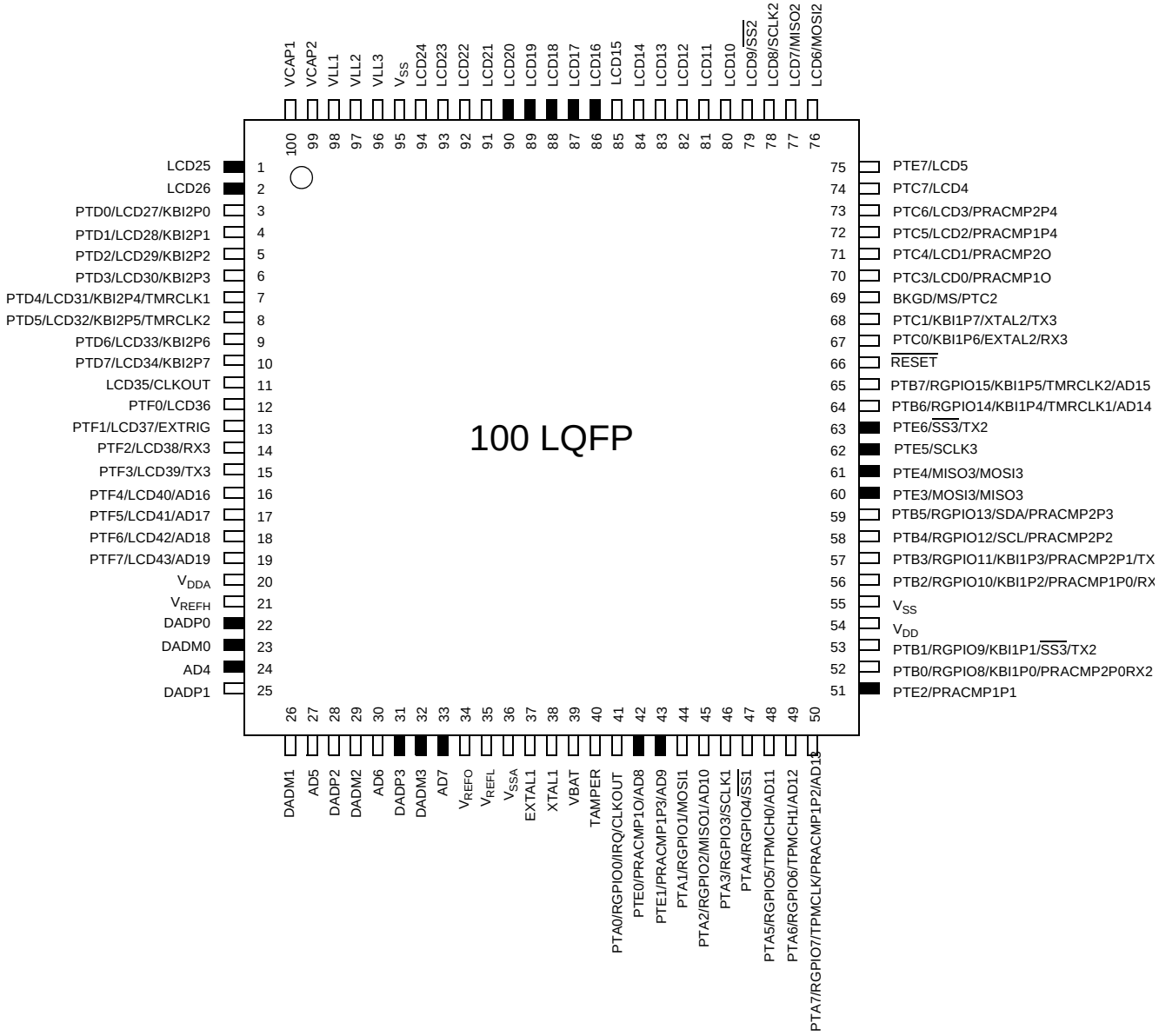

Figure 3. 100-Pin LQFP Pinout

Table 4 shows the package pin assignments.

Table 4. MCF51EM256 Series Package Pin Assignments

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
1	—	LCD25				
2	—	LCD26				
3	1	PTD0	LCD27	KBI2P0		
4	2	PTD1	LCD28	KBI2P1		
5	3	PTD2	LCD29	KBI2P2		
6	4	PTD3	LCD30	KBI2P3		
7	5	PTD4	LCD31	KBI2P4	TMRCLK1	
8	6	PTD5	LCD32	KBI2P5	TMRCLK2	
9	7	PTD6	LCD33	KBI2P6		
10	8	PTD7	LCD34	KBI2P7		
11	9	LCD35	CLKOUT			
12	10	PTF0	LCD36			
13	11	PTF1	LCD37		EXTRIG	
14	12	PTF2	LCD38		RX3	
15	13	PTF3	LCD39		TX3	
16	14	PTF4	LCD40		AD16	
17	15	PTF5	LCD41		AD17	
18	16	PTF6	LCD42		AD18	
19	17	PTF7	LCD43		AD19	
20	18	V_{DDA}				
21	19	V_{REFH}				
22	—	DADP0				
23	—	DADM0				
24	—	AD4				
25	20	DADP1				
26	21	DADM1				
27	22	AD5				
28	23	DADP2				
29	24	DADM2				
30	25	AD6				
31	—	DADP3				
32	—	DADM3				

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
58	47	PTB4/RGPIO12	SCL	PRACMP2P2		RGPIO_ENB is used to select between standard GPIO and RGPIO
59	48	PTB5/RGPIO13	SDA	PRACMP2P3		
60	—	PTE3	MOSI3	MISO3		
61	—	PTE4	MISO3	MOSI3		Open Drain
62	—	PTE5	SCLK3			Open Drain
63	—	PTE6	$\overline{SS3}$	TX2		Open Drain
64	49	PTB6/RGPIO14	KBI1P4	TMRCLK1	AD14	RGPIO_ENB is used to select between standard GPIO and RGPIO
65	50	PTB7/RGPIO15	KBI1P5	TMRCLK2	AD15	
66	51	$\overline{RESET}$				This pin is an open drain device and has an internal pullup. There is no clamp diode to V_{DD}.
67	52	PTC0	KBI1P6	EXTAL2	RX3	
68	53	PTC1	KBI1P7	XTAL2	TX3	
69	54	BKGD/MS	PTC2			This pin has an internal pullup. PTC2 can only be programmed as an output.
70[1]	55[1]	PTC3	LCD0	PRACMP1O		
71[1]	56[1]	PTC4	LCD1	PRACMP2O		
72[1]	57[1]	PTC5	LCD2		PRACMP1P4	
73[1]	58[1]	PTC6	LCD3		PRACMP2P4	
74[1]	59[1]	PTC7	LCD4			
75[1]	60[1]	PTE7	LCD5			
76[1]	61[1]	LCD6	MOSI2			
77[1]	62[1]	LCD7	MISO2			
78[1]	63[1]	LCD8	SCLK2			
79[1]	64[1]	LCD9	$\overline{SS2}$			
80	65	LCD10				
81	66	LCD11				
82	67	LCD12				
83	68	LCD13				
84	69	LCD14				
85	70	LCD15				
86	—	LCD16				

Table 4. MCF51EM256 Series Package Pin Assignments (continued)

100 LQFP	80 LQFP	Default Function	ALT1	ALT2	ALT3	Comment
87	—	LCD17				
88	—	LCD18				
89	—	LCD19				
90	—	LCD20				
91	71	LCD21				
92	72	LCD22				
93	73	LCD23				
94	74	LCD24				
95	75	V_{SS}				
96	76	VLL3				
97	77	VLL2				
98	78	VLL1				
99	79	VCAP2				
100	80	VCAP1				

[1] These pins that are shared with the LCD are open-drain by default if not used as LCD pins. To configure this pins as full complementary drive outputs, you must have the LCD modules bits configured as follow: FCDEN =1, VSUPPLY = 11 and RVEN = 0. The Input levels and internal pullup resistors are referenced to VLL3. Referer to the LCD chapter for further information.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51EM256/128 series microcontrollers, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 6 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 4.0	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins except PTB1 and PTB3)[1, 2, 3]	I_D	±25	mA
Instantaneous maximum current Single pin limit (applies to PTB1 and PTB3)[4, 5, 6]	I_D	±50	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

4 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 85	°C
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance [1,2,3,4] 100-pin LQFP 1s 2s2p 80-pin LQFP 1s 2s2p	θ_{JA}	 54 42 55 42	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layers board, two signal and two power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Machine Model (MM)	V_{MM}	±200	—	V
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V
4	Latch-up Current at T_A = 85 °C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter		Symbol	Min	Typical[1]	Max	Unit
1	P	Operating voltage	Digital supply — 50 MHz operation	V_{DD}	2.5	—	3.6	V
			Digital supply[2] — 20 MHz maximum operation	V_{DD}	1.8	—	3.6	
2	P	Analog supply		V_{DDA}	1.8	—	3.6	V
3	D	Battery supply		V_{BAT}	2.2	3	3.3	V
4	P	Bandgap voltage reference[3]		V_{BG}	1.15	1.17	1.18	V
5	C	Output high voltage	PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], low-drive strength. $V_{DD} \geq 1.8$ V, I_{Load} = –0.6 mA	V_{OH}	V_{DD} – 0.5	—	—	V
	P		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 2.7$ V, I_{Load} = –10 mA					
	C		PTA[7:0], PTB[7:0], PTC[2:0], PTE[6:0], high-drive strength. $V_{DD} \geq 1.8$ V, I_{Load} = –3 mA					
6	C	Output high voltage	PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, low drive strength. VDD ≥ 1.8 V, I_{Load} = –0.5 mA	V_{OH}	V_{DD} – 0.5	—	—	V
	P		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 2.7$ V, I_{Load} = –3 mA					
	C		PTC[7:3], PTD[7:0], PTE7, PTF[7:0], LCD35/CLKOUT, MOSI2, MISO2, SCK2, SS2, high-drive strength. $V_{DD} \geq 1.8$ V, I_{Load} = –1 mA					
7	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	100	mA

Table 11. Supply Current Characteristics

Num	C	Parameter		Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	25.165 MHz	RI_{DD}	3	66.2	100	mA	–40 to 85°C
	T		20 MHz			55.3	—		
	T		8 MHz			23.9	—		
	T		1 MHz			4.56	—		
2	C	Run supply current FEI mode, all modules off	25.165 MHz	RI_{DD}	3	55.1	56	mA	–40 to 85°C
	T		20 MHz			46.6	—		
	T		8 MHz			19.9	—		
	T		1 MHz			3.92	—		
3	T	Run supply current LPS=0, all modules off	16 kHz FBILP	RI_{DD}	3	239	—	µA	—
	T		16 kHz FBELP			249	—		
4	T	Run supply current LPS = 1, all modules off, running from flash	16 kHz FBELP	RI_{DD}	3	50	—	µA	—
5	C	Wait mode supply current FEI mode, all modules off	25.165 MHz	WI_{DD}	3	51.1	69	mA	–40 to 85°C
	T		20 MHz			42.6	—		
	T		8 MHz			18.8	—		
	T		1			3.69	—		
6	T	Wait mode supply current LPRS = 1, all mods off		WI_{DD}	3	1	—	µA	—
7	P	Stop2 mode supply current		$S2I_{DD}$	3	0.576	30	µA	–40 to 85°C
	C				2		16		
8	P	Stop3 mode supply current		$S3I_{DD}$	3	1.05	45	µA	–40 to 85°C
	C				2		27		
9	T	LVD adder to stop3, stop2 (LVDE = LVDSE = 1)		$S3I_{DDLVD}$	3	120	—	µA	—
10	T	Voltage reference adder to stop3	Low power mode	$S3I_{DDLVD}$	3	90	—	µA	—
			Tight regulation mode			270			
11	T	PRACMP adder to stop3	PRG disabled	$S3I_{DDLVD}$	3	13	—	µA	—
			PRG enabled			29			
12	T	LCD adder to stop3, stop2, VIREG enabled, 1/4 duty cycle, 4x39 configuration for 156 segments, 32Hz frame rate, no LCD glass connected		$S3I_{DDLVD}$	3	1.3	—	µA	—
13	C	Adder to stop3 for oscillator enabled[2] (ERCLKEN =1 and EREFSTEN = 1)		$S3I_{DDOSC}$	3	5		µA	—

Table 11. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max	Unit	Temp (°C)
14	P	IRTC supply current[3,4,5]	I_{DD-BAT}		1.5	5	µA	–40 to 85°C

1 Typicals are measured at 25 °C.

2 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

3 This is the current consumed when the IRTC is being powered by the V_{BAT}.

4 The IRTC power source depends on the MCU configuration and V_{DD} voltage level. Refer to reference manual for further information.

5 The IRTC current consumption includes the IRTC XOSC1.

Table 13. 16-bit ADC Operating Conditions

Num	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
5	Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
6	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
7	Input Capacitance	16-bit modes 8/10/12-bit modes	C_{ADIN}	—	8 4	10 5	pF	
8	Input Resistance		R_{ADIN}	—	2	5	kΩ	
9	Analog Source Resistance	16 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz	R_{AS}	— — —	— — —	0.5 1 2	kΩ	External to MCU Assumes ADLSMP=0
10		13/12 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	1 2 5		
11		11/10 bit modes f_{ADCK} > 8MHz 4MHz < f_{ADCK} < 8MHz f_{ADCK} < 4MHz		— — —	— — —	2 5 10		
12		9/8 bit modes f_{ADCK} > 8MHz f_{ADCK} < 8MHz		— —	— —	5 10		
13	ADC Conversion Clock Freq.	ADLPC = 0, ADHSC = 1	f_{ADCK}	1.0	—	8	MHz	
14		ADLPC = 0, ADHSC = 0		1.0	—	5		
15		ADLPC = 1, ADHSC = 0		1.0	—	2.5		

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

2.9 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits. XOSC1 operates only in low power low range mode. XOSC2 operates in all the power and range modes.

Table 16. XOSC Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 16 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO = 0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range (RANGE = 1, HGO = X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 600 400 5 15	 — — — —	ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode FBE or FBELP mode	f_{extal}	 0.03125 0	 — —	 50.33 50.33	 MHz MHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

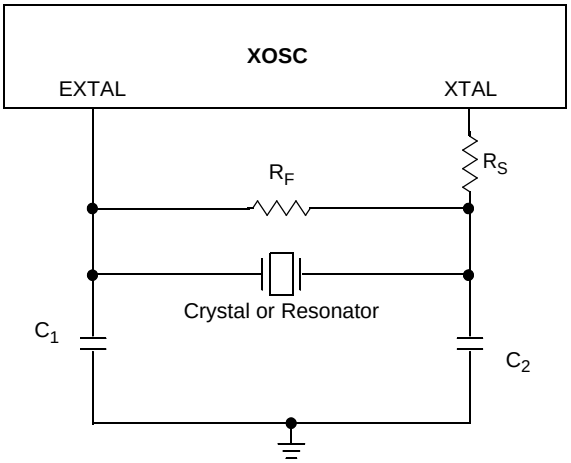

Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

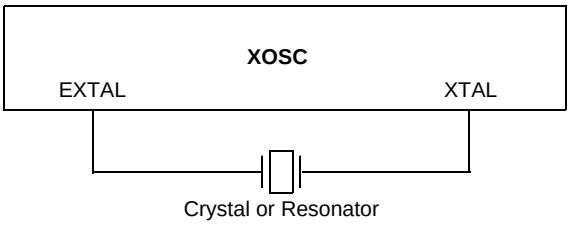

Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Gain

2.10 Internal Clock Source (ICS) Characteristics

Table 17. ICS Frequency Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at V_{DD} = 3.6 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	P	Internal reference frequency — user trimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_u}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	P		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
	P		High range (DRS = 10)		—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$

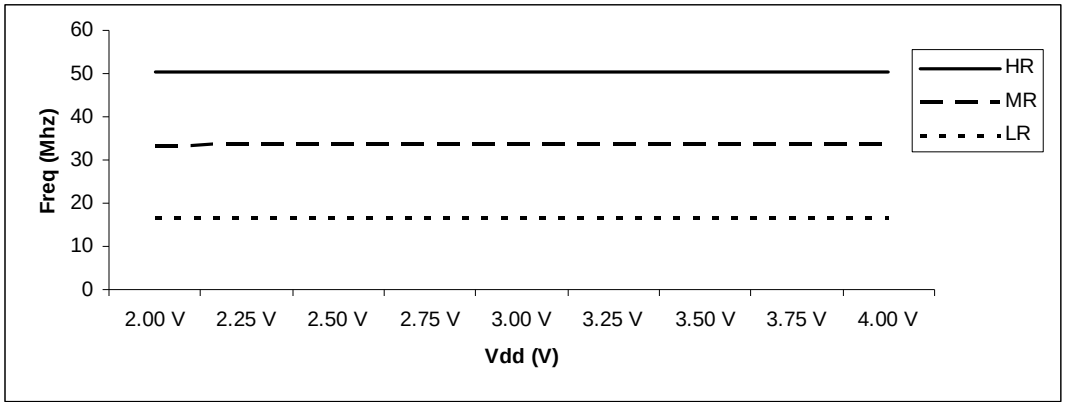

Figure 14. Deviation of DCO Output from Trimmed Frequency (50.33 MHz, 25 °C)

2.11 LCD Specifications

Table 18. LCD Electricals, 3 V Glass

N	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	D	LCD frame frequency	f_{Frame}	28	30	58	Hz
2	D	LCD charge pump capacitance	C_{LCD}		100	100	nF
3	D	LCD bypass capacitance	C_{BYLCD}		100	100	nF
4	D	LCD glass capacitance	C_{glass}		2000	8000	pF
5	D	V_{IREG} HRefSel = 0	V_{IREG}	.89	1.00	1.15	V
6		V_{IREG} HRefSel = 1		1.49	1.67	1.85[1]	
7	D	V_{IREG} trim resolution	Δ_{RTRIM}	1.5			% V_{IREG}
8	D	V_{IREG} ripple HRefSel = 0		—		0.1	V
		V_{IREG} ripple HRefSel = 1				0.15	
9	D	V_{IREG} current adder RVEN = 1	I_{VIREG}	—	1[2]		µA
10	D	V_{LCD} buffered adder[3]	I_{Buff}	—	1		µA

1 V_{IREG} Max can not exceed V_{DD} – 0.15 V
2 2000 pF Load LCD, frame frequency = 32 Hz
3 VSUPPLY = 10, BYPASS = 0

2.12 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

2.13 VREF Characteristics

Table 21. VREF Electrical Specifications

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DDAD}	1.80	—	3.60	V
2	—	Operating temperature range	T_{op}	–40	—	105	°C
3	D	Load capability	I_{load}	—	—	10	mA
4	C P	Voltage reference output untrimmed factory trimmed	V_{REFO}	 1.070 1.04	 — 1.150	 1.202 1.17	 V V
5	D	Load regulation mode = 10, I_{load} = 1 mA		20	—	100	µV/mA
6	T	Line regulation (power supply rejection) DC AC		±0.1 from room temp voltage –60			 mV dB
7	T	Bandgap only (mode = 00)	I_{BG}	—	72	—	µA
8	C	Low power mode (mode = 01)	I_{LP}	—	90	125	µA
9	T	Tight regulation mode (mode =10)	I_{TR}	—	0.27	—	mA

2.14 SPI Characteristics

Table 22 and Figure 19 through Figure 22 describe the timing requirements for the SPI system.

3.2 100-pin LQFP Package

4 Revision History

Table 24. Revision History

Revision	Date	Description
1	10/15/2009	Initial public release.
2	4/29/2010	Updated teh descriptions of SPI in the Table 2. Changed the FSPIx to SPI16 to keep the term in accordance. Updated Figure 4 to Figure 8. Updated WI_{DD}, $S2I_{DD}$, $S3I_{DD}$ in the Table 11. Updated the ADC characteristics in the Table 13 to Table 15. Updated description of XOSC in the Section 2.9, “External Oscillator (XOSC) Characteristics.” Updated t_{CSTL} in the Table 16. Updated the the classification of IBG and ITR to T and added Voltage reference output (factory trimmed) in the Table 21. Update SPI data in the Table 22.
3	8/9/2010	Updated the V_{DD} at 20 MHz maximum operation to 3.6 V. Updated the RI_{DD} (at Run supply current FEI mode, all module on), $S2I_{DD}$ and $S3I_{DD}$ at 3 V, $S3I_{DDLVD}$ in the Table 11. Updated ENOB at 16 bit single-ended mode in the Table 14.