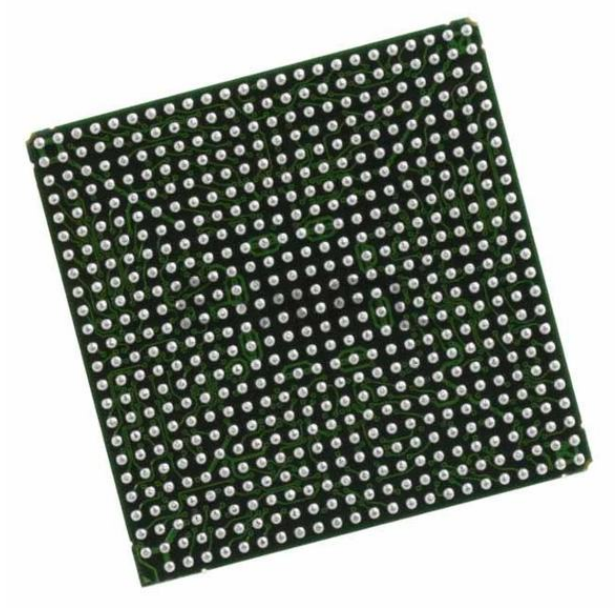
AMD Xilinx - XC2V1000-4BGG575C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	328
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-4bgg575c

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:
1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 µm / 0.12 µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally availabe in Pb-free versions CSG, FGG, and BGG. See Virtex-II Ordering Examples, page 6.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: **Maximum Number of User I/O Pads**

Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108

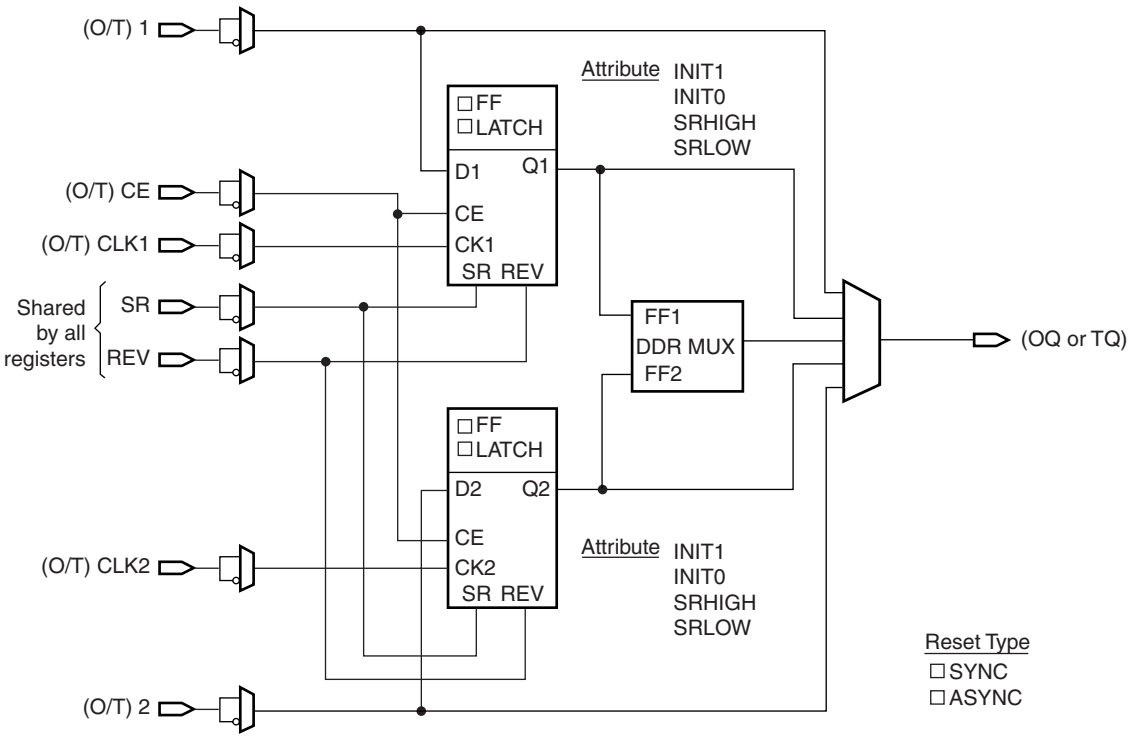


Figure 4: **Register / Latch Configuration in an IOB Block**

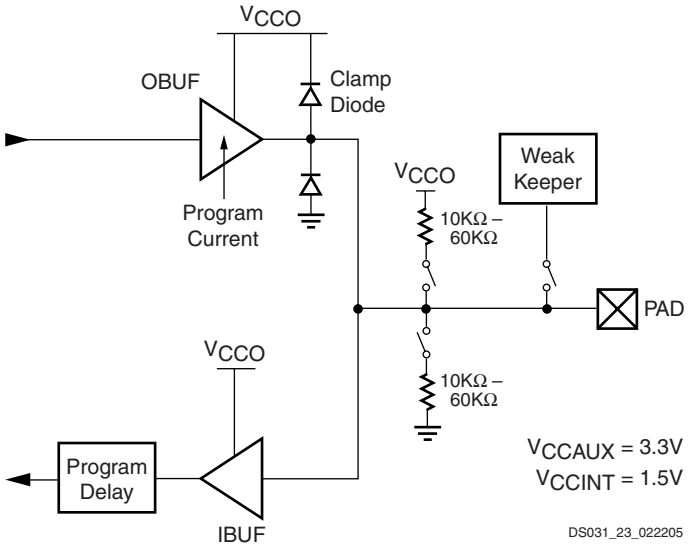


Figure 5: **LVTTL, LVCMOS or PCI SelectI/O-Ultra Standards**

Input/Output Individual Options

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V_{CCO} when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O-Ultra standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

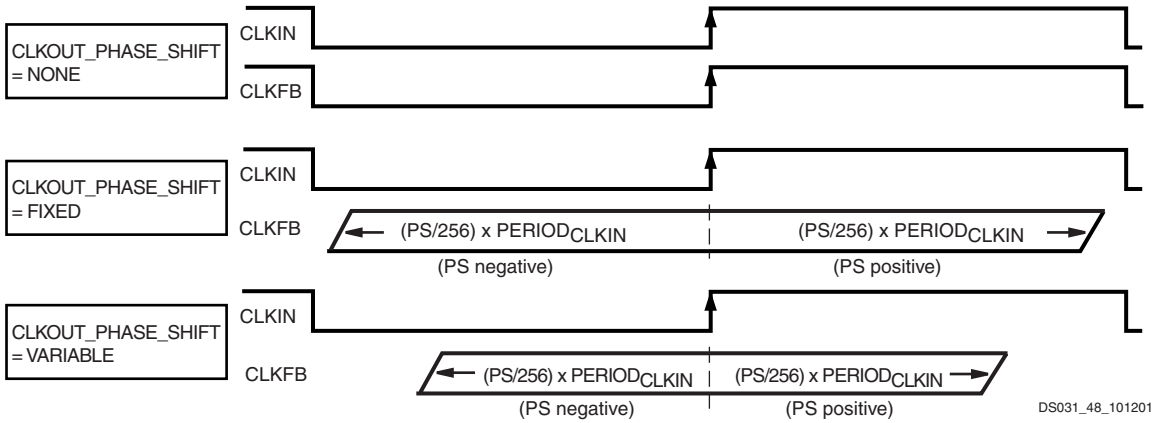


Figure 46: **Fine-Phase Shifting Effects**

Table 22 lists fine-phase shifting control pins, when used in variable mode.

Table 22: **Fine-Phase Shifting Control Pins**

Control Pin	Direction	Function
PSINCDEC	in	Increment or decrement
PSEN	in	Enable ± phase shift
PSCLK	in	Clock for phase shift
PSDONE	out	Active when completed

Two separate components of the phase shift range must be understood:

- PHASE_SHIFT attribute range
- FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

Phase Shift (ns) = (PHASE_SHIFT/256) * $PERIOD_{CLKIN}$

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit. Across process, voltage, and temperature, this absolute range is guaranteed to be as specified under DCM Timing Parameters in Module 3.

Absolute range (fixed mode) = ± FINE_SHIFT_RANGE

Absolute range (variable mode) = ± FINE_SHIFT_RANGE/2

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric, dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line, thus dividing the total delay line range in half. In fixed mode, since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertion into either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If $PERIOD_{CLKIN}$ = 2 * FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 128, and in variable mode it is limited to ± 64.
- If $PERIOD_{CLKIN}$ = FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 255, and in variable mode it is limited to ± 128.
- If $PERIOD_{CLKIN} \leq 0.5$ * FINE_SHIFT_RANGE, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to Table 23. (For actual values, see Virtex-II Switching Characteristics in Module 3). The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high-frequency mode.

High or low-frequency mode is selected by an attribute.

Table 23: **DCM Frequency Ranges**

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

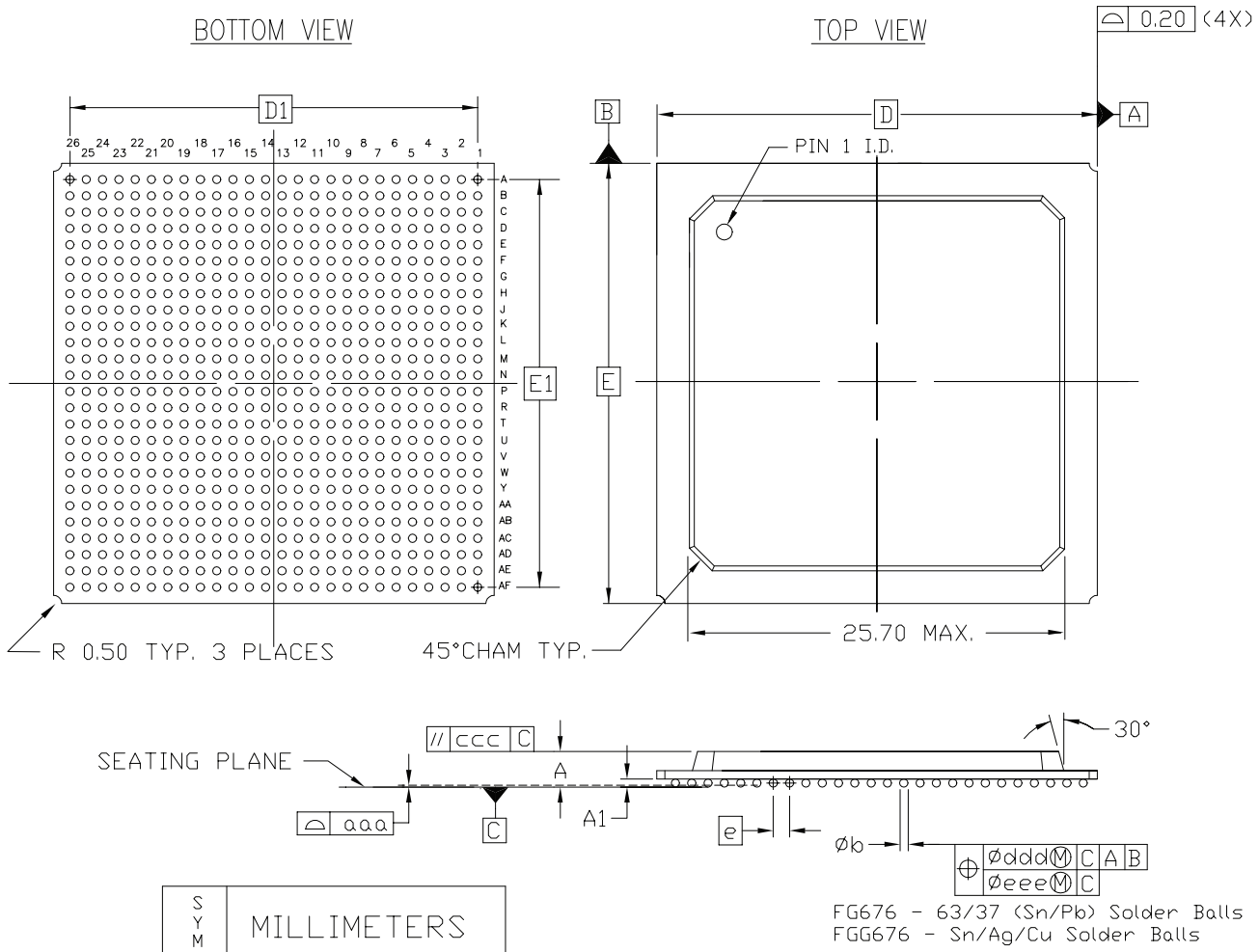
Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	IO_L93N_0	B10		
0	IO_L93P_0	A10		
0	IO_L94N_0/VREF_0	E11		
0	IO_L94P_0	F11		
0	IO_L95N_0/GCLK7P	D11		
0	IO_L95P_0/GCLK6S	C11		
0	IO_L96N_0/GCLK5P	B11		
0	IO_L96P_0/GCLK4S	A11		
1	IO_L96N_1/GCLK3P	F12		
1	IO_L96P_1/GCLK2S	F13		
1	IO_L95N_1/GCLK1P	E12		
1	IO_L95P_1/GCLK0S	D12		
1	IO_L94N_1	C12		
1	IO_L94P_1/VREF_1	B12		
1	IO_L93N_1	A13		
1	IO_L93P_1	B13		
1	IO_L92N_1	C13		
1	IO_L92P_1	D13		
1	IO_L91N_1	E13		
1	IO_L91P_1/VREF_1	E14		
1	IO_L54N_1	A14	NC	
1	IO_L54P_1	B14	NC	
1	IO_L52N_1	C14	NC	
1	IO_L52P_1	D14	NC	
1	IO_L51N_1/VREF_1	A15	NC	
1	IO_L51P_1	B15	NC	
1	IO_L49N_1	C15	NC	
1	IO_L49P_1	D15	NC	
1	IO_L24N_1	F14	NC	NC
1	IO_L24P_1	E15	NC	NC
1	IO_L22N_1	A16	NC	NC
1	IO_L22P_1	B16	NC	NC
1	IO_L21N_1/VREF_1	C16	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	IO_L51N_7	J2	NC	
7	IO_L49P_7	J3	NC	
7	IO_L49N_7	J4	NC	
7	IO_L48P_7	H1		
7	IO_L48N_7	H2		
7	IO_L46P_7	H3		
7	IO_L46N_7	H4		
7	IO_L45P_7/VREF_7	J6		
7	IO_L45N_7	H5		
7	IO_L43P_7	G1		
7	IO_L43N_7	G2		
7	IO_L24P_7	G3	NC	NC
7	IO_L24N_7	G4	NC	NC
7	IO_L22P_7	F1	NC	NC
7	IO_L22N_7	F2	NC	NC
7	IO_L21P_7/VREF_7	F3	NC	NC
7	IO_L21N_7	F4	NC	NC
7	IO_L19P_7	G5	NC	NC
7	IO_L19N_7	F5	NC	NC
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	D1		
7	IO_L03N_7	D2		
7	IO_L02P_7/VRN_7	C1		
7	IO_L02N_7/VRP_7	C2		
7	IO_L01P_7	E5		
7	IO_L01N_7	E6		
0	VCCO_0	G11		
0	VCCO_0	G10		
0	VCCO_0	G9		
0	VCCO_0	F8		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	VCCO_1	B14		
2	VCCO_2	M16		
2	VCCO_2	L23		
2	VCCO_2	L19		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	F22		
3	VCCO_3	W22		
3	VCCO_3	R16		
3	VCCO_3	P23		
3	VCCO_3	P19		
3	VCCO_3	P16		
3	VCCO_3	N16		
4	VCCO_4	AC14		
4	VCCO_4	AB19		
4	VCCO_4	W14		
4	VCCO_4	T15		
4	VCCO_4	T14		
4	VCCO_4	T13		
5	VCCO_5	AC11		
5	VCCO_5	AB6		
5	VCCO_5	W11		
5	VCCO_5	T12		
5	VCCO_5	T11		
5	VCCO_5	T10		
6	VCCO_6	W3		
6	VCCO_6	R9		
6	VCCO_6	P9		
6	VCCO_6	P6		
6	VCCO_6	P2		
6	VCCO_6	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	L6		
7	VCCO_7	L2		
7	VCCO_7	K9		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	VCCINT	R10		
NA	VCCINT	P15		
NA	VCCINT	P10		
NA	VCCINT	N15		
NA	VCCINT	N10		
NA	VCCINT	M15		
NA	VCCINT	M10		
NA	VCCINT	L15		
NA	VCCINT	L10		
NA	VCCINT	K15		
NA	VCCINT	K14		
NA	VCCINT	K13		
NA	VCCINT	K12		
NA	VCCINT	K11		
NA	VCCINT	K10		
NA	VCCINT	J16		
NA	VCCINT	J9		
NA	VCCINT	H17		
NA	VCCINT	H8		
NA	GND	AD24		
NA	GND	AD23		
NA	GND	AD18		
NA	GND	AD7		
NA	GND	AD2		
NA	GND	AD1		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC2		
NA	GND	AC1		
NA	GND	AB22		
NA	GND	AB3		
NA	GND	AA21		
NA	GND	AA15		
NA	GND	AA10		
NA	GND	AA4		
NA	GND	Y20		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L94N_1	C15
1	IO_L94P_1/VREF_1	D15
1	IO_L93N_1	E15
1	IO_L93P_1	F15
1	IO_L92N_1	G15
1	IO_L92P_1	H15
1	IO_L91N_1	J15
1	IO_L91P_1/VREF_1	J16
1	IO_L78N_1	A16
1	IO_L78P_1	B16
1	IO_L76N_1	D16
1	IO_L76P_1	E16
1	IO_L75N_1/VREF_1	F16
1	IO_L75P_1	F17
1	IO_L73N_1	H16
1	IO_L73P_1	H17
1	IO_L72N_1	A17
1	IO_L72P_1	B17
1	IO_L70N_1	C17
1	IO_L70P_1	D17
1	IO_L69N_1/VREF_1	G18
1	IO_L69P_1	G17
1	IO_L67N_1	A18
1	IO_L67P_1	B18
1	IO_L54N_1	C18
1	IO_L54P_1	D18
1	IO_L52N_1	E18
1	IO_L52P_1	F18
1	IO_L51N_1/VREF_1	H19
1	IO_L51P_1	H18
1	IO_L49N_1	A19
1	IO_L49P_1	A20
1	IO_L30N_1	B19
1	IO_L30P_1	C19
1	IO_L28N_1	D19
1	IO_L28P_1	E19

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
6	IO_L01N_6	AD1
6	IO_L02P_6/VRN_6	AD3
6	IO_L02N_6/VRP_6	AD2
6	IO_L03P_6	AC4
6	IO_L03N_6/VREF_6	AC3
6	IO_L04P_6	AC2
6	IO_L04N_6	AC1
6	IO_L06P_6	AB5
6	IO_L06N_6	AB4
6	IO_L19P_6	AB3
6	IO_L19N_6	AB2
6	IO_L21P_6	AB1
6	IO_L21N_6/VREF_6	AA1
6	IO_L22P_6	AA5
6	IO_L22N_6	AA6
6	IO_L24P_6	AA3
6	IO_L24N_6	AA2
6	IO_L25P_6	Y5
6	IO_L25N_6	Y6
6	IO_L27P_6	Y4
6	IO_L27N_6/VREF_6	Y3
6	IO_L28P_6	Y1
6	IO_L28N_6	W1
6	IO_L43P_6	W8
6	IO_L43N_6	W9
6	IO_L45P_6	W6
6	IO_L45N_6/VREF_6	W7
6	IO_L46P_6	W5
6	IO_L46N_6	W4
6	IO_L48P_6	W3
6	IO_L48N_6	W2
6	IO_L49P_6	V7
6	IO_L49N_6	V8
6	IO_L51P_6	V5
6	IO_L51N_6/VREF_6	V6
6	IO_L52P_6	V4

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L68N_6	Y26	NC	
6	IO_L69P_6	AA30	NC	
6	IO_L69N_6/VREF_6	Y30	NC	
6	IO_L70P_6	W24	NC	
6	IO_L70N_6	V24	NC	
6	IO_L71P_6	Y27	NC	
6	IO_L71N_6	W27	NC	
6	IO_L72P_6	W28	NC	
6	IO_L72N_6	Y28	NC	
6	IO_L73P_6	V25	NC	NC
6	IO_L73N_6	U25	NC	NC
6	IO_L74P_6	V26	NC	NC
6	IO_L74N_6	V27	NC	NC
6	IO_L75P_6	Y29	NC	NC
6	IO_L75N_6/VREF_6	W29	NC	NC
6	IO_L76P_6	U22	NC	NC
6	IO_L76N_6	T22	NC	NC
6	IO_L77P_6	U26	NC	NC
6	IO_L77N_6	T26	NC	NC
6	IO_L78P_6	V30	NC	NC
6	IO_L78N_6	W30	NC	NC
6	IO_L91P_6	U23		
6	IO_L91N_6	T23		
6	IO_L92P_6	U27		
6	IO_L92N_6	T27		
6	IO_L93P_6	V29		
6	IO_L93N_6/VREF_6	U29		
6	IO_L94P_6	T24		
6	IO_L94N_6	T25		
6	IO_L95P_6	U28		
6	IO_L95N_6	T28		
6	IO_L96P_6	T30		
6	IO_L96N_6	U30		
7	IO_L96P_7	P28		
7	IO_L96N_7	R28		
7	IO_L95P_7	R25		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	VBATT	A2		
NA	RSVD	E6		
NA	VCCAUX	AK28		
NA	VCCAUX	AK16		
NA	VCCAUX	AK3		
NA	VCCAUX	T1		
NA	VCCAUX	R30		
NA	VCCAUX	A28		
NA	VCCAUX	A15		
NA	VCCAUX	A3		
NA	VCCINT	AB22		
NA	VCCINT	AB9		
NA	VCCINT	AA21		
NA	VCCINT	AA10		
NA	VCCINT	Y20		
NA	VCCINT	Y19		
NA	VCCINT	Y18		
NA	VCCINT	Y17		
NA	VCCINT	Y16		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	Y12		
NA	VCCINT	Y11		
NA	VCCINT	W20		
NA	VCCINT	W11		
NA	VCCINT	V20		
NA	VCCINT	V11		
NA	VCCINT	U20		
NA	VCCINT	U11		
NA	VCCINT	T20		
NA	VCCINT	T11		
NA	VCCINT	R20		
NA	VCCINT	R11		
NA	VCCINT	P20		
NA	VCCINT	P11		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	T13		
NA	GND	T12		
NA	GND	R19		
NA	GND	R18		
NA	GND	R17		
NA	GND	R16		
NA	GND	R15		
NA	GND	R14		
NA	GND	R13		
NA	GND	R12		
NA	GND	P24		
NA	GND	P19		
NA	GND	P18		
NA	GND	P17		
NA	GND	P16		
NA	GND	P15		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P7		
NA	GND	N19		
NA	GND	N18		
NA	GND	N17		
NA	GND	N16		
NA	GND	N15		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	M26		
NA	GND	M19		
NA	GND	M18		
NA	GND	M17		
NA	GND	M16		
NA	GND	M15		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L26P_7	M31		
7	IO_L26N_7	L31		
7	IO_L25P_7	G38		
7	IO_L25N_7	H38		
7	IO_L24P_7	J34		
7	IO_L24N_7	K34		
7	IO_L23P_7	K32		
7	IO_L23N_7	K31		
7	IO_L22P_7	F39		
7	IO_L22N_7	G39		
7	IO_L21P_7/VREF_7	G36		
7	IO_L21N_7	H36		
7	IO_L20P_7	N28		
7	IO_L20N_7	M28		
7	IO_L19P_7	G37		
7	IO_L19N_7	H37		
7	IO_L12P_7	J33	NC	
7	IO_L12N_7	K33	NC	
7	IO_L11P_7	M29	NC	
7	IO_L11N_7	L28	NC	
7	IO_L10P_7	E38	NC	
7	IO_L10N_7	F38	NC	
7	IO_L09P_7/VREF_7	G35	NC	
7	IO_L09N_7	H35	NC	
7	IO_L08P_7	L30	NC	
7	IO_L08N_7	K29	NC	
7	IO_L07P_7	D39	NC	
7	IO_L07N_7	E39	NC	
7	IO_L06P_7	G34		
7	IO_L06N_7	H34		
7	IO_L05P_7	J32		
7	IO_L05N_7	H33		
7	IO_L04P_7	F36		
7	IO_L04N_7	F37		
7	IO_L03P_7/VREF_7	E36		
7	IO_L03N_7	F35		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		

BF957 Flip-Chip BGA Package

As shown in Table 14, XC2V2000, XC2V3000, XC2V4000, and XC2V6000 Virtex-II devices are available in the BF957 package. Pins in each of these devices are the same, except for the pin differences in the XC2V2000 device shown in the No Connect column. Following this table are the BF957 Flip-Chip BGA Package Specifications (1.27mm pitch).

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L01N_0	H23	
0	IO_L01P_0	H22	
0	IO_L02N_0	G24	
0	IO_L02P_0	E25	
0	IO_L03N_0/VRP_0	B29	
0	IO_L03P_0/VRN_0	C27	
0	IO_L04N_0/VREF_0	F24	
0	IO_L04P_0	F23	
0	IO_L05N_0	D26	
0	IO_L05P_0	D25	
0	IO_L06N_0	A28	
0	IO_L06P_0	A27	
0	IO_L19N_0	J22	
0	IO_L19P_0	J21	
0	IO_L20N_0	G23	
0	IO_L20P_0	G22	
0	IO_L21N_0	B27	
0	IO_L21P_0/VREF_0	B26	
0	IO_L22N_0	K20	
0	IO_L22P_0	K19	
0	IO_L23N_0	C26	
0	IO_L23P_0	C24	
0	IO_L24N_0	D24	
0	IO_L24P_0	D23	
0	IO_L25N_0	E24	NC
0	IO_L25P_0	E23	NC
0	IO_L26N_0	G21	NC
0	IO_L26P_0	G20	NC
0	IO_L27N_0	A26	NC
0	IO_L27P_0/VREF_0	A25	NC
0	IO_L29N_0	H21	NC
0	IO_L29P_0	H20	NC
0	IO_L30N_0	B25	NC
0	IO_L30P_0	B23	NC