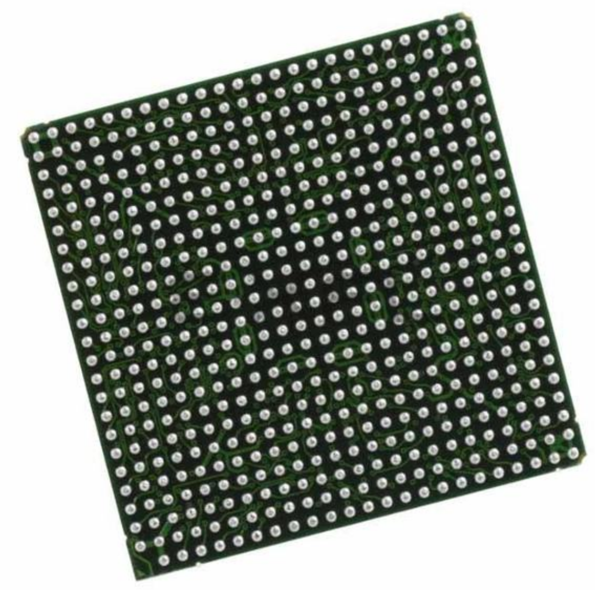

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

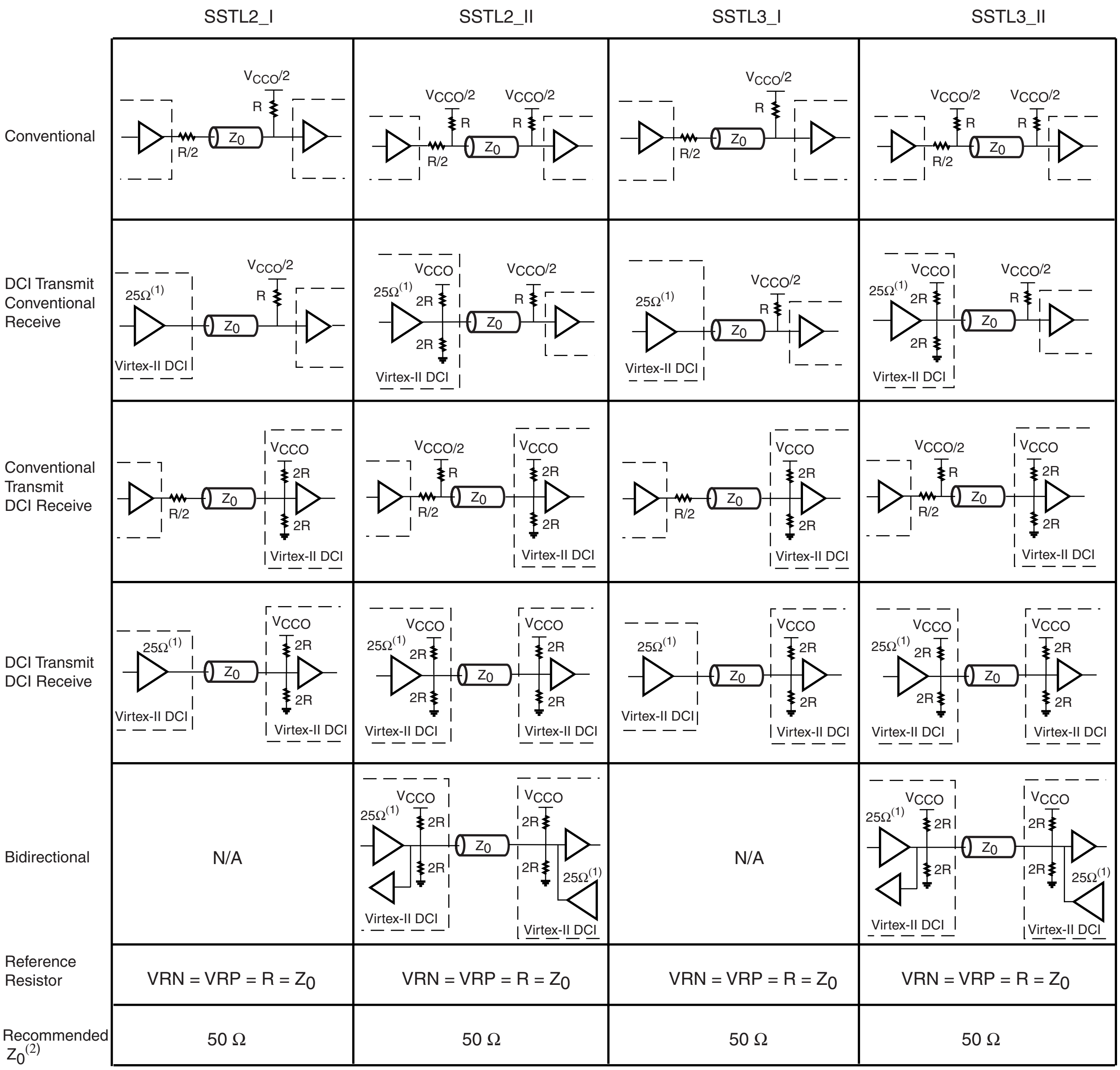
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	328
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-4bgg575i

Figure 12 provides examples illustrating the use of the SSTL2_I_DCI, SSTL2_II_DCI, SSTL3_I_DCI, and SSTL3_II_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.



Notes:
1. The SSTL-compatible 25Ω series resistor is accounted for in the DCI buffer, and it is not DCI controlled.
2. Z_0 is the recommended PCB trace impedance.

Figure 12: **SSTL DCI Usage Examples**

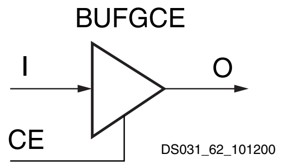


Figure 42: **Virtex-II BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect .

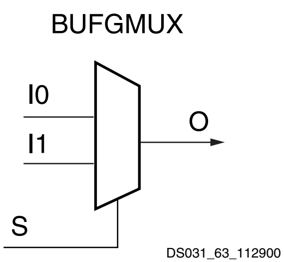


Figure 43: **Virtex-II BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 44 shows a switchover from I0 to I1.

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

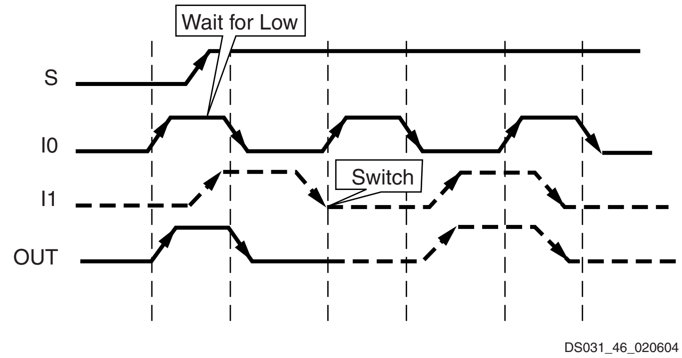


Figure 44: **Clock Multiplexer Waveform Diagram**

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 45). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 1.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 19.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 17) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

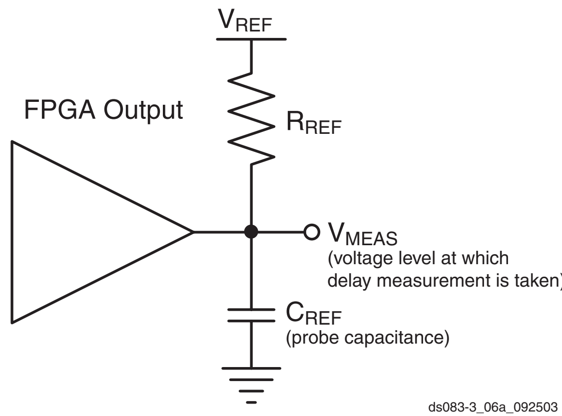


Figure 1: **Generalized Test Setup**

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10[(2)]	0.94	0
	PCI33_3 (falling edge)	25	10[(2)]	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10[(2)]	0.94	0
	PCI66_3 (falling edge)	25	10[(2)]	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10[(3)]	0.94	
	PCIX (falling edge	25	10[(3)]	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

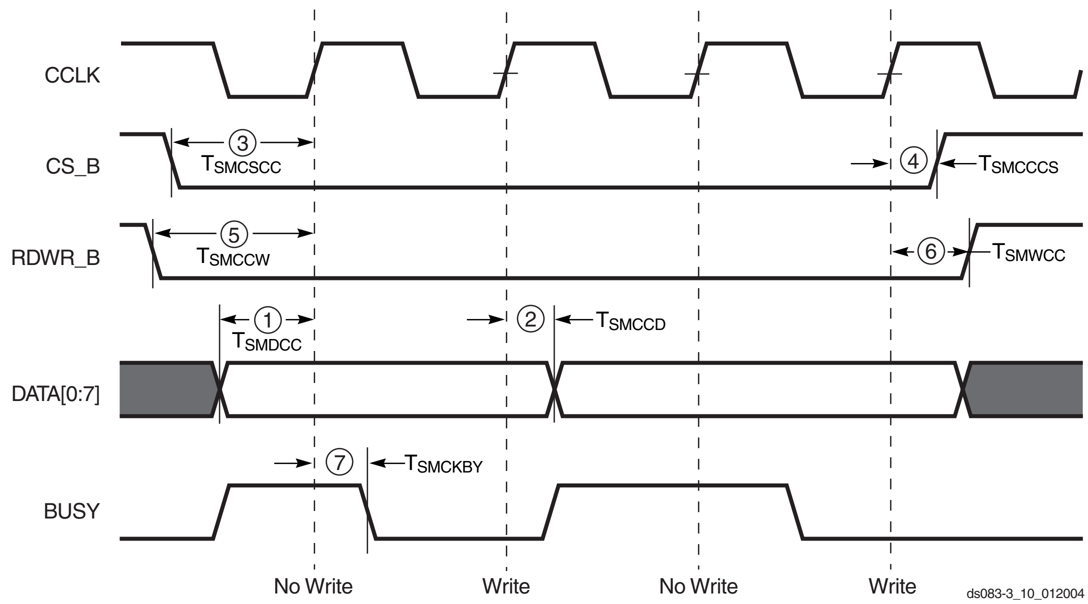


Figure 5: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 32: **SelectMAP Mode Write Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	CS_B setup/hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		$F_{CC\_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake		F_{CCNH}	50	MHz, max

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word “monotonically” to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
1	IO_L21P_1	D16	NC	NC
1	IO_L06N_1	E16		
1	IO_L06P_1	E17		
1	IO_L05N_1	A17		
1	IO_L05P_1	B17		
1	IO_L04N_1	C17		
1	IO_L04P_1/VREF_1	D17		
1	IO_L03N_1/VRP_1	A18		
1	IO_L03P_1/VRN_1	B18		
1	IO_L02N_1	C18		
1	IO_L02P_1	D18		
1	IO_L01N_1	A19		
1	IO_L01P_1	B19		
2	IO_L01N_2	C21		
2	IO_L01P_2	C22		
2	IO_L02N_2/VRP_2	E18		
2	IO_L02P_2/VRN_2	F18		
2	IO_L03N_2	D21		
2	IO_L03P_2/VREF_2	D22		
2	IO_L04N_2	E19		
2	IO_L04P_2	E20		
2	IO_L06N_2	E21		
2	IO_L06P_2	E22		
2	IO_L19N_2	F19	NC	NC
2	IO_L19P_2	F20	NC	NC
2	IO_L21N_2	F21	NC	NC
2	IO_L21P_2/VREF_2	F22	NC	NC
2	IO_L22N_2	G18	NC	NC
2	IO_L22P_2	H18	NC	NC
2	IO_L24N_2	G19	NC	NC
2	IO_L24P_2	G20	NC	NC
2	IO_L43N_2	G21		
2	IO_L43P_2	G22		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT[(1)]	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

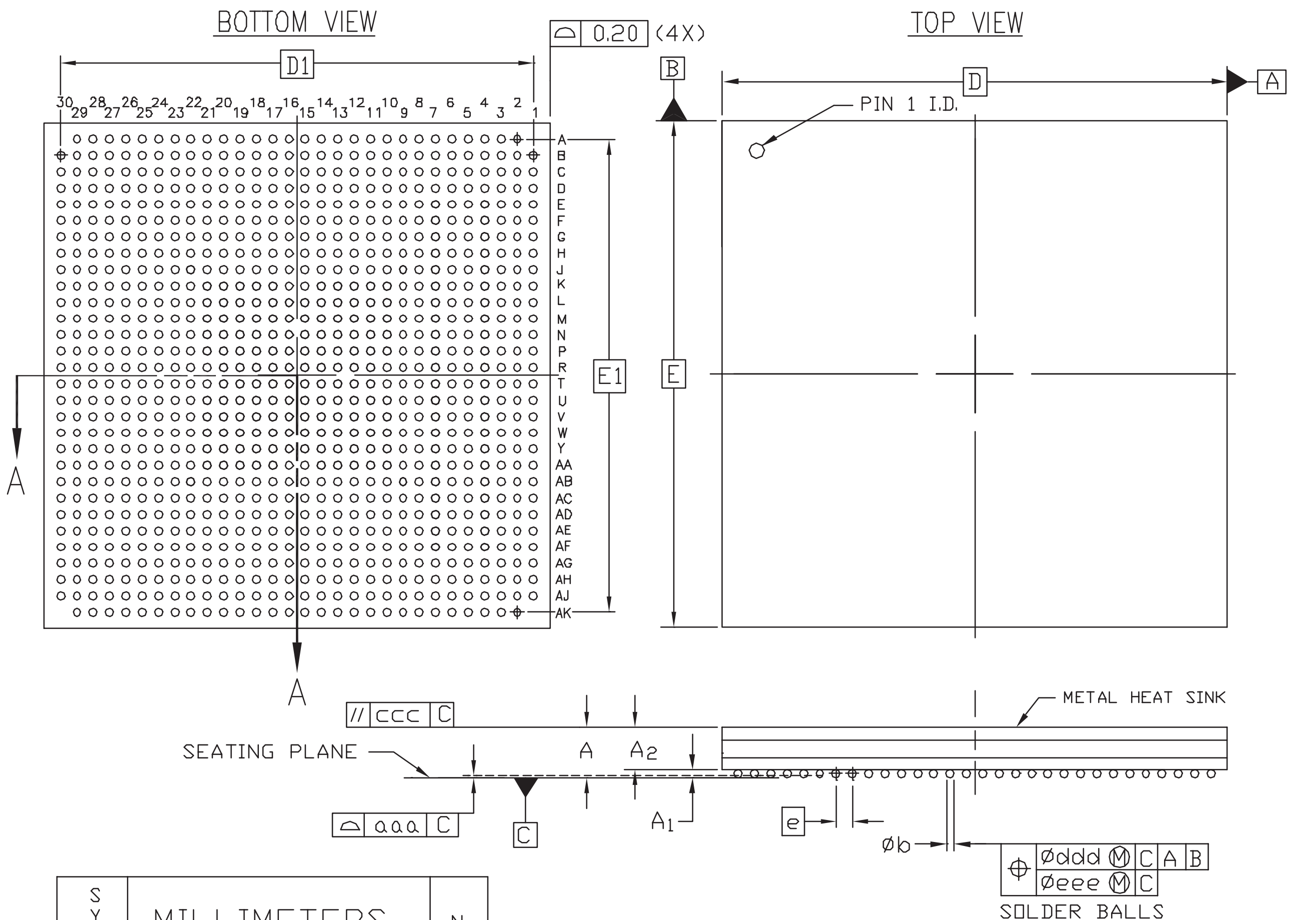
Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

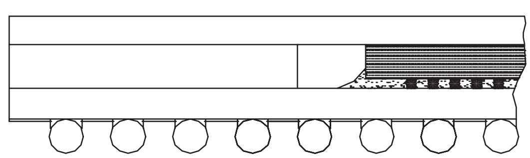
Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L19P_2	F26
2	IO_L21N_2	F27
2	IO_L21P_2/VREF_2	G27
2	IO_L22N_2	G23
2	IO_L22P_2	H23
2	IO_L24N_2	G25
2	IO_L24P_2	G26
2	IO_L25N_2	H21
2	IO_L25P_2	J21
2	IO_L27N_2	H22
2	IO_L27P_2/VREF_2	J22
2	IO_L28N_2	H24
2	IO_L28P_2	H25
2	IO_L30N_2	H27
2	IO_L30P_2	J27
2	IO_L43N_2	J23
2	IO_L43P_2	J24
2	IO_L45N_2	J25
2	IO_L45P_2/VREF_2	J26
2	IO_L46N_2	K20
2	IO_L46P_2	K21
2	IO_L48N_2	K22
2	IO_L48P_2	K23
2	IO_L49N_2	K24
2	IO_L49P_2	K25
2	IO_L51N_2	K26
2	IO_L51P_2/VREF_2	K27
2	IO_L52N_2	L20
2	IO_L52P_2	M20
2	IO_L54N_2	L21
2	IO_L54P_2	L22
2	IO_L67N_2	L24
2	IO_L67P_2	L25
2	IO_L69N_2	L26
2	IO_L69P_2/VREF_2	L27
2	IO_L70N_2	M19

FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	—	—	2.80	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	30			2



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAN–1 (DEPOPULATED)

Figure 7: **FF896 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 12, XC2V3000, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V3000

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT(1)	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN(1)	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	IO_L23N_6	AM38		
6	IO_L24P_6	AM36		
6	IO_L24N_6	AN36		
6	IO_L25P_6	AH30		
6	IO_L25N_6	AG30		
6	IO_L26P_6	AM37		
6	IO_L26N_6	AL37		
6	IO_L27P_6	AK34		
6	IO_L27N_6/VREF_6	AL34		
6	IO_L28P_6	AG29		
6	IO_L28N_6	AF29		
6	IO_L29P_6	AL35		
6	IO_L29N_6	AK35		
6	IO_L30P_6	AH33		
6	IO_L30N_6	AJ33		
6	IO_L31P_6	AJ32	NC	
6	IO_L31N_6	AH32	NC	
6	IO_L32P_6	AM39	NC	
6	IO_L32N_6	AL39	NC	
6	IO_L33P_6	AK36	NC	
6	IO_L33N_6/VREF_6	AL36	NC	
6	IO_L34P_6	AF28	NC	
6	IO_L34N_6	AE28	NC	
6	IO_L35P_6	AL38	NC	
6	IO_L35N_6	AK38	NC	
6	IO_L36P_6	AH34	NC	
6	IO_L36N_6	AJ34	NC	
6	IO_L43P_6	AG31		
6	IO_L43N_6	AF31		
6	IO_L44P_6	AK37		
6	IO_L44N_6	AJ37		
6	IO_L45P_6	AH36		
6	IO_L45N_6/VREF_6	AJ36		
6	IO_L46P_6	AF30		
6	IO_L46N_6	AE30		
6	IO_L47P_6	AK39		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	VCCINT	R19		
NA	VCCINT	R18		
NA	VCCINT	R17		
NA	VCCINT	R16		
NA	VCCINT	R15		
NA	VCCINT	P26		
NA	VCCINT	P20		
NA	VCCINT	P14		
NA	VCCINT	N27		
NA	VCCINT	N20		
NA	VCCINT	N13		
NA	GND	AW38		
NA	GND	AW37		
NA	GND	AW20		
NA	GND	AW3		
NA	GND	AW2		
NA	GND	AV39		
NA	GND	AV38		
NA	GND	AV37		
NA	GND	AV29		
NA	GND	AV11		
NA	GND	AV3		
NA	GND	AV2		
NA	GND	AV1		
NA	GND	AU39		
NA	GND	AU38		
NA	GND	AU37		
NA	GND	AU3		
NA	GND	AU2		
NA	GND	AU1		
NA	GND	AT36		
NA	GND	AT23		
NA	GND	AT20		
NA	GND	AT17		
NA	GND	AT4		
NA	GND	AR35		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
3	IO_L03P_3	AD7	
3	IO_L02N_3/VRP_3	AE6	
3	IO_L02P_3/VRN_3	AF5	
3	IO_L01N_3	AH2	
3	IO_L01P_3	AH3	
4	IO_L01N_4/BUSY/DOUT(1)	AD9	
4	IO_L01P_4/INIT_B	AD10	
4	IO_L02N_4/D0/DIN(1)	AF7	
4	IO_L02P_4/D1	AG7	
4	IO_L03N_4/D2/ALT_VRP_4	AK3	
4	IO_L03P_4/D3/ALT_VRN_4	AJ5	
4	IO_L04N_4/VREF_4	AE8	
4	IO_L04P_4	AF8	
4	IO_L05N_4/VRP_4	AK4	
4	IO_L05P_4/VRN_4	AK5	
4	IO_L06N_4	AH6	
4	IO_L06P_4	AH7	
4	IO_L19N_4	AC10	
4	IO_L19P_4	AC11	
4	IO_L20N_4	AE9	
4	IO_L20P_4	AE10	
4	IO_L21N_4	AL4	
4	IO_L21P_4/VREF_4	AL5	
4	IO_L22N_4	AB12	
4	IO_L22P_4	AB13	
4	IO_L23N_4	AJ6	
4	IO_L23P_4	AJ8	
4	IO_L24N_4	AK6	
4	IO_L24P_4	AK7	
4	IO_L25N_4	AG8	NC
4	IO_L25P_4	AG9	NC
4	IO_L26N_4	AF9	NC
4	IO_L26P_4	AF11	NC
4	IO_L27N_4	AH8	NC
4	IO_L27P_4/VREF_4	AH9	NC
4	IO_L28N_4	AD11	NC
4	IO_L28P_4	AD12	NC

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L06N_7	E28	
7	IO_L05P_7	K22	
7	IO_L05N_7	K21	
7	IO_L04P_7	F29	
7	IO_L04N_7	E29	
7	IO_L03P_7/VREF_7	H26	
7	IO_L03N_7	H25	
7	IO_L02P_7/VRN_7	G26	
7	IO_L02N_7/VRP_7	F27	
7	IO_L01P_7	D30	
7	IO_L01N_7	D29	
0	VCCO_0	C18	
0	VCCO_0	C25	
0	VCCO_0	F22	
0	VCCO_0	H18	
0	VCCO_0	L17	
0	VCCO_0	L18	
0	VCCO_0	L19	
0	VCCO_0	L20	
0	VCCO_0	M17	
0	VCCO_0	M18	
0	VCCO_0	M19	
1	VCCO_1	C7	
1	VCCO_1	C14	
1	VCCO_1	F10	
1	VCCO_1	H14	
1	VCCO_1	L12	
1	VCCO_1	L13	
1	VCCO_1	L14	
1	VCCO_1	L15	
1	VCCO_1	M13	
1	VCCO_1	M14	
1	VCCO_1	M15	
2	VCCO_2	G3	
2	VCCO_2	K6	
2	VCCO_2	M11	
2	VCCO_2	N11	