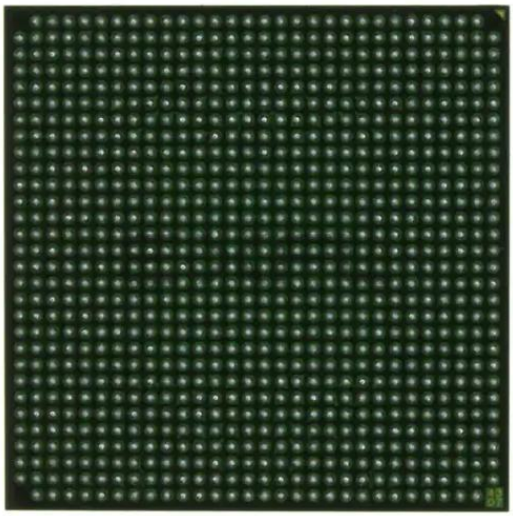

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	432
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-4ffg896i

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF}. Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: **IOB Output Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTL_S2	T_{OLVTTL_S2}	9.42	9.71	10.68	ns
LVTTL, Slow, 4 mA	LVTTL_S4	T_{OLVTTL_S4}	5.77	5.95	6.55	ns
LVTTL, Slow, 6 mA	LVTTL_S6	T_{OLVTTL_S6}	4.11	4.24	4.66	ns
LVTTL, Slow, 8 mA	LVTTL_S8	T_{OLVTTL_S8}	2.87	2.96	3.26	ns
LVTTL, Slow, 12 mA	LVTTL_S12	T_{OLVTTL_S12}	2.32	2.39	2.63	ns
LVTTL, Slow, 16 mA	LVTTL_S16	T_{OLVTTL_S16}	1.70	1.75	1.93	ns
LVTTL, Slow, 24 mA	LVTTL_S24	T_{OLVTTL_S24}	1.26	1.30	1.43	ns
LVTTL, Fast, 2 mA	LVTTL_F2	T_{OLVTTL_F2}	6.52	6.72	7.39	ns
LVTTL, Fast, 4 mA	LVTTL_F4	T_{OLVTTL_F4}	2.80	2.88	3.17	ns
LVTTL, Fast, 6 mA	LVTTL_F6	T_{OLVTTL_F6}	1.57	1.62	1.78	ns
LVTTL, Fast, 8 mA	LVTTL_F8	T_{OLVTTL_F8}	0.46	0.48	0.52	ns
LVTTL, Fast, 12 mA	LVTTL_F12	T_{OLVTTL_F12}	0.00	0.00	0.00	ns
LVTTL, Fast, 16 mA	LVTTL_F16	T_{OLVTTL_F16}	–0.13	–0.14	–0.15	ns
LVTTL, Fast, 24 mA	LVTTL_F24	T_{OLVTTL_F24}	–0.22	–0.23	–0.26	ns
LVCMOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVCMOS33_S2	$T_{OLVCMOS33\_S2}$	7.67	7.91	8.70	ns
LVCMOS, 3.3V, Slow, 4 mA	LVCMOS33_S4	$T_{OLVCMOS33\_S4}$	4.37	4.50	4.95	ns
LVCMOS, 3.3V, Slow, 6 mA	LVCMOS33_S6	$T_{OLVCMOS33\_S6}$	3.34	3.44	3.78	ns
LVCMOS, 3.3V, Slow, 8 mA	LVCMOS33_S8	$T_{OLVCMOS33\_S8}$	2.29	2.36	2.60	ns
LVCMOS, 3.3V, Slow, 12 mA	LVCMOS33_S12	$T_{OLVCMOS33\_S12}$	1.91	1.97	2.16	ns
LVCMOS, 3.3V, Slow, 16 mA	LVCMOS33_S16	$T_{OLVCMOS33\_S16}$	1.24	1.27	1.40	ns
LVCMOS, 3.3V, Slow, 24 mA	LVCMOS33_S24	$T_{OLVCMOS33\_S24}$	1.18	1.22	1.34	ns
LVCMOS, 3.3V, Fast, 2 mA	LVCMOS33_F2	$T_{OLVCMOS33\_F2}$	5.82	6.00	6.60	ns
LVCMOS, 3.3V, Fast, 4 mA	LVCMOS33_F4	$T_{OLVCMOS33\_F4}$	2.48	2.55	2.81	ns
LVCMOS, 3.3V, Fast, 6 mA	LVCMOS33_F6	$T_{OLVCMOS33\_F6}$	1.28	1.31	1.45	ns
LVCMOS, 3.3V, Fast, 8 mA	LVCMOS33_F8	$T_{OLVCMOS33\_F8}$	0.48	0.49	0.54	ns
LVCMOS, 3.3V, Fast, 12 mA	LVCMOS33_F12	$T_{OLVCMOS33\_F12}$	0.27	0.28	0.31	ns
LVCMOS, 3.3V, Fast, 16 mA	LVCMOS33_F16	$T_{OLVCMOS33\_F16}$	–0.14	–0.14	–0.15	ns
LVCMOS, 3.3V, Fast, 24 mA	LVCMOS33_F24	$T_{OLVCMOS33\_F24}$	–0.21	–0.21	–0.23	ns
LVCMOS, 2.5V, Slow, 2 mA	LVCMOS25_S2	$T_{OLVCMOS25\_S2}$	9.11	9.39	10.33	ns
LVCMOS, 2.5V, Slow, 4 mA	LVCMOS25_S4	$T_{OLVCMOS25\_S4}$	5.00	5.16	5.67	ns
LVCMOS, 2.5V, Slow, 6 mA	LVCMOS25_S6	$T_{OLVCMOS25\_S6}$	4.53	4.67	5.13	ns
LVCMOS, 2.5V, Slow, 8 mA	LVCMOS25_S8	$T_{OLVCMOS25\_S8}$	3.86	3.98	4.38	ns
LVCMOS, 2.5V, Slow, 12 mA	LVCMOS25_S12	$T_{OLVCMOS25\_S12}$	2.84	2.93	3.22	ns
LVCMOS, 2.5V, Slow, 16 mA	LVCMOS25_S16	$T_{OLVCMOS25\_S16}$	2.36	2.43	2.67	ns
LVCMOS, 2.5V, Slow, 24 mA	LVCMOS25_S24	$T_{OLVCMOS25\_S24}$	2.00	2.06	2.27	ns
LVCMOS, 2.5V, Fast, 2 mA	LVCMOS25_F2	$T_{OLVCMOS25\_F2}$	4.06	4.18	4.60	ns
LVCMOS, 2.5V, Fast, 4 mA	LVCMOS25_F4	$T_{OLVCMOS25\_F4}$	1.15	1.18	1.30	ns
LVCMOS, 2.5V, Fast, 6 mA	LVCMOS25_F6	$T_{OLVCMOS25\_F6}$	0.72	0.74	0.81	ns
LVCMOS, 2.5V, Fast, 8 mA	LVCMOS25_F8	$T_{OLVCMOS25\_F8}$	0.33	0.34	0.37	ns
LVCMOS, 2.5V, Fast, 12 mA	LVCMOS25_F12	$T_{OLVCMOS25\_F12}$	0.02	0.02	0.03	ns

Virtex-II Platform FPGAs: Pinout Information

DS031-4 (v3.5) November 5, 2007

Product Specification

This document provides Virtex-II™ Device/Package Combinations, Maximum I/Os Available, and Virtex-II Pin Definitions, followed by pinout tables for the following packages:

- CS144/CSG144 Chip-Scale BGA Package
- FG256/FGG256 Fine-Pitch BGA Package
- FG456/FGG456 Fine-Pitch BGA Package
- FG676/FGG676 Fine-Pitch BGA Package
- BG575/BGG575 Standard BGA Package
- BG728/BGG728 Standard BGA Package
- FF896 Flip-Chip Fine-Pitch BGA Package
- FF1152 Flip-Chip Fine-Pitch BGA Package
- FF1517 Flip-Chip Fine-Pitch BGA Package
- BF957 Flip-Chip BGA Package

For device pinout diagrams and layout guidelines, refer to the ***Virtex-II Platform FPGA User Guide***. ASCII package pinout files are also available for download from the Xilinx website (**www.xilinx.com**).

Virtex-II Device/Package Combinations and Maximum I/Os Available

Wire-bond and flip-chip packages are available. Table 1 and Table 2 show the maximum number of user I/Os possible in wire-bond and flip-chip packages, respectively.

Table 3 shows the number of user I/Os available for all device/package combinations.

- CS denotes wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- CSG denotes Pb-free wire-bond chip-scale ball grid array (BGA) (0.80 mm pitch).
- FG denotes wire-bond fine-pitch BGA (1.00 mm pitch).
- FGG denotes Pb-free wire-bond fine-pitch BGA (1.00 mm pitch).
- BG denotes standard BGA (1.27 mm pitch).
- BGG denotes Pb-free standard BGA (1.27 mm pitch).
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch).
- BF denotes flip-chip BGA (1.27 mm pitch).

The number of I/Os per package include all user I/Os except the 15 control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAP_EN, DXN, DXP, AND RSVD).

Table 1: **Wire-Bond Packages Information**

Package[1]	CS144/ CSG144	FG256/ FGG256	FG456/ FGG456	FG676/ FGG676	BG575/ BGG575	BG728/ BGG728
Pitch (mm)	0.80	1.00	1.00	1.00	1.27	1.27
Size (mm)	12 x 12	17 x 17	23 x 23	27 x 27	31 x 31	35 x 35
I/Os	92	172	324	484	408	516

Notes:
1. Wire-bond packages include FGG*nnn* Pb-free versions. See Virtex-II Ordering Examples (Module 1).

Table 2: **Flip-Chip Packages Information**

Package	FF896	FF1152	FF1517	BF957
Pitch (mm)	1.00	1.00	1.00	1.27
Size (mm)	31 x 31	35 x 35	40 x 40	40 x 40
I/Os	624	824	1,108	684

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

FG676/FGG676 Fine-Pitch BGA Package

As shown in Table 8, XC2V1500, XC2V2000, and XC2V3000 Virtex-II devices are available in the FG676/FGG676 fine-pitch BGA package. Pins in the XC2V1500, XC2V2000, and XC2V3000 devices are the same, except for the pin differences in the XC2V1500 and XC2V2000 devices shown in the No Connect columns. Following this table are the FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
0	IO_L01N_0	D6		
0	IO_L01P_0	C6		
0	IO_L02N_0	B1		
0	IO_L02P_0	A2		
0	IO_L03N_0/VRP_0	D7		
0	IO_L03P_0/VRN_0	C7		
0	IO_L04N_0/VREF_0	B3		
0	IO_L04P_0	A3		
0	IO_L05N_0	G6		
0	IO_L05P_0	G7		
0	IO_L06N_0	E6		
0	IO_L06P_0	E7		
0	IO_L19N_0	B4		
0	IO_L19P_0	A4		
0	IO_L21N_0	B5		
0	IO_L21P_0/VREF_0	A5		
0	IO_L22N_0	B6		
0	IO_L22P_0	A6		
0	IO_L24N_0	A7		
0	IO_L24P_0	A8		
0	IO_L25N_0	E8	NC	NC
0	IO_L25P_0	D8	NC	NC
0	IO_L27N_0	G8	NC	NC
0	IO_L27P_0/VREF_0	F8	NC	NC
0	IO_L49N_0	C8		
0	IO_L49P_0	B8		
0	IO_L51N_0	D9		
0	IO_L51P_0/VREF_0	E9		
0	IO_L52N_0	F9		
0	IO_L52P_0	G9		
0	IO_L54N_0	B9		
0	IO_L54P_0	A9		
0	IO_L67N_0	C9		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L06P_4	Y21		
4	IO_L19N_4	AE24		
4	IO_L19P_4	AF24		
4	IO_L21N_4	AE23		
4	IO_L21P_4/VREF_4	AF23		
4	IO_L22N_4	AE22		
4	IO_L22P_4	AF22		
4	IO_L24N_4	AF21		
4	IO_L24P_4	AF20		
4	IO_L25N_4	AA19	NC	NC
4	IO_L25P_4	AB19	NC	NC
4	IO_L27N_4	AD20	NC	NC
4	IO_L27P_4/VREF_4	AC20	NC	NC
4	IO_L28N_4	AC19	NC	NC
4	IO_L28P_4	AD19	NC	NC
4	IO_L49N_4	AE19		
4	IO_L49P_4	AF19		
4	IO_L51N_4	AA18		
4	IO_L51P_4/VREF_4	AB18		
4	IO_L52N_4	Y18		
4	IO_L52P_4	Y17		
4	IO_L54N_4	AC18		
4	IO_L54P_4	AD18		
4	IO_L67N_4	AE18		
4	IO_L67P_4	AF18		
4	IO_L69N_4	AA17		
4	IO_L69P_4/VREF_4	AB17		
4	IO_L70N_4	AC17		
4	IO_L70P_4	AD17		
4	IO_L72N_4	AF17		
4	IO_L72P_4	AF16		
4	IO_L73N_4	AB16	NC	
4	IO_L73P_4	AC16	NC	
4	IO_L75N_4	AA16	NC	
4	IO_L75P_4/VREF_4	Y16	NC	
4	IO_L76N_4	AD16	NC	
4	IO_L76P_4	AE16	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	L11		
NA	GND	L10		
NA	GND	K17		
NA	GND	K16		
NA	GND	K15		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	F21		
NA	GND	F6		
NA	GND	E22		
NA	GND	E5		
NA	GND	D23		
NA	GND	D4		
NA	GND	C24		
NA	GND	C3		
NA	GND	B25		
NA	GND	B14		
NA	GND	B13		
NA	GND	B2		
NA	GND	A26		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	VCCINT	R10		
NA	VCCINT	P15		
NA	VCCINT	P10		
NA	VCCINT	N15		
NA	VCCINT	N10		
NA	VCCINT	M15		
NA	VCCINT	M10		
NA	VCCINT	L15		
NA	VCCINT	L10		
NA	VCCINT	K15		
NA	VCCINT	K14		
NA	VCCINT	K13		
NA	VCCINT	K12		
NA	VCCINT	K11		
NA	VCCINT	K10		
NA	VCCINT	J16		
NA	VCCINT	J9		
NA	VCCINT	H17		
NA	VCCINT	H8		
NA	GND	AD24		
NA	GND	AD23		
NA	GND	AD18		
NA	GND	AD7		
NA	GND	AD2		
NA	GND	AD1		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC2		
NA	GND	AC1		
NA	GND	AB22		
NA	GND	AB3		
NA	GND	AA21		
NA	GND	AA15		
NA	GND	AA10		
NA	GND	AA4		
NA	GND	Y20		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L51N_2	L6	
2	IO_L51P_2/VREF_2	M6	
2	IO_L52N_2	M3	
2	IO_L52P_2	L3	
2	IO_L53N_2	L4	
2	IO_L53P_2	K4	
2	IO_L54N_2	N4	
2	IO_L54P_2	M4	
2	IO_L67N_2	M2	
2	IO_L67P_2	L2	
2	IO_L68N_2	N8	
2	IO_L68P_2	P8	
2	IO_L69N_2	N6	
2	IO_L69P_2/VREF_2	P6	
2	IO_L70N_2	P5	
2	IO_L70P_2	N5	
2	IO_L71N_2	P10	
2	IO_L71P_2	R10	
2	IO_L72N_2	P3	
2	IO_L72P_2	N3	
2	IO_L73N_2	M1	
2	IO_L73P_2	L1	
2	IO_L74N_2	P9	
2	IO_L74P_2	R9	
2	IO_L75N_2	P2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	R4	
2	IO_L76P_2	P4	
2	IO_L77N_2	R8	
2	IO_L77P_2	T8	
2	IO_L78N_2	T3	
2	IO_L78P_2	R3	
2	IO_L79N_2	P1	NC
2	IO_L79P_2	N1	NC
2	IO_L80N_2	T11	NC
2	IO_L80P_2	U11	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L53P_3	AD2	
3	IO_L52N_3	AC8	
3	IO_L52P_3	AB8	
3	IO_L51N_3/VREF_3	AB10	
3	IO_L51P_3	AC10	
3	IO_L50N_3	AD5	
3	IO_L50P_3	AE5	
3	IO_L49N_3	AE4	
3	IO_L49P_3	AF4	
3	IO_L48N_3	AB9	
3	IO_L48P_3	AC9	
3	IO_L47N_3	AE2	
3	IO_L47P_3	AF1	
3	IO_L46N_3	AD6	
3	IO_L46P_3	AE6	
3	IO_L45N_3/VREF_3	AD9	
3	IO_L45P_3	AE9	
3	IO_L44N_3	AF2	
3	IO_L44P_3	AG2	
3	IO_L43N_3	AF3	
3	IO_L43P_3	AG3	
3	IO_L30N_3	AD7	
3	IO_L30P_3	AE7	
3	IO_L29N_3	AF5	
3	IO_L29P_3	AG5	
3	IO_L28N_3	AE8	
3	IO_L28P_3	AD8	
3	IO_L27N_3/VREF_3	AF8	
3	IO_L27P_3	AF9	
3	IO_L26N_3	AH1	
3	IO_L26P_3	AJ1	
3	IO_L25N_3	AG4	
3	IO_L25P_3	AH5	
3	IO_L24N_3	AF6	
3	IO_L24P_3	AG6	
3	IO_L23N_3	AH3	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	IO_L79P_5	AP21	NC
5	IO_L78N_5	AK22	
5	IO_L78P_5	AK21	
5	IO_L77N_5	AD18	
5	IO_L77P_5	AD19	
5	IO_L76N_5	AN22	
5	IO_L76P_5	AN21	
5	IO_L75N_5/VREF_5	AJ20	
5	IO_L75P_5	AH20	
5	IO_L74N_5	AG19	
5	IO_L74P_5	AG20	
5	IO_L73N_5	AP24	
5	IO_L73P_5	AP23	
5	IO_L72N_5	AL23	
5	IO_L72P_5	AL22	
5	IO_L71N_5	AF20	
5	IO_L71P_5	AF21	
5	IO_L70N_5	AM24	
5	IO_L70P_5	AM23	
5	IO_L69N_5/VREF_5	AJ21	
5	IO_L69P_5	AJ22	
5	IO_L68N_5	AJ24	
5	IO_L68P_5	AJ23	
5	IO_L67N_5	AN24	
5	IO_L67P_5	AN23	
5	IO_L60N_5	AN26	NC
5	IO_L60P_5	AN25	NC
5	IO_L54N_5	AL25	
5	IO_L54P_5	AL24	
5	IO_L53N_5	AE20	
5	IO_L53P_5	AE21	
5	IO_L52N_5	AN27	
5	IO_L52P_5	AP26	
5	IO_L51N_5/VREF_5	AP29	
5	IO_L51P_5	AP28	
5	IO_L50N_5	AG21	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L29P_6	AF31	
6	IO_L29N_6	AG31	
6	IO_L30P_6	AF32	
6	IO_L30N_6	AG32	
6	IO_L43P_6	AC25	
6	IO_L43N_6	AB25	
6	IO_L44P_6	AJ33	
6	IO_L44N_6	AH33	
6	IO_L45P_6	AE31	
6	IO_L45N_6/VREF_6	AD32	
6	IO_L46P_6	AD27	
6	IO_L46N_6	AC27	
6	IO_L47P_6	AJ34	
6	IO_L47N_6	AH34	
6	IO_L48P_6	AE30	
6	IO_L48N_6	AD30	
6	IO_L49P_6	AC26	
6	IO_L49N_6	AB26	
6	IO_L50P_6	AD29	
6	IO_L50N_6	AC29	
6	IO_L51P_6	AF33	
6	IO_L51N_6/VREF_6	AG33	
6	IO_L52P_6	AC28	
6	IO_L52N_6	AB28	
6	IO_L53P_6	AF34	
6	IO_L53N_6	AE33	
6	IO_L54P_6	AB27	
6	IO_L54N_6	AA27	
6	IO_L67P_6	AA25	
6	IO_L67N_6	Y25	
6	IO_L68P_6	AD33	
6	IO_L68N_6	AC33	
6	IO_L69P_6	AC32	
6	IO_L69N_6/VREF_6	AB32	
6	IO_L70P_6	AA26	
6	IO_L70N_6	Y26	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L50P_7	P32		
7	IO_L50N_7	N32		
7	IO_L49P_7	L37		
7	IO_L49N_7	M37		
7	IO_L48P_7	N34		
7	IO_L48N_7	P34		
7	IO_L47P_7	P31		
7	IO_L47N_7	N31		
7	IO_L46P_7	M35		
7	IO_L46N_7	N35		
7	IO_L45P_7/VREF_7	L36		
7	IO_L45N_7	M36		
7	IO_L44P_7	R28		
7	IO_L44N_7	P28		
7	IO_L43P_7	K39		
7	IO_L43N_7	L39		
7	IO_L36P_7	L34	NC	
7	IO_L36N_7	M34	NC	
7	IO_L35P_7	P29	NC	
7	IO_L35N_7	N29	NC	
7	IO_L34P_7	J38	NC	
7	IO_L34N_7	K38	NC	
7	IO_L33P_7/VREF_7	L33	NC	
7	IO_L33N_7	M33	NC	
7	IO_L32P_7	M32	NC	
7	IO_L32N_7	L32	NC	
7	IO_L31P_7	H39	NC	
7	IO_L31N_7	J39	NC	
7	IO_L30P_7	J36		
7	IO_L30N_7	K36		
7	IO_L29P_7	N30		
7	IO_L29N_7	M30		
7	IO_L28P_7	J37		
7	IO_L28N_7	K37		
7	IO_L27P_7/VREF_7	J35		
7	IO_L27N_7	K35		

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.