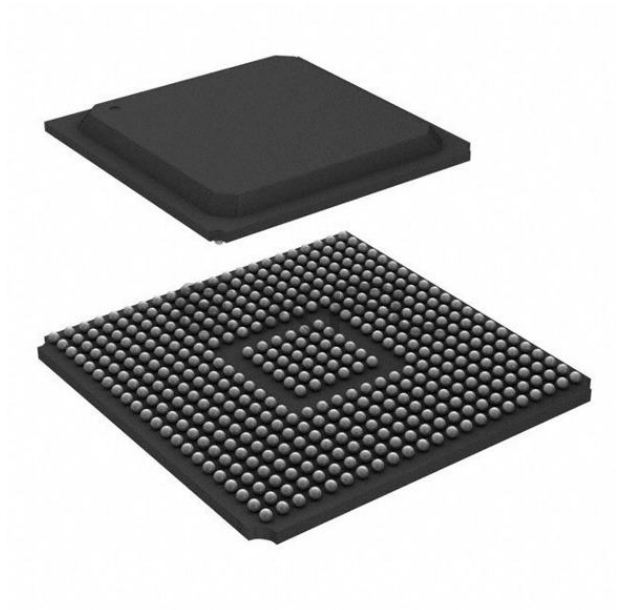


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	324
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-4fgg456c

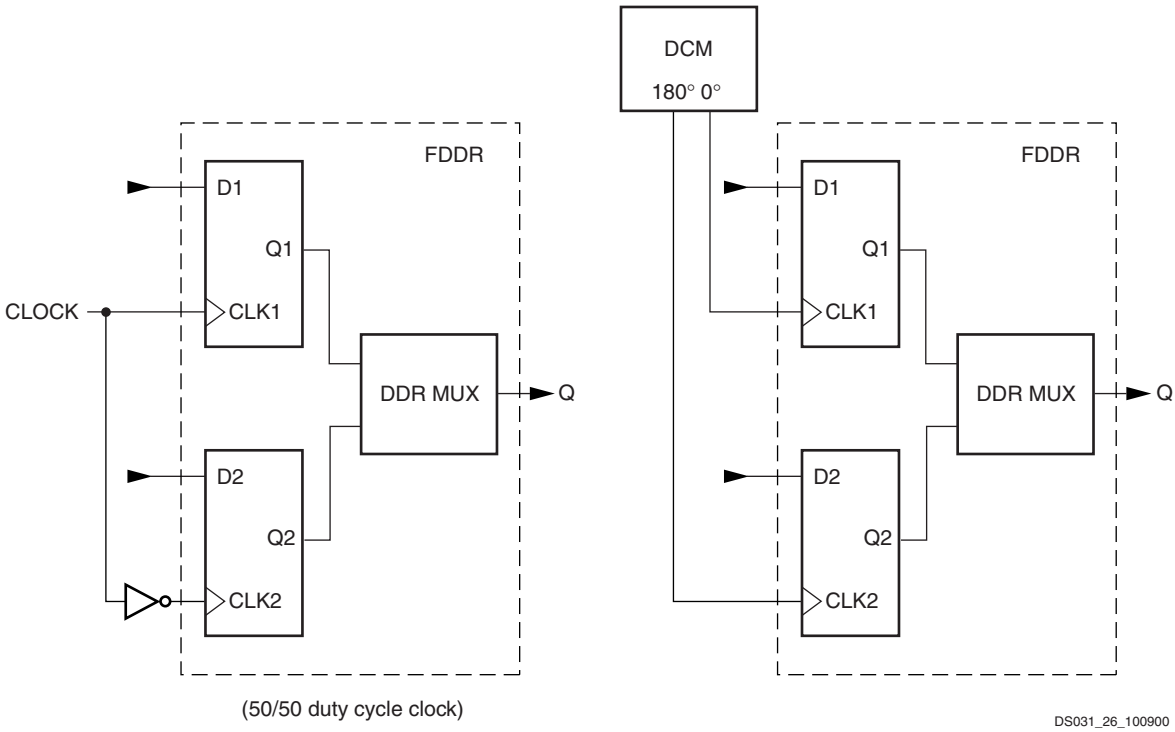


Figure 3: **Double Data Rate Registers**

The DDR mechanism shown in Figure 3 can be used to mirror a copy of the clock on the output. This is useful for propagating a clock along the data that has an identical delay. It is also useful for multiple clock generation, where there is a unique clock driver for every clock load. Virtex-II devices can produce many copies of a clock with very little skew.

Each group of two registers has a clock enable signal (ICE for the input registers, OCE for the output registers, and TCE for the 3-state registers). The clock enable signals are active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

Each IOB block has common synchronous or asynchronous set and reset (SR and REV signals).

SR forces the storage element into the state specified by the SRHIGH or SRLOW attribute. SRHIGH forces a logic “1”. SRLOW forces a logic “0”. When SR is used, a second input (REV) forces the storage element into the opposite state. The reset condition predominates over the set condition. The initial state after configuration or global initialization state is defined by a separate INIT0 and INIT1 attribute. By default, the SRLOW attribute forces INIT0, and the SRHIGH attribute forces INIT1.

For each storage element, the SRHIGH, SRLOW, INIT0, and INIT1 attributes are independent. Synchronous or asynchronous set / reset is consistent in an IOB block.

All the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Each register or latch (independent of all other registers or latches) (see Figure 4) can be configured as follows:

- No set or reset
- Synchronous set
- Synchronous reset
- Synchronous set and reset
- Asynchronous set (preset)
- Asynchronous reset (clear)
- Asynchronous set and reset (preset and clear)

The synchronous reset overrides a set, and an asynchronous clear overrides a preset.

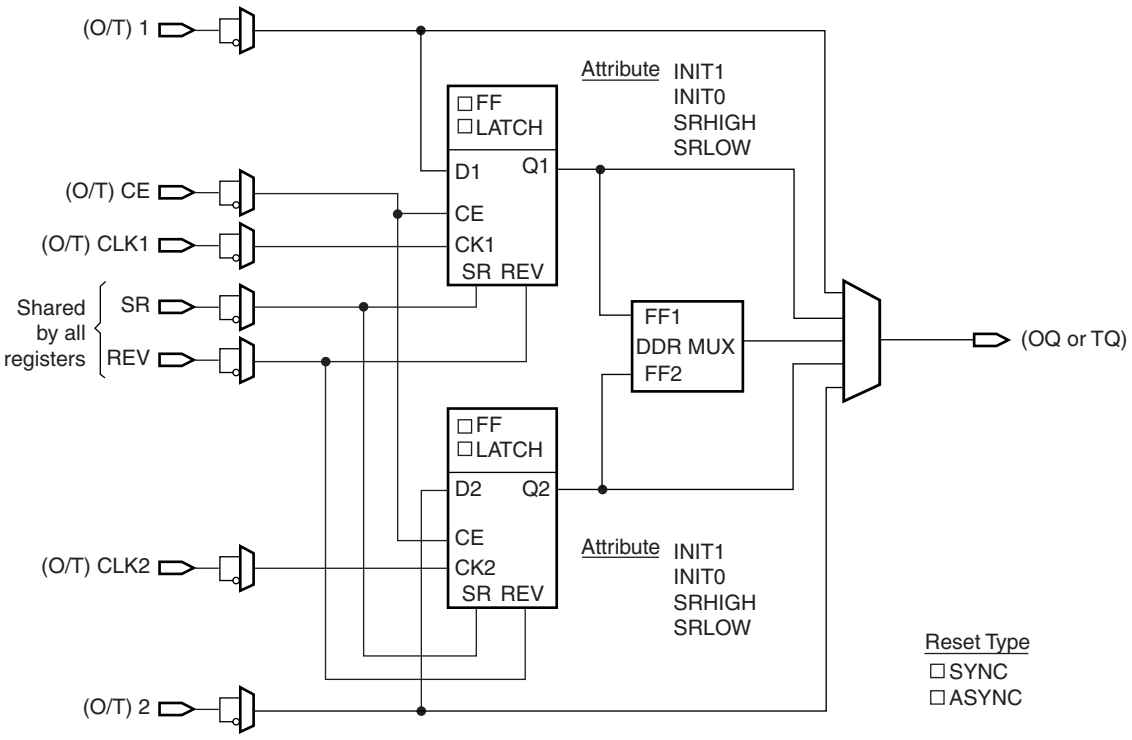


Figure 4: **Register / Latch Configuration in an IOB Block**

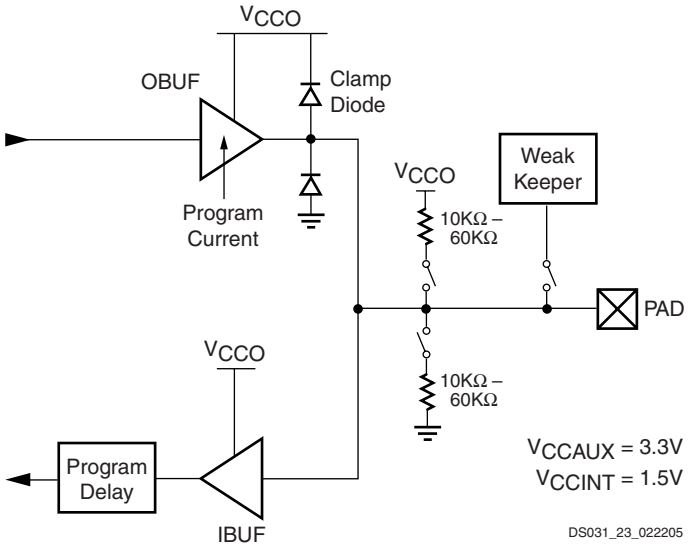


Figure 5: **LVTTL, LVCMOS or PCI SelectI/O-Ultra Standards**

Input/Output Individual Options

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V_{CCO} when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O-Ultra standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

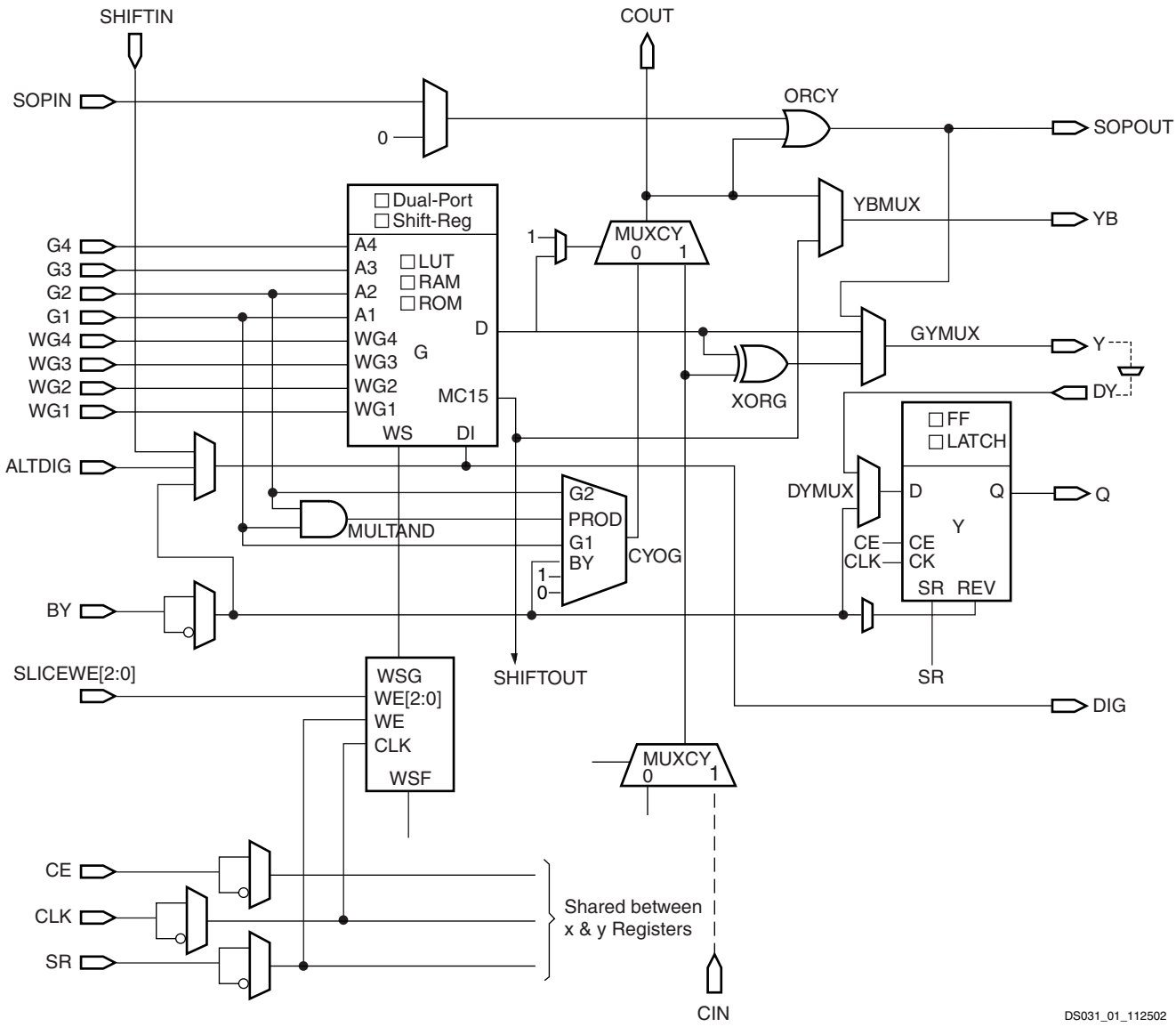


Figure 16: **Virtex-II Slice (Top Half)**

Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 35.

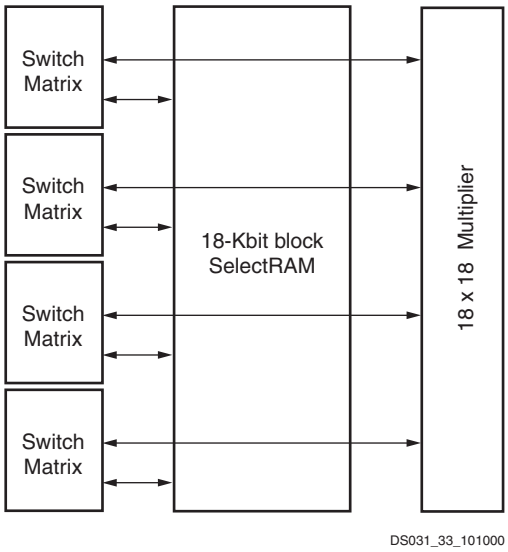


Figure 35: **SelectRAM and Multiplier Blocks**

Association With Block SelectRAM Memory

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 36 shows a multiplier block.

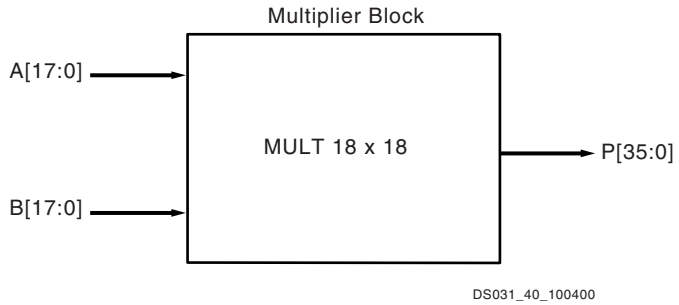


Figure 36: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kbit SelectRAM organization, because each multiplier is associated with an 18 Kbit block SelectRAM resource.

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs)).

Table 20: **Multiplier Floor Plan**

Device	Columns	Multipliers	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

Creating a Design

Creating Virtex-II designs is easy with Xilinx Integrated Synthesis Environment (ISE) development systems, which support advanced design capabilities, including ProActive Timing Closure, integrated logic analysis, and the fastest place and route runtimes in the industry. ISE solutions enable designers to get the performance they need, quickly and easily.

As a result of the ongoing cooperative development efforts between Xilinx and EDA Alliance partners, designers can take advantage of the benefits provided by EDA technologies in the programmable logic design process. Xilinx development systems are available in a number of easy to use configurations, collectively known as the ISE Series.

ISE Alliance

The ISE Alliance solution is designed to plug and play within an existing design environment. Built using industry standard data formats and netlists, these stable, flexible products enable Alliance EDA partners to deliver their best design automation capabilities to Xilinx customers, along with the time to market benefits of ProActive Timing Closure.

ISE Foundation

The ISE Foundation solution delivers the benefits of true HDL-based design in a seamlessly integrated design environment. An intuitive project navigator, as well as powerful HDL design and two HDL synthesis tools, ensure that high-quality results are achieved quickly and easily. The ISE Foundation product includes:

- State Diagram entry using Xilinx StateCAD
- Automatic HDL Testbench generation using Xilinx HDLBencher
- HDL Simulation using ModelSim XE

Design Flow

Virtex-II design flow proceeds as follows:

- Design Entry
- Synthesis
- Implementation
- Verification

Most programmable logic designers iterate through these steps several times in the process of completing a design.

Design Entry

All Xilinx ISE development systems support the mainstream EDA design entry capabilities, ranging from schematic design to advanced HDL design methodologies. Given the high densities of the Virtex-II family, designs are created most efficiently using HDLs. To further improve their time to market, many Xilinx customers employ incremental, modular, and Intellectual Property (IP) design techniques. When properly used, these techniques further accelerate the logic design process.

To enable designers to leverage existing investments in EDA tools, and to ensure high performance design flows, Xilinx jointly develops tools with leading EDA vendors, including:

- Aldec®
- Cadence®
- Exemplar®
- Mentor Graphics®
- Model Technology®
- Synopsys®
- Synplicity®

Complete information on Alliance Series partners and their associated design flows is available at www.xilinx.com on the Xilinx Alliance Series web page.

The ISE Foundation product offers schematic entry and HDL design capabilities as part of an integrated design solution - enabling one-stop shopping. These capabilities are powerful, easy to use, and they support the full portfolio of Xilinx programmable logic devices. HDL design capabilities include a color-coded HDL editor with integrated language templates, state diagram entry, and Core generation capabilities.

Synthesis

The ISE Alliance product is engineered to support advanced design flows with the industry's best synthesis tools. Advanced design methodologies include:

- Physical Synthesis
- Incremental synthesis
- RTL floorplanning
- Direct physical mapping

The ISE Foundation product seamlessly integrates synthesis capabilities purchased directly from Exemplar, Synopsys, and Synplicity. In addition, it includes the capabilities of Xilinx Synthesis Technology.

A benefit of having two seamlessly integrated synthesis engines within an ISE design flow is the ability to apply alternative sets of optimization techniques on designs, helping to ensure that designers can meet even the toughest timing requirements.

Design Implementation

The ISE Series development systems include Xilinx timing-driven implementation tools, frequently called “place and route” or “fitting” software. This robust suite of tools enables the creation of an intuitive, flexible, tightly integrated design flow that efficiently bridges “logical” and “physical” design domains. This simplifies the task of defining a design, including its behavior, timing requirements, and optional layout (or floorplanning), as well as simplifying the task of analyzing reports generated during the implementation process.

Input Clock Tolerances

Table 39: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word “monotonically” to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

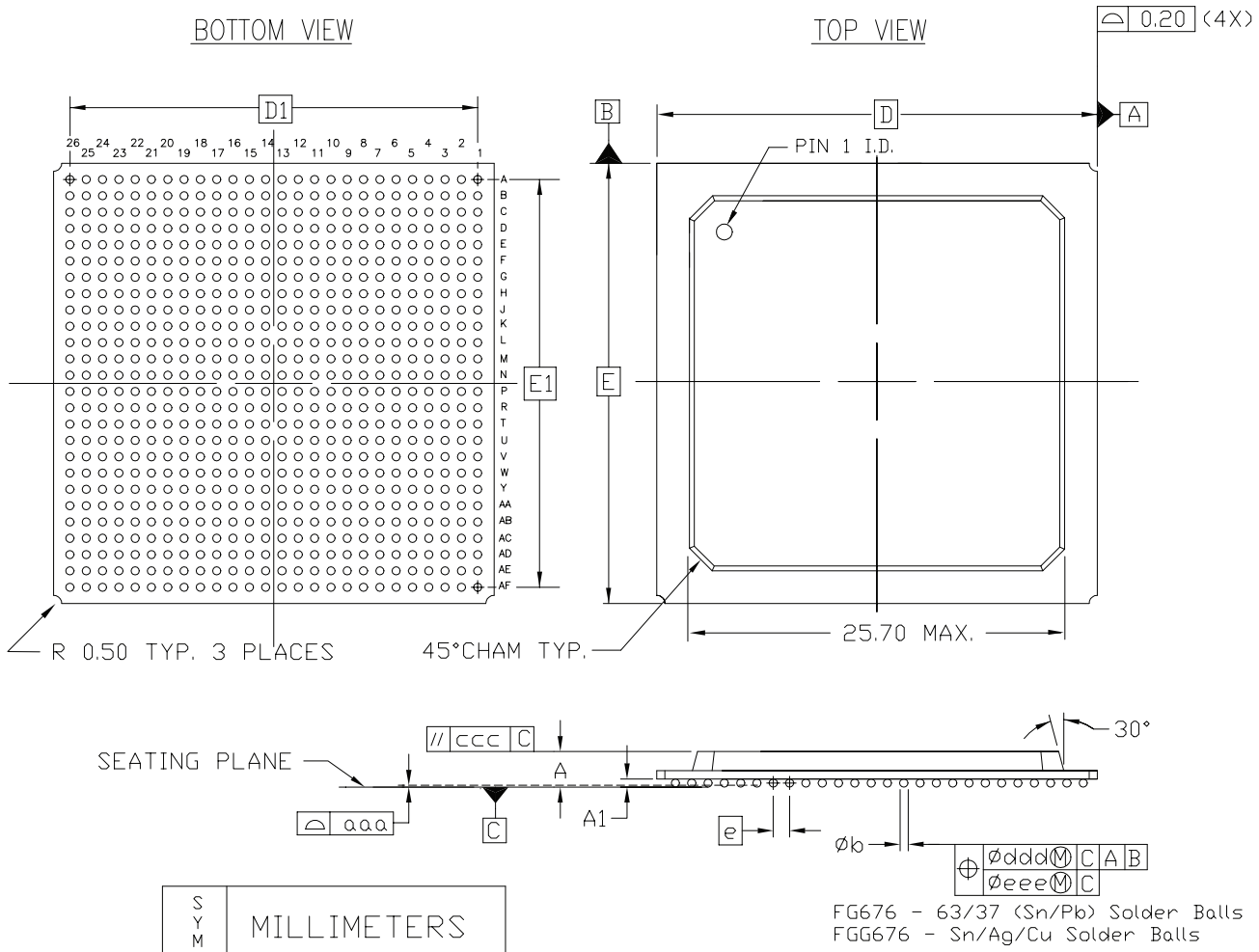
Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
4	IO_L91N_4/VREF_4	R11	NC	NC
4	IO_L91P_4	T11	NC	NC
4	IO_L92N_4	M11	NC	NC
4	IO_L92P_4	M10	NC	NC
4	IO_L93N_4	N10	NC	NC
4	IO_L93P_4	P10	NC	NC
4	IO_L94N_4/VREF_4	R10		
4	IO_L94P_4	T10		
4	IO_L95N_4/GCLK3S	N9		
4	IO_L95P_4/GCLK2P	P9		
4	IO_L96N_4/GCLK1S	R9		
4	IO_L96P_4/GCLK0P	T9		
5	IO_L96N_5/GCLK7S	T8		
5	IO_L96P_5/GCLK6P	R8		
5	IO_L95N_5/GCLK5S	P8		
5	IO_L95P_5/GCLK4P	N8		
5	IO_L94N_5	T7		
5	IO_L94P_5/VREF_5	R7		
5	IO_L93N_5	P7	NC	NC
5	IO_L93P_5	N7	NC	NC
5	IO_L92N_5	M7	NC	NC
5	IO_L92P_5	M6	NC	NC
5	IO_L91N_5	T6	NC	NC
5	IO_L91P_5/VREF_5	R6	NC	NC
5	IO_L05N_5/VRP_5	P6	NC	NC
5	IO_L05P_5/VRN_5	N6	NC	NC
5	IO_L04N_5	T5	NC	NC
5	IO_L04P_5/VREF_5	R5	NC	NC
5	IO_L03N_5/D4/ALT_VRP_5	P5		
5	IO_L03P_5/D5/ALT_VRN_5	N5		
5	IO_L02N_5/D6	R4		
5	IO_L02P_5/D7	P4		
5	IO_L01N_5/RDWR_B	T4		

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
7	IO_L45N_7	F5	NC	NC
7	IO_L43P_7	F1	NC	NC
7	IO_L43N_7	F2	NC	NC
7	IO_L06P_7	F3	NC	
7	IO_L06N_7	F4	NC	
7	IO_L04P_7	E1	NC	
7	IO_L04N_7	E2	NC	
7	IO_L03P_7/VREF_7	E3		
7	IO_L03N_7	E4		
7	IO_L02P_7/VRN_7	D2		
7	IO_L02N_7/VRP_7	D3		
7	IO_L01P_7	D1		
7	IO_L01N_7	C1		
0	VCCO_0	F8		
0	VCCO_0	F7		
0	VCCO_0	E8		
1	VCCO_1	F10		
1	VCCO_1	F9		
1	VCCO_1	E9		
2	VCCO_2	H12		
2	VCCO_2	H11		
2	VCCO_2	G11		
3	VCCO_3	K11		
3	VCCO_3	J12		
3	VCCO_3	J11		
4	VCCO_4	M9		
4	VCCO_4	L10		
4	VCCO_4	L9		
5	VCCO_5	M8		
5	VCCO_5	L8		
5	VCCO_5	L7		
6	VCCO_6	K6		
6	VCCO_6	J6		

FG676/FGG676 Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.25	2.60
A_1	0.40	0.50	0.60
D/E	27.00 BSC		
D_1/E_1	25.00 REF		
e	1.00 BSC		
øb	0.50	0.60	0.70
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.10
M	26		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

676-BALL FINE PITCH BGA (FG676/FGG676)

Figure 4: **FG676/FGG676 Fine-Pitch BGA Package Specifications**

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
4	IO_L27P_4/VREF_4	AG19
4	IO_L28N_4	AB19
4	IO_L28P_4	AA19
4	IO_L30N_4	AC19
4	IO_L30P_4	AD19
4	IO_L49N_4	AE19
4	IO_L49P_4	AF19
4	IO_L51N_4	AA18
4	IO_L51P_4/VREF_4	Y18
4	IO_L52N_4	AB18
4	IO_L52P_4	AC18
4	IO_L54N_4	AD18
4	IO_L54P_4	AE18
4	IO_L67N_4	AF18
4	IO_L67P_4	AG18
4	IO_L69N_4	AA17
4	IO_L69P_4/VREF_4	Y17
4	IO_L70N_4	AB17
4	IO_L70P_4	AB16
4	IO_L72N_4	AD17
4	IO_L72P_4	AE17
4	IO_L73N_4	AF17
4	IO_L73P_4	AG17
4	IO_L75N_4	Y16
4	IO_L75P_4/VREF_4	W16
4	IO_L76N_4	AC16
4	IO_L76P_4	AD16
4	IO_L78N_4	AF16
4	IO_L78P_4	AG16
4	IO_L91N_4/VREF_4	W15
4	IO_L91P_4	Y15
4	IO_L92N_4	AB15
4	IO_L92P_4	AA15
4	IO_L93N_4	AC15
4	IO_L93P_4	AD15
4	IO_L94N_4/VREF_4	AE15

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L78P_7	N6
7	IO_L78N_7	N7
7	IO_L76P_7	N9
7	IO_L76N_7	N8
7	IO_L75P_7/VREF_7	N5
7	IO_L75N_7	M6
7	IO_L73P_7	M1
7	IO_L73N_7	M2
7	IO_L72P_7	M4
7	IO_L72N_7	M5
7	IO_L70P_7	M8
7	IO_L70N_7	M9
7	IO_L69P_7/VREF_7	L1
7	IO_L69N_7	L2
7	IO_L67P_7	L3
7	IO_L67N_7	L4
7	IO_L54P_7	K1
7	IO_L54N_7	K2
7	IO_L52P_7	K4
7	IO_L52N_7	K5
7	IO_L51P_7/VREF_7	L6
7	IO_L51N_7	L7
7	IO_L49P_7	K6
7	IO_L49N_7	K7
7	IO_L48P_7	L8
7	IO_L48N_7	K8
7	IO_L46P_7	J1
7	IO_L46N_7	H1
7	IO_L45P_7/VREF_7	J2
7	IO_L45N_7	J3
7	IO_L43P_7	K3
7	IO_L43N_7	J4
7	IO_L30P_7	H3
7	IO_L30N_7	H4
7	IO_L28P_7	J5
7	IO_L28N_7	J6

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L48N_2	J5		
2	IO_L48P_2	H5		
2	IO_L49N_2	J3		
2	IO_L49P_2	H3		
2	IO_L50N_2	K7		
2	IO_L50P_2	L7		
2	IO_L51N_2	J4		
2	IO_L51P_2/VREF_2	K4		
2	IO_L52N_2	K1		
2	IO_L52P_2	J1		
2	IO_L53N_2	L6		
2	IO_L53P_2	M6		
2	IO_L54N_2	L5		
2	IO_L54P_2	K5		
2	IO_L67N_2	L2	NC	
2	IO_L67P_2	K2	NC	
2	IO_L68N_2	M8	NC	
2	IO_L68P_2	N8	NC	
2	IO_L69N_2	L4	NC	
2	IO_L69P_2/VREF_2	M4	NC	
2	IO_L70N_2	M1	NC	
2	IO_L70P_2	L1	NC	
2	IO_L71N_2	M7	NC	
2	IO_L71P_2	N7	NC	
2	IO_L72N_2	M3	NC	
2	IO_L72P_2	L3	NC	
2	IO_L73N_2	N2	NC	NC
2	IO_L73P_2	M2	NC	NC
2	IO_L74N_2	N6	NC	NC
2	IO_L74P_2	P6	NC	NC
2	IO_L75N_2	N5	NC	NC
2	IO_L75P_2/VREF_2	N4	NC	NC
2	IO_L76N_2	P1	NC	NC
2	IO_L76P_2	N1	NC	NC
2	IO_L77N_2	P9	NC	NC
2	IO_L77P_2	R9	NC	NC
2	IO_L78N_2	R5	NC	NC

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L30N_0	F23	
0	IO_L30P_0	F24	
0	IO_L49N_0	B28	
0	IO_L49P_0	B29	
0	IO_L50N_0	J22	
0	IO_L50P_0	J21	
0	IO_L51N_0	A28	
0	IO_L51P_0/VREF_0	A29	
0	IO_L52N_0	A26	
0	IO_L52P_0	B27	
0	IO_L53N_0	C24	
0	IO_L53P_0	D24	
0	IO_L54N_0	D22	
0	IO_L54P_0	D23	
0	IO_L60N_0	B25	NC
0	IO_L60P_0	B26	NC
0	IO_L67N_0	B23	
0	IO_L67P_0	B24	
0	IO_L68N_0	G22	
0	IO_L68P_0	G23	
0	IO_L69N_0	F22	
0	IO_L69P_0/VREF_0	F21	
0	IO_L70N_0	A23	
0	IO_L70P_0	A24	
0	IO_L71N_0	K21	
0	IO_L71P_0	K20	
0	IO_L72N_0	C22	
0	IO_L72P_0	C23	
0	IO_L73N_0	E21	
0	IO_L73P_0	E22	
0	IO_L74N_0	H21	
0	IO_L74P_0	H20	
0	IO_L75N_0	G20	
0	IO_L75P_0/VREF_0	F20	
0	IO_L76N_0	B21	
0	IO_L76P_0	B22	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L21N_2	H7	
2	IO_L21P_2/VREF_2	J7	
2	IO_L22N_2	H6	
2	IO_L22P_2	G6	
2	IO_L23N_2	L10	
2	IO_L23P_2	L9	
2	IO_L24N_2	G3	
2	IO_L24P_2	F3	
2	IO_L25N_2	G2	
2	IO_L25P_2	F2	
2	IO_L26N_2	M10	
2	IO_L26P_2	N10	
2	IO_L27N_2	J6	
2	IO_L27P_2/VREF_2	K6	
2	IO_L28N_2	J5	
2	IO_L28P_2	H5	
2	IO_L29N_2	L7	
2	IO_L29P_2	K7	
2	IO_L30N_2	J4	
2	IO_L30P_2	H4	
2	IO_L43N_2	G1	
2	IO_L43P_2	F1	
2	IO_L44N_2	L8	
2	IO_L44P_2	M8	
2	IO_L45N_2	J1	
2	IO_L45P_2/VREF_2	H2	
2	IO_L46N_2	J3	
2	IO_L46P_2	H3	
2	IO_L47N_2	M9	
2	IO_L47P_2	N9	
2	IO_L48N_2	L5	
2	IO_L48P_2	K5	
2	IO_L49N_2	K2	
2	IO_L49P_2	J2	
2	IO_L50N_2	N7	
2	IO_L50P_2	M7	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L93N_1	E19		
1	IO_L93P_1	E20		
1	IO_L92N_1	J19		
1	IO_L92P_1	J18		
1	IO_L91N_1	A18		
1	IO_L91P_1/VREF_1	A19		
1	IO_L84N_1	D18		
1	IO_L84P_1	D19		
1	IO_L83N_1	K19		
1	IO_L83P_1	K18		
1	IO_L82N_1	B18		
1	IO_L82P_1	B19		
1	IO_L81N_1/VREF_1	G18		
1	IO_L81P_1	G19		
1	IO_L80N_1	E18		
1	IO_L80P_1	E17		
1	IO_L79N_1	A16		
1	IO_L79P_1	A17		
1	IO_L78N_1	F17		
1	IO_L78P_1	F18		
1	IO_L77N_1	L19		
1	IO_L77P_1	L18		
1	IO_L76N_1	B16		
1	IO_L76P_1	B17		
1	IO_L75N_1/VREF_1	G16		
1	IO_L75P_1	G17		
1	IO_L74N_1	M19		
1	IO_L74P_1	M18		
1	IO_L73N_1	C16		
1	IO_L73P_1	C17		
1	IO_L72N_1	D15		
1	IO_L72P_1	D16		
1	IO_L71N_1	J17		
1	IO_L71P_1	J16		
1	IO_L70N_1	A14		
1	IO_L70P_1	A15		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L55N_5	AV28		
5	IO_L55P_5	AV27		
5	IO_L54N_5	AP27		
5	IO_L54P_5	AP26		
5	IO_L53N_5	AN25		
5	IO_L53P_5	AN26		
5	IO_L52N_5	AU29		
5	IO_L52P_5	AU28		
5	IO_L51N_5/VREF_5	AR28		
5	IO_L51P_5	AR27		
5	IO_L50N_5	AJ24		
5	IO_L50P_5	AJ25		
5	IO_L49N_5	AW30		
5	IO_L49P_5	AW29		
5	IO_L36N_5	AT29	NC	
5	IO_L36P_5	AT28	NC	
5	IO_L35N_5	AK25	NC	
5	IO_L35P_5	AL26	NC	
5	IO_L34N_5	AV31	NC	
5	IO_L34P_5	AV30	NC	
5	IO_L33N_5/VREF_5	AP29	NC	
5	IO_L33P_5	AP28	NC	
5	IO_L32N_5	AK26	NC	
5	IO_L32P_5	AJ26	NC	
5	IO_L31N_5	AW32	NC	
5	IO_L31P_5	AW31	NC	
5	IO_L30N_5	AM27		
5	IO_L30P_5	AM26		
5	IO_L29N_5	AN28		
5	IO_L29P_5	AN29		
5	IO_L28N_5	AU31		
5	IO_L28P_5	AU30		
5	IO_L27N_5/VREF_5	AT31		
5	IO_L27P_5	AT30		
5	IO_L26N_5	AH25		
5	IO_L26P_5	AH26		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	
7	IO_L53P_7	L30	