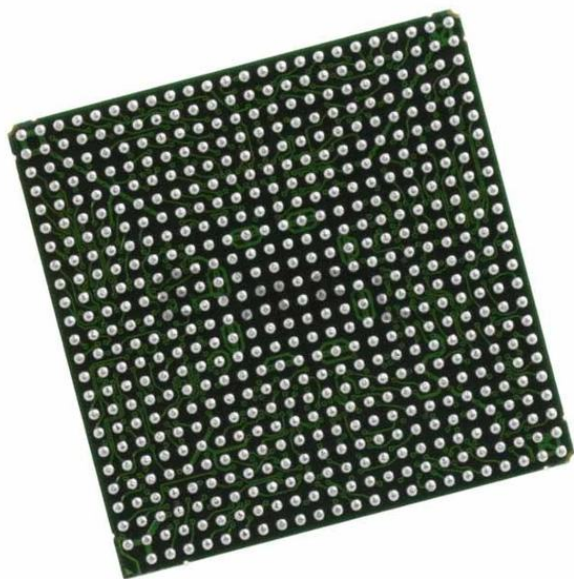




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

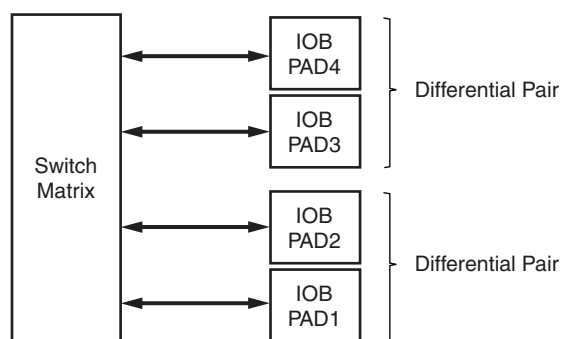
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	328
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-5bgg575i

Detailed Description

Input/Output Blocks (IOBs)

Virtex-II™ I/O blocks (IOBs) are provided in groups of two or four on the perimeter of each device. Each IOB can be used as input and/or output for single-ended I/Os. Two IOBs can be used as a differential pair. A differential pair is always connected to the same switch matrix, as shown in **Figure 1**.

IOB blocks are designed for high performances I/Os, supporting 19 single-ended standards, as well as differential signaling with LVDS, LDT, Bus LVDS, and LVPECL.



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Figure 1: Virtex-II Input/Output Tile

Note: Differential I/Os must use the same clock.

Supported I/O Standards

Virtex-II IOB blocks feature SelectI/O-Ultra inputs and outputs that support a wide variety of I/O signaling standards. In addition to the internal supply voltage ($V_{CCINT} = 1.5V$), output driver supply voltage (V_{CCO}) is dependent on the I/O standard (see **Table 1** and **Table 2**). An auxiliary supply voltage ($V_{CCAUX} = 3.3V$) is required, regardless of the I/O standard used. For exact supply voltage absolute maximum ratings, see **DC Input and Output Levels** in Module 3.

All of the user IOBs have fixed-clamp diodes to V_{CCO} and to ground. As outputs, these IOBs are not compatible or compliant with 5V I/O standards. As inputs, these IOBs are not normally 5V tolerant, but can be used with 5V I/O standards when external current-limiting resistors are used. For more details, see the “5V Tolerant I/Os” Tech Topic at www.xilinx.com.

Table 3 lists supported I/O standards with Digitally Controlled Impedance. See **Digitally Controlled Impedance (DCI)**, page 8.

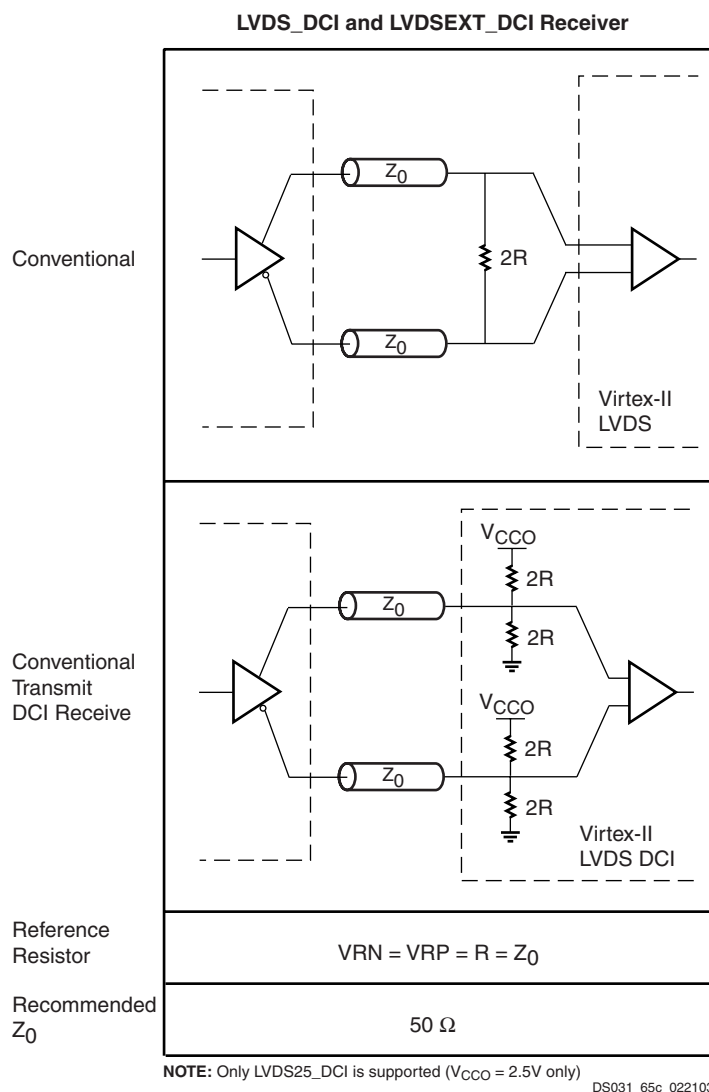
Table 1: Supported Single-Ended I/O Standards

IOSTANDARD Attribute	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/R ⁽³⁾	N/R
LVC MOS33	3.3	3.3	N/R	N/R
LVC MOS25	2.5	2.5	N/R	N/R
LVC MOS18	1.8	1.8	N/R	N/R
LVC MOS15	1.5	1.5	N/R	N/R
PCI33_3	3.3	3.3	N/R	N/R
PCI66_3	3.3	3.3	N/R	N/R
PCI-X	3.3	3.3	N/R	N/R
GTL	Note (1)	Note (1)	0.8	1.2
GTLP	Note (1)	Note (1)	1.0	1.5
HSTL_I	1.5	N/R	0.75	0.75
HSTL_II	1.5	N/R	0.75	0.75
HSTL_III	1.5	N/R	0.9	1.5
HSTL_IV	1.5	N/R	0.9	1.5
HSTL_I_18	1.8	N/R	0.9	0.9
HSTL_II_18	1.8	N/R	0.9	0.9
HSTL_III_18	1.8	N/R	1.1	1.8
HSTL_IV_18	1.8	N/R	1.1	1.8
SSTL18_I ⁽²⁾	1.8	N/R	0.9	0.9
SSTL18_II	1.8	N/R	0.9	0.9
SSTL2_I	2.5	N/R	1.25	1.25
SSTL2_II	2.5	N/R	1.25	1.25
SSTL3_I	3.3	N/R	1.5	1.5
SSTL3_II	3.3	N/R	1.5	1.5
AGP-2X/AGP	3.3	N/R	1.32	N/R

Notes:

- V_{CCO} of GTL or GTLP should not be lower than the termination voltage or the voltage seen at the I/O pad. Example: If the pin High level is 1.5V, connect V_{CCO} to 1.5V.
- SSTL18_I is not a JEDEC-supported standard.
- N/R = no requirement.

Figure 13 provides examples illustrating the use of the LVDS_DCI and LVDS25_DCI I/O standards. For a complete list, see the [Virtex-II Platform FPGA User Guide](#).



NOTE: Only LVDS25_DCI is supported ($V_{CCO} = 2.5V$ only)

Figure 13: LVDS DCI Usage Examples

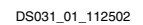


Figure 16: Virtex-II Slice (Top Half)

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing

large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

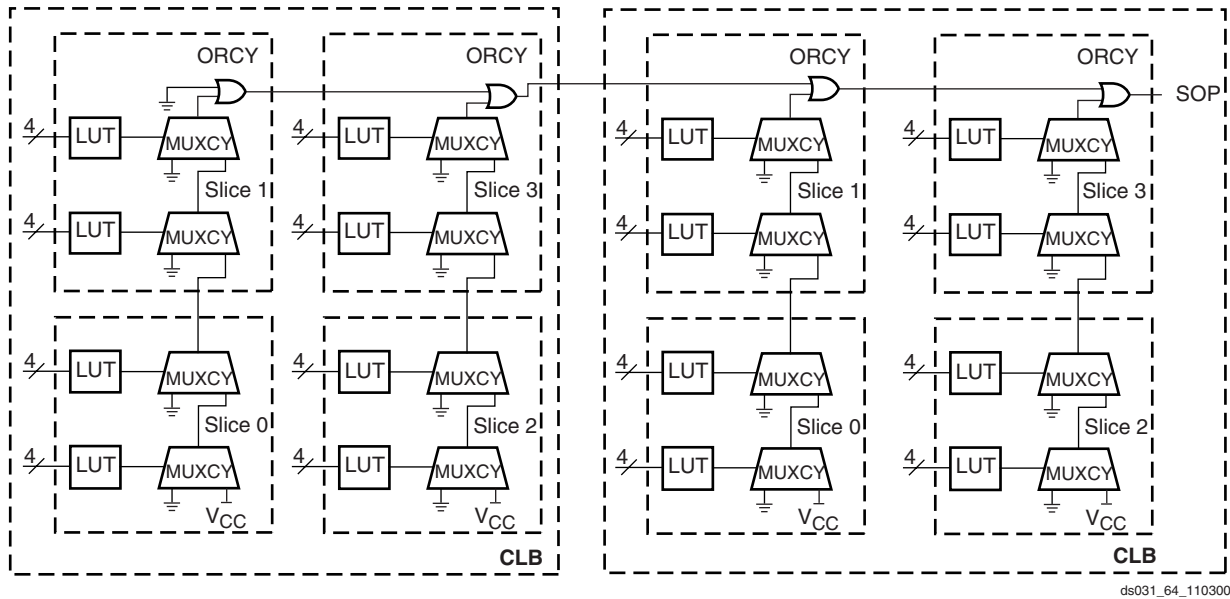


Figure 25: Horizontal Cascade Chain

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates

LUT and MUXCY resources configured as a 16-input AND gate.

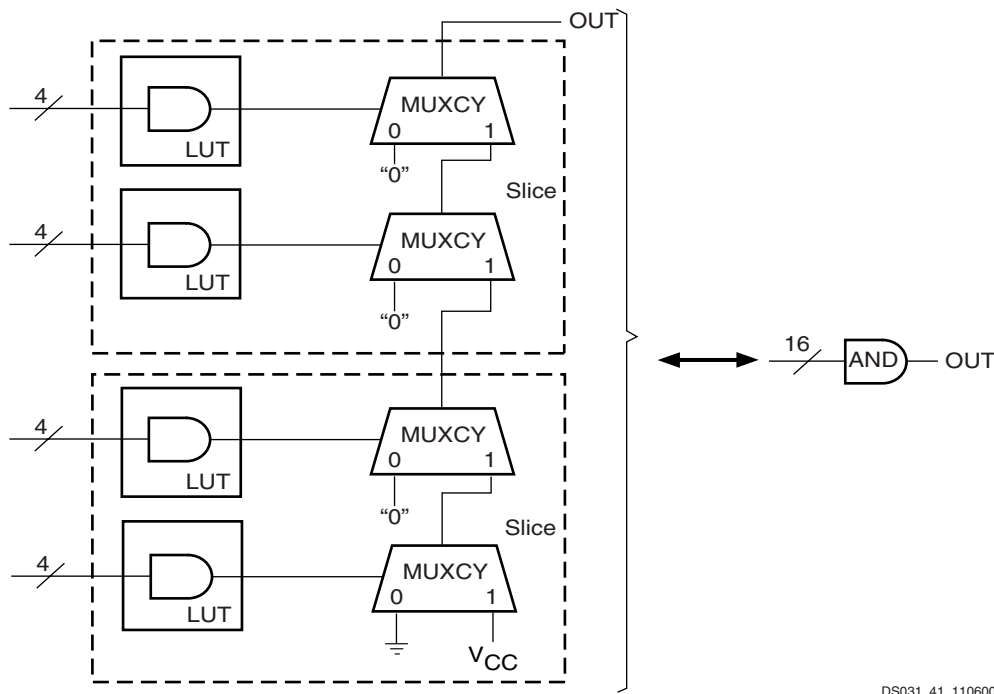


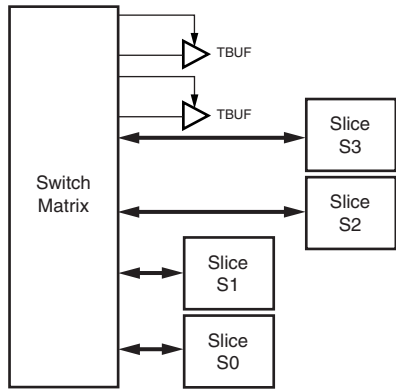
Figure 26: Wide-Input AND Gate (16 Inputs)

3-State Buffers

Introduction

Each Virtex-II CLB contains two 3-state drivers (TBUFs) that can drive on-chip busses. Each 3-state buffer has its own 3-state control pin and its own input pin.

Each of the four slices have access to the two 3-state buffers through the switch matrix, as shown in Figure 27. TBUFs in neighboring CLBs can access slice outputs by direct connects. The outputs of the 3-state buffers drive horizontal routing resources used to implement 3-state busses.



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Figure 27: Virtex-II 3-State Buffers

The 3-state buffer logic is implemented using AND-OR logic rather than 3-state drivers, so that timing is more predictable and less load dependant especially with larger devices.

Locations / Organization

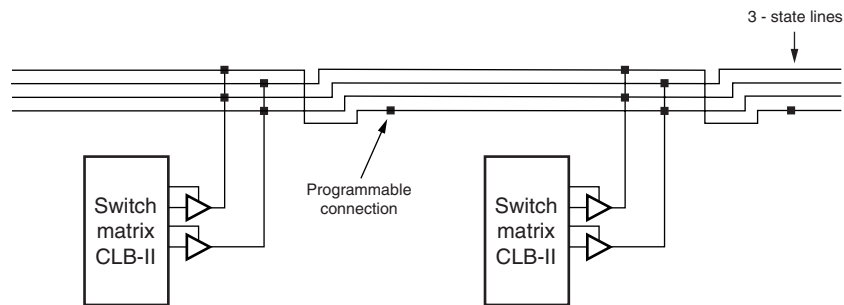
Four horizontal routing resources per CLB are provided for on-chip 3-state busses. Each 3-state buffer has access alternately to two horizontal lines, which can be partitioned as shown in Figure 28. The switch matrices corresponding to SelectRAM memory and multiplier or I/O blocks are skipped.

Number of 3-State Buffers

Table 11 shows the number of 3-state buffers available in each Virtex-II device. The number of 3-state buffers is twice the number of CLB elements.

Table 11: Virtex-II 3-State Buffers

Device	3-State Buffers per Row	Total Number of 3-State Buffers
XC2V40	16	128
XC2V80	16	256
XC2V250	32	768
XC2V500	48	1,536
XC2V1000	64	2,560
XC2V1500	80	3,840
XC2V2000	96	5,376
XC2V3000	112	7,168
XC2V4000	144	11,520
XC2V6000	176	16,896
XC2V8000	208	23,296



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Figure 28: 3-State Buffer Connection to Horizontal Lines

CLB/Slice Configurations

Table 12 summarizes the logic resources in one CLB. All of the CLBs are identical and each CLB or slice can be implemented in one of the configurations listed. Table 13 shows the available resources in all CLBs.

Table 12: Logic Resources in One CLB

Slices	LUTs	Flip-Flops	MULT_ANDs	Arithmetic & Carry-Chains	SOP Chains	Distributed SelectRAM	Shift Registers	TBUF
4	8	8	8	2	2	128 bits	128 bits	2

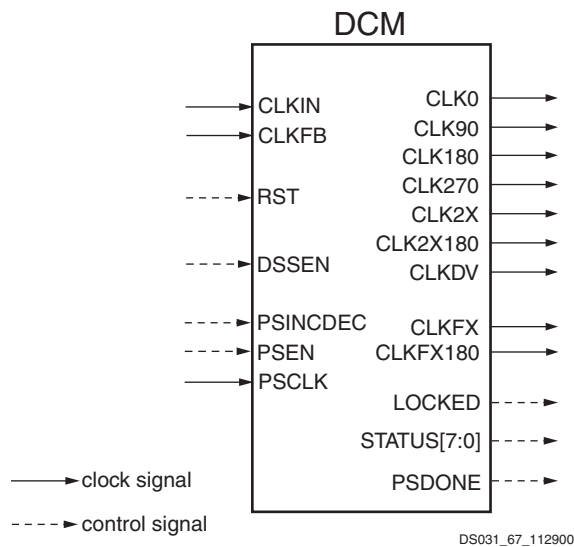


Figure 45: Digital Clock Manager

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 21.

Table 21: DCM Status Pins

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock,

can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$\text{FREQ}_{\text{CLKFX}} = (\text{M}/\text{D}) * \text{FREQ}_{\text{CLKIN}}$$

where M and D are two integers. Specifications for M and D are provided under **DCM Timing Parameters** in Module 3. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 46 illustrates the effects of fine-phase shifting. For more information on DCM features, see the Virtex-II User Guide.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new

IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: Virtex-II Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M2	M1	M0	CCLK Direction	Data Width	Serial D _{OUT} ⁽²⁾
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: Virtex-II Bitstream Lengths

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V,

and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Virtex-II Switching Characteristics

Switching characteristics in this document are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Note that **Virtex-II Performance Characteristics, page 7** are subject to these guidelines as well. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. **Table 13** correlates the current status of each Virtex-II device with a corresponding speed grade designation.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the Xilinx static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-II devices.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments, page 11**.

Table 13: Virtex-II Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC2V40			-6, -5, -4
XC2V80			-6, -5, -4
XC2V250			-6, -5, -4
XC2V500			-6, -5, -4
XC2V1000			-6, -5, -4
XC2V1500			-6, -5, -4
XC2V2000			-6, -5, -4
XC2V3000			-6, -5, -4
XC2V4000			-6, -5, -4
XC2V6000			-6, -5, -4
XC2V8000			-5, -4

Table 14: IOB Input Switching Characteristics

			Speed Grade			Units
Description	Symbol	Device	-6	-5	-4	
Propagation Delays						
Pad to I output, no delay	T _{IOPI}	All	0.69	0.76	0.88	ns, Max
Pad to I output, with delay	T _{IOPID}	XC2V40	1.92	2.11	2.43	ns, Max
		XC2V80	1.92	2.11	2.43	ns, Max
		XC2V250	1.92	2.11	2.43	ns, Max
		XC2V500	1.92	2.11	2.43	ns, Max
		XC2V1000	1.92	2.11	2.43	ns, Max
		XC2V1500	1.92	2.11	2.43	ns, Max
		XC2V2000	1.92	2.11	2.43	ns, Max
		XC2V3000	1.97	2.16	2.49	ns, Max
		XC2V4000	1.97	2.16	2.49	ns, Max
		XC2V6000	2.10	2.31	2.66	ns, Max
		XC2V8000		2.31	2.66	ns, Max

CS144/CSG144 Chip-Scale BGA Package

As shown in [Table 5](#), XC2V40, XC2V80, and XC2V250 Virtex-II devices are available in the CS144/CSG144 package. Pins in the XC2V40, XC2V80, and XC2V250 devices are the same except for pin differences in the XC2V40 device, shown in the No Connect column. Following this table are the [CS144/CSG144 Chip-Scale BGA Package Specifications \(0.80mm pitch\)](#).

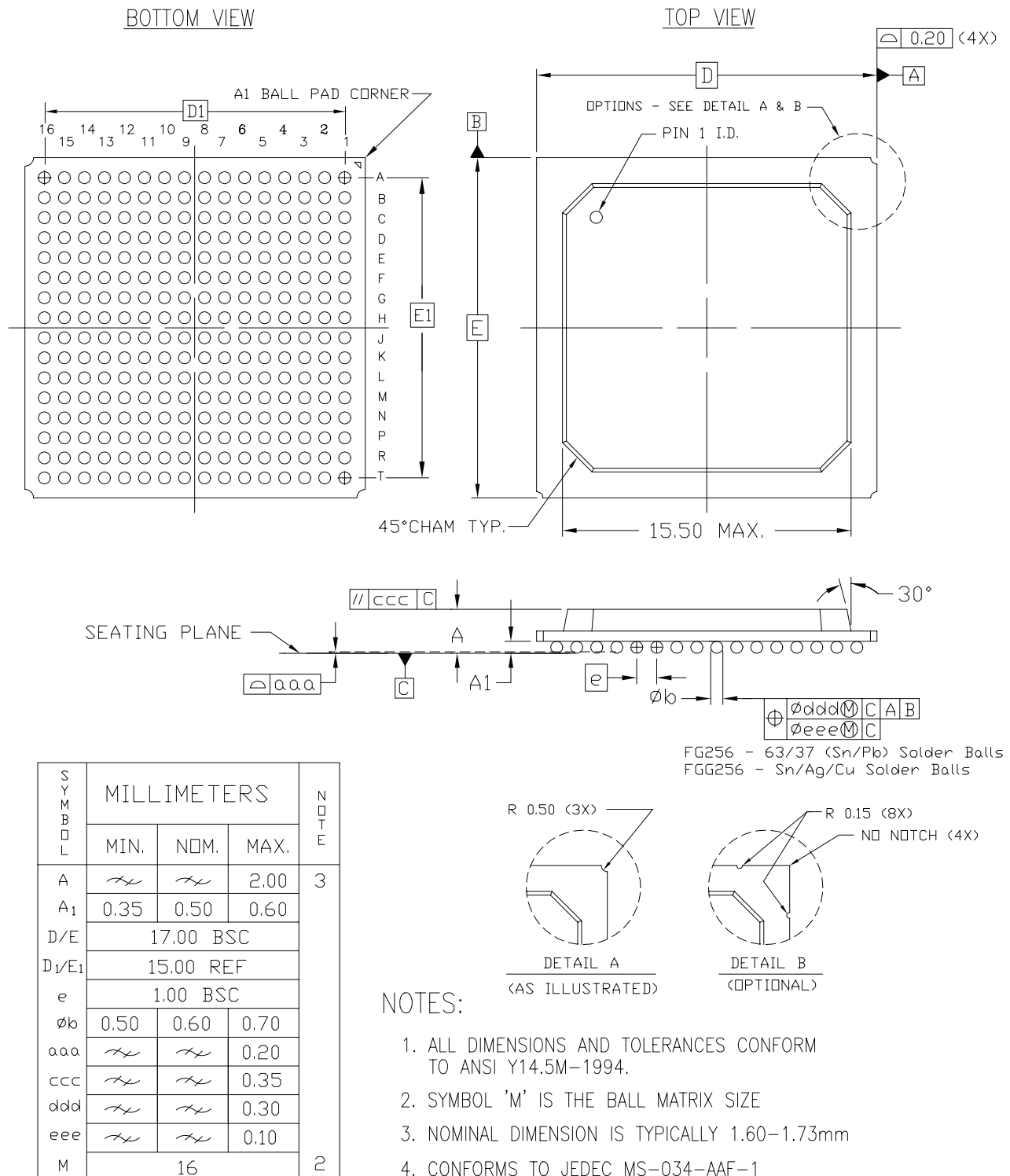
Table 5: CS144/CSG144 — XC2V40, XC2V80, and XC2V250

Bank	Pin Description	Pin Number	No Connect in the XC2V40
0	IO_L01N_0	B3	
0	IO_L01P_0	A3	
0	IO_L02N_0	C4	
0	IO_L02P_0	B4	
0	IO_L03N_0/VRP_0	A4	
0	IO_L03P_0/VRN_0	D5	
0	IO_L94N_0/VREF_0	A5	
0	IO_L94P_0	D6	
0	IO_L95N_0/GCLK7P	C6	
0	IO_L95P_0/GCLK6S	B6	
0	IO_L96N_0/GCLK5P	A6	
0	IO_L96P_0/GCLK4S	D7	
1	IO_L96N_1/GCLK3P	A7	
1	IO_L96P_1/GCLK2S	B7	
1	IO_L95N_1/GCLK1P	A8	
1	IO_L95P_1/GCLK0S	B8	
1	IO_L94N_1	C8	
1	IO_L94P_1/VREF_1	D8	
1	IO_L03N_1/VRP_1	C9	
1	IO_L03P_1/VRN_1	D9	
1	IO_L02N_1	A10	
1	IO_L02P_1	B10	
1	IO_L01N_1	C10	
1	IO_L01P_1	D10	
2	IO_L01N_2	C13	
2	IO_L01P_2	D11	
2	IO_L02N_2/VRP_2	D12	
2	IO_L02P_2/VRN_2	D13	
2	IO_L03N_2	E10	
2	IO_L03P_2/VREF_2	E11	
2	IO_L93N_2	E13	NC
2	IO_L93P_2/VREF_2	F11	NC
2	IO_L94N_2	F12	
2	IO_L94P_2	G10	

Table 6: FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)



256-BALL FINE PITCH BGA (FG256/FGG256)

Figure 2: FG256/FGG256 Fine-Pitch BGA Package Specifications

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
3	IO_L52N_3	T21		
3	IO_L52P_3	T20		
3	IO_L51N_3/VREF_3	R20		
3	IO_L51P_3	R19		
3	IO_L49N_3	W24		
3	IO_L49P_3	W23		
3	IO_L48N_3	U23		
3	IO_L48P_3	V23		
3	IO_L46N_3	U22		
3	IO_L46P_3	U21		
3	IO_L45N_3/VREF_3	V22		
3	IO_L45P_3	V21		
3	IO_L43N_3	U19		
3	IO_L43P_3	U20		
3	IO_L24N_3	T19		
3	IO_L24P_3	T18		
3	IO_L22N_3	R18		
3	IO_L22P_3	R17		
3	IO_L21N_3/VREF_3	Y24		
3	IO_L21P_3	Y23		
3	IO_L19N_3	AA24		
3	IO_L19P_3	AB24		
3	IO_L06N_3	AA23		
3	IO_L06P_3	AA22		
3	IO_L04N_3	Y22		
3	IO_L04P_3	Y21		
3	IO_L03N_3/VREF_3	W21		
3	IO_L03P_3	W20		
3	IO_L02N_3/VRP_3	V20		
3	IO_L02P_3/VRN_3	V19		
3	IO_L01N_3	U18		
3	IO_L01P_3	T17		
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	AD22		
4	IO_L01P_4/INIT_B	AD21		
4	IO_L02N_4/D0/DIN ⁽¹⁾	AA20		

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
4	IO_L19N_4	AK6		
4	IO_L19P_4	AK5		
4	IO_L20N_4	AE9		
4	IO_L20P_4	AE10		
4	IO_L21N_4	AF7		
4	IO_L21P_4/VREF_4	AF8		
4	IO_L22N_4	AK7		
4	IO_L22P_4	AJ6		
4	IO_L23N_4	AD10		
4	IO_L23P_4	AD11		
4	IO_L24N_4	AG8		
4	IO_L24P_4	AG7		
4	IO_L49N_4	AJ8		
4	IO_L49P_4	AJ7		
4	IO_L50N_4	AE11		
4	IO_L50P_4	AE12		
4	IO_L51N_4	AG9		
4	IO_L51P_4/VREF_4	AG10		
4	IO_L52N_4	AK9		
4	IO_L52P_4	AJ9		
4	IO_L53N_4	AH8		
4	IO_L53P_4	AH9		
4	IO_L54N_4	AF11		
4	IO_L54P_4	AF10		
4	IO_L67N_4	AJ11	NC	
4	IO_L67P_4	AJ10	NC	
4	IO_L68N_4	AC12	NC	
4	IO_L68P_4	AC13	NC	
4	IO_L69N_4	AG11	NC	
4	IO_L69P_4/VREF_4	AG12	NC	
4	IO_L70N_4	AK11	NC	
4	IO_L70P_4	AK10	NC	
4	IO_L71N_4	AD12	NC	
4	IO_L71P_4	AD13	NC	
4	IO_L72N_4	AH12	NC	
4	IO_L72P_4	AH11	NC	
4	IO_L73N_4	AJ13	NC	NC

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L69P_1	F13	
1	IO_L68N_1	C11	
1	IO_L68P_1	C12	
1	IO_L67N_1	B11	
1	IO_L67P_1	B12	
1	IO_L60N_1	F11	NC
1	IO_L60P_1	F12	NC
1	IO_L54N_1	D10	
1	IO_L54P_1	D11	
1	IO_L53N_1	G12	
1	IO_L53P_1	G13	
1	IO_L52N_1	B9	
1	IO_L52P_1	B10	
1	IO_L51N_1/VREF_1	B8	
1	IO_L51P_1	A9	
1	IO_L50N_1	K14	
1	IO_L50P_1	K13	
1	IO_L49N_1	A6	
1	IO_L49P_1	A7	
1	IO_L30N_1	D9	
1	IO_L30P_1	C9	
1	IO_L29N_1	H13	
1	IO_L29P_1	H12	
1	IO_L28N_1	C7	
1	IO_L28P_1	C8	
1	IO_L27N_1/VREF_1	E11	
1	IO_L27P_1	E10	
1	IO_L26N_1	J13	
1	IO_L26P_1	K12	
1	IO_L25N_1	B6	
1	IO_L25P_1	B7	
1	IO_L24N_1	E8	
1	IO_L24P_1	E9	
1	IO_L23N_1	G10	
1	IO_L23P_1	G11	
1	IO_L22N_1	A4	

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L26P_7	M31		
7	IO_L26N_7	L31		
7	IO_L25P_7	G38		
7	IO_L25N_7	H38		
7	IO_L24P_7	J34		
7	IO_L24N_7	K34		
7	IO_L23P_7	K32		
7	IO_L23N_7	K31		
7	IO_L22P_7	F39		
7	IO_L22N_7	G39		
7	IO_L21P_7/VREF_7	G36		
7	IO_L21N_7	H36		
7	IO_L20P_7	N28		
7	IO_L20N_7	M28		
7	IO_L19P_7	G37		
7	IO_L19N_7	H37		
7	IO_L12P_7	J33	NC	
7	IO_L12N_7	K33	NC	
7	IO_L11P_7	M29	NC	
7	IO_L11N_7	L28	NC	
7	IO_L10P_7	E38	NC	
7	IO_L10N_7	F38	NC	
7	IO_L09P_7/VREF_7	G35	NC	
7	IO_L09N_7	H35	NC	
7	IO_L08P_7	L30	NC	
7	IO_L08N_7	K29	NC	
7	IO_L07P_7	D39	NC	
7	IO_L07N_7	E39	NC	
7	IO_L06P_7	G34		
7	IO_L06N_7	H34		
7	IO_L05P_7	J32		
7	IO_L05N_7	H33		
7	IO_L04P_7	F36		
7	IO_L04N_7	F37		
7	IO_L03P_7/VREF_7	E36		
7	IO_L03N_7	F35		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AC20		
NA	GND	AC19		
NA	GND	AC18		
NA	GND	AC17		
NA	GND	AC16		
NA	GND	AC8		
NA	GND	AC4		
NA	GND	AB24		
NA	GND	AB23		
NA	GND	AB22		
NA	GND	AB21		
NA	GND	AB20		
NA	GND	AB19		
NA	GND	AB18		
NA	GND	AB17		
NA	GND	AB16		
NA	GND	AA24		
NA	GND	AA23		
NA	GND	AA22		
NA	GND	AA21		
NA	GND	AA20		
NA	GND	AA19		
NA	GND	AA18		
NA	GND	AA17		
NA	GND	AA16		
NA	GND	Y39		
NA	GND	Y36		
NA	GND	Y33		
NA	GND	Y30		
NA	GND	Y24		
NA	GND	Y23		
NA	GND	Y22		
NA	GND	Y21		
NA	GND	Y20		
NA	GND	Y19		
NA	GND	Y18		