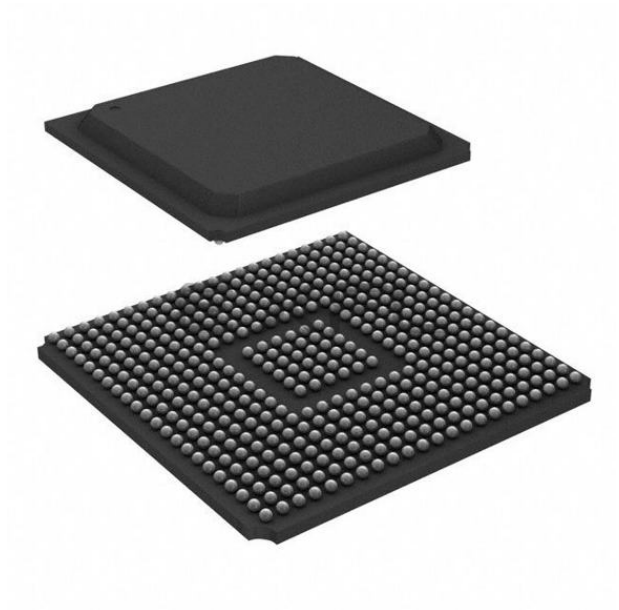

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	324
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-5fgg456c

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Notes:
1. See details in Table 2, "Maximum Number of User I/O Pads".

General Description

The Virtex-II family is a platform FPGA developed for high performance from low-density to high-density designs that are based on IP cores and customized modules. The family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications, including PCI, LVDS, and DDR interfaces.

The leading-edge 0.15 µm / 0.12 µm CMOS 8-layer metal process and the Virtex-II architecture are optimized for high speed with low power consumption. Combining a wide variety of flexible features and a large range of densities up to 10 million system gates, the Virtex-II family enhances programmable logic design capabilities and is a powerful alternative to mask-programmed gates arrays. As shown in Table 1, the Virtex-II family comprises 11 members, ranging from 40K to 8M system gates.

Packaging

Offerings include ball grid array (BGA) packages with 0.80 mm, 1.00 mm, and 1.27 mm pitches. In addition to traditional wire-bond interconnects, flip-chip interconnect is used in some of the BGA offerings. The use of flip-chip interconnect offers more I/Os than is possible in wire-bond versions of the similar packages. Flip-chip construction offers the combination of high pin count with high thermal capacity.

Wire-bond packages CS, FG, and BG are optionally availabe in Pb-free versions CSG, FGG, and BGG. See Virtex-II Ordering Examples, page 6.

Table 2 shows the maximum number of user I/Os available. The Virtex-II device/package combination table (Table 6 at the end of this section) details the maximum number of I/Os for each device and package using wire-bond or flip-chip technology.

Table 2: **Maximum Number of User I/O Pads**

Device	Wire-Bond	Flip-Chip
XC2V40	88	-
XC2V80	120	-
XC2V250	200	-
XC2V500	264	-
XC2V1000	328	432
XC2V1500	392	528
XC2V2000	-	624
XC2V3000	516	720
XC2V4000	-	912
XC2V6000	-	1,104
XC2V8000	-	1,108

Table 6: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package(1,2)	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Notes:
1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See Virtex-II Ordering Examples for details on how to order.

Virtex-II Ordering Examples

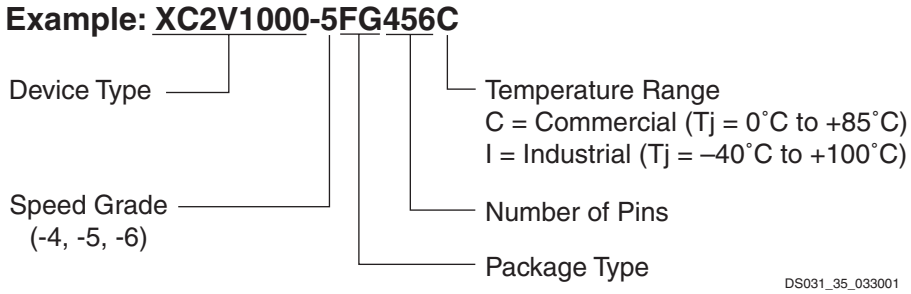

Figure 2: **Virtex-II Ordering Example. Regular Package**

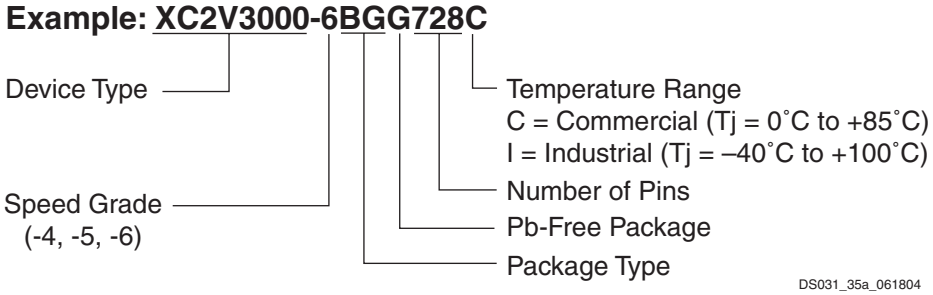

Figure 3: **Virtex-II Ordering Example. Pb-Free Package**

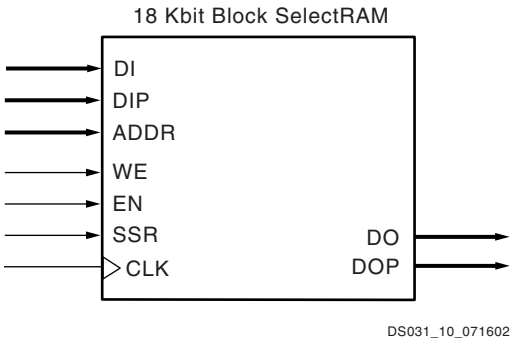

Figure 29: **18 Kbit Block SelectRAM Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 15 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Table 15: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

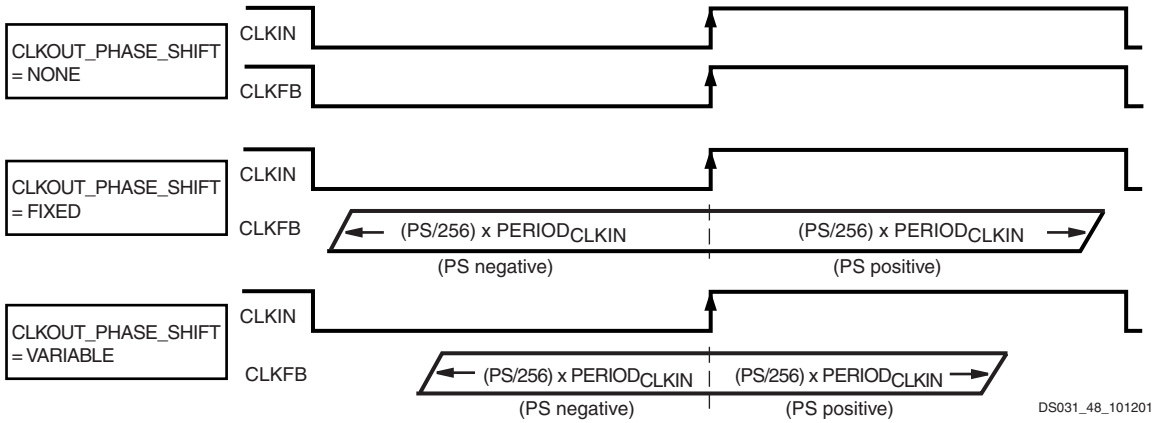

Figure 46: **Fine-Phase Shifting Effects**

Table 22 lists fine-phase shifting control pins, when used in variable mode.

Table 22: **Fine-Phase Shifting Control Pins**

Control Pin	Direction	Function
PSINCDEC	in	Increment or decrement
PSEN	in	Enable ± phase shift
PSCLK	in	Clock for phase shift
PSDONE	out	Active when completed

Two separate components of the phase shift range must be understood:

- PHASE_SHIFT attribute range
- FINE_SHIFT_RANGE DCM timing parameter range

The PHASE_SHIFT attribute is the numerator in the following equation:

Phase Shift (ns) = (PHASE_SHIFT/256) * $PERIOD_{CLKIN}$

The full range of this attribute is always -255 to +255, but its practical range varies with CLKIN frequency, as constrained by the FINE_SHIFT_RANGE component, which represents the total delay achievable by the phase shift delay line. Total delay is a function of the number of delay taps used in the circuit. Across process, voltage, and temperature, this absolute range is guaranteed to be as specified under DCM Timing Parameters in Module 3.

Absolute range (fixed mode) = ± FINE_SHIFT_RANGE

Absolute range (variable mode) = ± FINE_SHIFT_RANGE/2

The reason for the difference between fixed and variable modes is as follows. For variable mode to allow symmetric, dynamic sweeps from -255/256 to +255/256, the DCM sets the "zero phase skew" point as the middle of the delay line, thus dividing the total delay line range in half. In fixed mode, since the PHASE_SHIFT value never changes after configuration, the entire delay line is available for insertion into either the CLKIN or CLKFB path (to create either positive or negative skew).

Taking both of these components into consideration, the following are some usage examples:

- If $PERIOD_{CLKIN}$ = 2 * FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 128, and in variable mode it is limited to ± 64.
- If $PERIOD_{CLKIN}$ = FINE_SHIFT_RANGE, then PHASE_SHIFT in fixed mode is limited to ± 255, and in variable mode it is limited to ± 128.
- If $PERIOD_{CLKIN} \leq 0.5$ * FINE_SHIFT_RANGE, then PHASE_SHIFT is limited to ± 255 in either mode.

Operating Modes

The frequency ranges of DCM input and output clocks depend on the operating mode specified, either low-frequency mode or high-frequency mode, according to Table 23. (For actual values, see Virtex-II Switching Characteristics in Module 3). The CLK2X, CLK2X180, CLK90, and CLK270 outputs are not available in high-frequency mode.

High or low-frequency mode is selected by an attribute.

Table 23: **DCM Frequency Ranges**

Output Clock	Low-Frequency Mode		High-Frequency Mode	
	CLKIN Input	CLK Output	CLKIN Input	CLK Output
CLK0, CLK180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_1X_HF
CLK90, CLK270	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_1X_LF	NA	NA
CLK2X, CLK2X180	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_2X_LF	NA	NA
CLKDV	CLKIN_FREQ_DLL_LF	CLKOUT_FREQ_DV_LF	CLKIN_FREQ_DLL_HF	CLKOUT_FREQ_DV_HF
CLKFX, CLKFX180	CLKIN_FREQ_FX_LF	CLKOUT_FREQ_FX_LF	CLKIN_FREQ_FX_HF	CLKOUT_FREQ_FX_HF

Place-and-route software takes advantage of this regular array to deliver optimum system performance and fast compile times. The segmented routing resources are essential to guarantee IP cores portability and to efficiently handle an incremental design flow that is based on modular implementations. Total design time is reduced due to fewer and shorter design iterations.

Hierarchical Routing Resources

Most Virtex-II signals are routed using the global routing resources, which are located in horizontal and vertical routing channels between each switch matrix.

As shown in Figure 49, Virtex-II has fully buffered programmable interconnections, with a number of resources counted between any two adjacent switch matrix rows or columns. Fanout has minimal impact on the performance of each net.

- The long lines are bidirectional wires that distribute signals across the device. Vertical and horizontal long lines span the full height and width of the device.
- The hex lines route signals to every third or sixth block away in all four directions. Organized in a staggered pattern, hex lines can only be driven from one end. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source).
- The double lines route signals to every first or second block away in all four directions. Organized in a staggered pattern, double lines can be driven only at their endpoints. Double-line signals can be accessed either at the endpoints or at the midpoint (one block from the source).
- The direct connect lines route signals to neighboring blocks: vertically, horizontally, and diagonally.
- The fast connect lines are the internal CLB local interconnections from LUT outputs to LUT inputs.

Dedicated Routing

In addition to the global and local routing resources, dedicated signals are available.

- There are eight global clock nets per quadrant (see Global Clock Multiplexer Buffers).
- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row. (See 3-State Buffers.)
- Two dedicated carry-chain resources per slice column (two per CLB column) propagate carry-chain MUXCY output signals vertically to the adjacent slice. (See CLB/Slice Configurations.)
- One dedicated SOP chain per slice row (two per CLB row) propagate ORCY output logic signals horizontally to the adjacent slice. (See Sum of Products.)
- One dedicated shift-chain per CLB connects the output of LUTs in shift-register mode to the input of the next LUT in shift-register mode (vertically) inside the CLB. (See Shift Registers, page 16.)

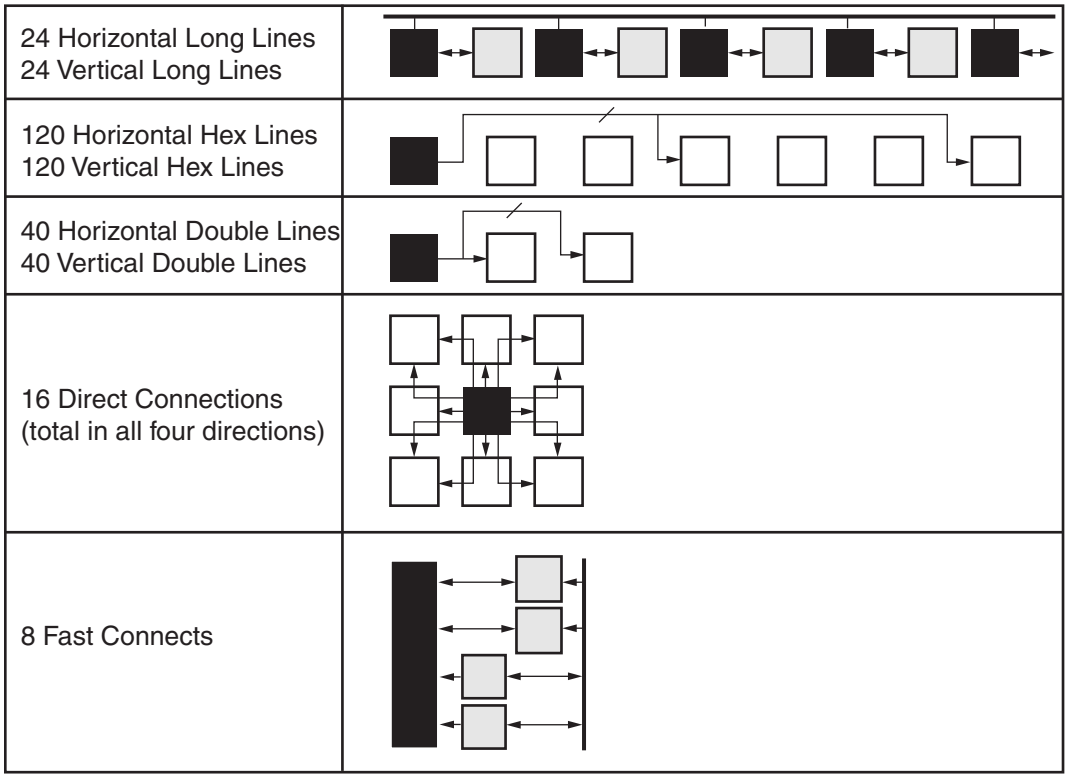

Figure 49: **Hierarchical Routing Resources**

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	50	50	60	ps
		XC2V80	50	50	60	ps
		XC2V250	50	50	60	ps
		XC2V500	50	50	60	ps
		XC2V1000	80	80	90	ps
		XC2V1500	80	80	90	ps
		XC2V2000	100	100	110	ps
		XC2V3000	100	100	110	ps
		XC2V4000	400	400	450	ps
		XC2V6000	500	500	550	ps
		XC2V8000		600	650	ps

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 46: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:

1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Date	Version	Revision
03/01/05 (*cont'd*)	3.4 (*cont'd*)	• Table 15, Table 17, Table 18, and Table 19: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in Xilinx ISE™ software) for all I/O standards. • Table 15: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18, LVDSEXT_25, LVDSEXT_33, BLVDS_25, LVDS_25_DCI, LVDS_33_DCI, LVDSEXT_25_DCI, LVDSEXT_33_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Rearranged I/O standards in a more logical order. • Table 16: Added parameter T_{RPW} (Minimum Pulse Width, SR Input). • Table 17: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Changed "Csl" to "C_{REF}" to agree with Figure 1 and Table 19. Rearranged I/O standards in a more logical order. • Table 18: Added data for the following I/O standards: SSTL18_I, SSTL18_II, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18. Added footnote defining equivalents for DCI standards. • Table 19: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load (C_{REF}) values. Added HSLVDCI callouts to LVDCI parameter rows (same values). • Table 28: Added parameter T_{BCCS}, CLKA to CLKB Setup Time. • Table 31: Added Footnote (1) indicating that F_{CC_SERIAL} should not exceed $F_{CC\_STARTUP}$ if no provision is made to adjust the speed of CCLK. • Table 33: T_{TCKTDO} corrected from a "Min" to a "Max" specification.
11/05/07	3.5	• Updated copyright notice and legal disclaimer.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
NA	CCLK	M13	
NA	PROG_B	B1	
NA	DONE	N12	
NA	M0	N2	
NA	M1	M2	
NA	M2	M3	
NA	TCK	B12	
NA	TDI	C1	
NA	TDO	C11	
NA	TMS	A13	
NA	PWRDWN_B	M12	
NA	HSWAP_EN	A1	
NA	RSVD	A2	
NA	RSVD	B2	
NA	VBATT	A12	
NA	RSVD	B11	
NA	VCCAUX	C2	
NA	VCCAUX	N1	
NA	VCCAUX	N13	
NA	VCCAUX	B13	
NA	VCCINT	H2	
NA	VCCINT	L7	
NA	VCCINT	H13	
NA	VCCINT	C7	
NA	GND	E1	
NA	GND	G2	
NA	GND	J1	
NA	GND	J4	
NA	GND	M5	
NA	GND	L9	
NA	GND	J11	
NA	GND	H10	
NA	GND	F13	
NA	GND	E12	
NA	GND	B9	
NA	GND	C5	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L52P_7	J29		
7	IO_L52N_7	K29		
7	IO_L51P_7/VREF_7	K27		
7	IO_L51N_7	J27		
7	IO_L50P_7	L24		
7	IO_L50N_7	K24		
7	IO_L49P_7	H27		
7	IO_L49N_7	J28		
7	IO_L48P_7	H26		
7	IO_L48N_7	J26		
7	IO_L47P_7	K25		
7	IO_L47N_7	J25		
7	IO_L46P_7	H28		
7	IO_L46N_7	H29		
7	IO_L45P_7/VREF_7	G28		
7	IO_L45N_7	F28		
7	IO_L44P_7	L23		
7	IO_L44N_7	K23		
7	IO_L43P_7	F30		
7	IO_L43N_7	G30		
7	IO_L24P_7	F26		
7	IO_L24N_7	G27		
7	IO_L23P_7	J24		
7	IO_L23N_7	H24		
7	IO_L22P_7	F29		
7	IO_L22N_7	G29		
7	IO_L21P_7/VREF_7	G26		
7	IO_L21N_7	G25		
7	IO_L20P_7	H25		
7	IO_L20N_7	G24		
7	IO_L19P_7	D30		
7	IO_L19N_7	E30		
7	IO_L06P_7	E27		
7	IO_L06N_7	F27		
7	IO_L05P_7	J23		
7	IO_L05N_7	H22		
7	IO_L04P_7	C29		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L22P_1	A5	
1	IO_L21N_1/VREF_1	F10	
1	IO_L21P_1	G9	
1	IO_L20N_1	J12	
1	IO_L20P_1	J11	
1	IO_L19N_1	B4	
1	IO_L19P_1	B5	
1	IO_L06N_1	D6	
1	IO_L06P_1	C6	
1	IO_L05N_1	H11	
1	IO_L05P_1	J10	
1	IO_L04N_1	D8	
1	IO_L04P_1/VREF_1	E7	
1	IO_L03N_1/VRP_1	F9	
1	IO_L03P_1/VRN_1	F8	
1	IO_L02N_1	H10	
1	IO_L02P_1	H9	
1	IO_L01N_1	C2	
1	IO_L01P_1	B3	
2	IO_L01N_2	E2	
2	IO_L01P_2	D2	
2	IO_L02N_2/VRP_2	K11	
2	IO_L02P_2/VRN_2	K10	
2	IO_L03N_2	F5	
2	IO_L03P_2/VREF_2	G5	
2	IO_L04N_2	E3	
2	IO_L04P_2	D3	
2	IO_L05N_2	J9	
2	IO_L05P_2	K9	
2	IO_L06N_2	F4	
2	IO_L06P_2	E4	
2	IO_L19N_2	E1	
2	IO_L19P_2	D1	
2	IO_L20N_2	J8	
2	IO_L20P_2	K8	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L51N_2	L6	
2	IO_L51P_2/VREF_2	M6	
2	IO_L52N_2	M3	
2	IO_L52P_2	L3	
2	IO_L53N_2	L4	
2	IO_L53P_2	K4	
2	IO_L54N_2	N4	
2	IO_L54P_2	M4	
2	IO_L67N_2	M2	
2	IO_L67P_2	L2	
2	IO_L68N_2	N8	
2	IO_L68P_2	P8	
2	IO_L69N_2	N6	
2	IO_L69P_2/VREF_2	P6	
2	IO_L70N_2	P5	
2	IO_L70P_2	N5	
2	IO_L71N_2	P10	
2	IO_L71P_2	R10	
2	IO_L72N_2	P3	
2	IO_L72P_2	N3	
2	IO_L73N_2	M1	
2	IO_L73P_2	L1	
2	IO_L74N_2	P9	
2	IO_L74P_2	R9	
2	IO_L75N_2	P2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	R4	
2	IO_L76P_2	P4	
2	IO_L77N_2	R8	
2	IO_L77P_2	T8	
2	IO_L78N_2	T3	
2	IO_L78P_2	R3	
2	IO_L79N_2	P1	NC
2	IO_L79P_2	N1	NC
2	IO_L80N_2	T11	NC
2	IO_L80P_2	U11	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L03N_7	F30	
7	IO_L02P_7/VRN_7	K25	
7	IO_L02N_7/VRP_7	J25	
7	IO_L01P_7	D33	
7	IO_L01N_7	E33	
0	VCCO_0	M22	
0	VCCO_0	M21	
0	VCCO_0	M20	
0	VCCO_0	M19	
0	VCCO_0	M18	
0	VCCO_0	L23	
0	VCCO_0	L22	
0	VCCO_0	L21	
0	VCCO_0	L20	
0	VCCO_0	E20	
0	VCCO_0	D28	
0	VCCO_0	A25	
0	VCCO_0	A19	
1	VCCO_1	M17	
1	VCCO_1	M16	
1	VCCO_1	M15	
1	VCCO_1	M14	
1	VCCO_1	M13	
1	VCCO_1	L15	
1	VCCO_1	L14	
1	VCCO_1	L13	
1	VCCO_1	L12	
1	VCCO_1	E15	
1	VCCO_1	D7	
1	VCCO_1	A16	
1	VCCO_1	A10	
2	VCCO_2	U12	
2	VCCO_2	T12	
2	VCCO_2	T1	
2	VCCO_2	R12	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
5	VCCO_5	AP19	
5	VCCO_5	AL28	
5	VCCO_5	AK20	
5	VCCO_5	AD23	
5	VCCO_5	AD22	
5	VCCO_5	AD21	
5	VCCO_5	AD20	
5	VCCO_5	AC22	
5	VCCO_5	AC21	
5	VCCO_5	AC20	
5	VCCO_5	AC19	
5	VCCO_5	AC18	
6	VCCO_6	AH31	
6	VCCO_6	AE34	
6	VCCO_6	AC24	
6	VCCO_6	AB24	
6	VCCO_6	AB23	
6	VCCO_6	AA24	
6	VCCO_6	AA23	
6	VCCO_6	Y30	
6	VCCO_6	Y24	
6	VCCO_6	Y23	
6	VCCO_6	W34	
6	VCCO_6	W23	
6	VCCO_6	V23	
7	VCCO_7	U23	
7	VCCO_7	T34	
7	VCCO_7	T23	
7	VCCO_7	R30	
7	VCCO_7	R24	
7	VCCO_7	R23	
7	VCCO_7	P24	
7	VCCO_7	P23	
7	VCCO_7	N24	
7	VCCO_7	N23	
7	VCCO_7	M24	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L52P_0	A30		
0	IO_L53N_0	G26		
0	IO_L53P_0	G25		
0	IO_L54N_0	D26		
0	IO_L54P_0	D27		
0	IO_L55N_0	B27		
0	IO_L55P_0	B28		
0	IO_L56N_0	H25		
0	IO_L56P_0	H24		
0	IO_L57N_0	F25		
0	IO_L57P_0/VREF_0	F26		
0	IO_L58N_0	A27		
0	IO_L58P_0	A28		
0	IO_L59N_0	K24		
0	IO_L59P_0	K23		
0	IO_L60N_0	E24		
0	IO_L60P_0	E25		
0	IO_L67N_0	C26		
0	IO_L67P_0	C27		
0	IO_L68N_0	J24		
0	IO_L68P_0	J23		
0	IO_L69N_0	D24		
0	IO_L69P_0/VREF_0	D25		
0	IO_L70N_0	A25		
0	IO_L70P_0	A26		
0	IO_L71N_0	M22		
0	IO_L71P_0	M21		
0	IO_L72N_0	G23		
0	IO_L72P_0	G24		
0	IO_L73N_0	B25		
0	IO_L73P_0	C25		
0	IO_L74N_0	L22		
0	IO_L74P_0	L21		
0	IO_L75N_0	F23		
0	IO_L75P_0/VREF_0	F24		
0	IO_L76N_0	C23		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L02P_7/VRN_7	M27		
7	IO_L02N_7/VRP_7	L27		
7	IO_L01P_7	D38		
7	IO_L01N_7	E37		
0	VCCO_0	P25		
0	VCCO_0	P24		
0	VCCO_0	P23		
0	VCCO_0	P22		
0	VCCO_0	P21		
0	VCCO_0	N26		
0	VCCO_0	N25		
0	VCCO_0	N24		
0	VCCO_0	N23		
0	VCCO_0	N22		
0	VCCO_0	N21		
0	VCCO_0	L23		
0	VCCO_0	J25		
0	VCCO_0	G27		
0	VCCO_0	E29		
0	VCCO_0	C22		
0	VCCO_0	B26		
1	VCCO_1	P19		
1	VCCO_1	P18		
1	VCCO_1	P17		
1	VCCO_1	P16		
1	VCCO_1	P15		
1	VCCO_1	N19		
1	VCCO_1	N18		
1	VCCO_1	N17		
1	VCCO_1	N16		
1	VCCO_1	N15		
1	VCCO_1	N14		
1	VCCO_1	L17		
1	VCCO_1	J15		
1	VCCO_1	G13		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	VCCO_2	N12	
2	VCCO_2	P3	
2	VCCO_2	P8	
2	VCCO_2	P11	
2	VCCO_2	P12	
2	VCCO_2	R11	
2	VCCO_2	R12	
3	VCCO_3	U11	
3	VCCO_3	U12	
3	VCCO_3	V3	
3	VCCO_3	V8	
3	VCCO_3	V11	
3	VCCO_3	V12	
3	VCCO_3	W11	
3	VCCO_3	W12	
3	VCCO_3	Y11	
3	VCCO_3	AB6	
3	VCCO_3	AE3	
4	VCCO_4	Y13	
4	VCCO_4	Y14	
4	VCCO_4	Y15	
4	VCCO_4	AA12	
4	VCCO_4	AA13	
4	VCCO_4	AA14	
4	VCCO_4	AA15	
4	VCCO_4	AD14	
4	VCCO_4	AF10	
4	VCCO_4	AJ7	
4	VCCO_4	AJ14	
5	VCCO_5	Y17	
5	VCCO_5	Y18	
5	VCCO_5	Y19	
5	VCCO_5	AA17	
5	VCCO_5	AA18	
5	VCCO_5	AA19	
5	VCCO_5	AA20	
5	VCCO_5	AD18	
5	VCCO_5	AF22	