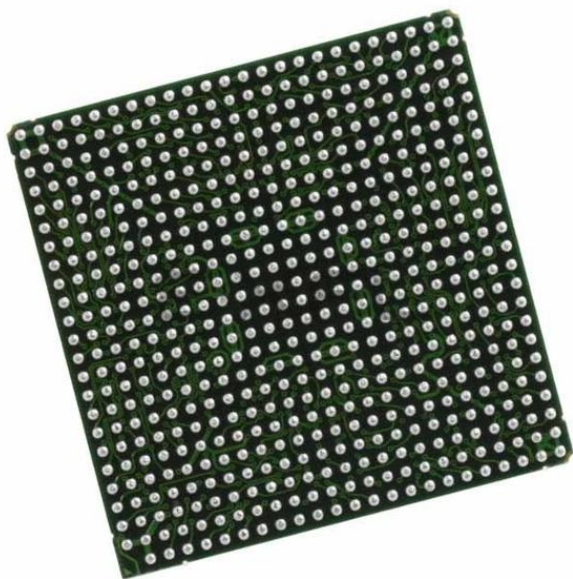




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	328
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-6bgg575c

Table 6: Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)

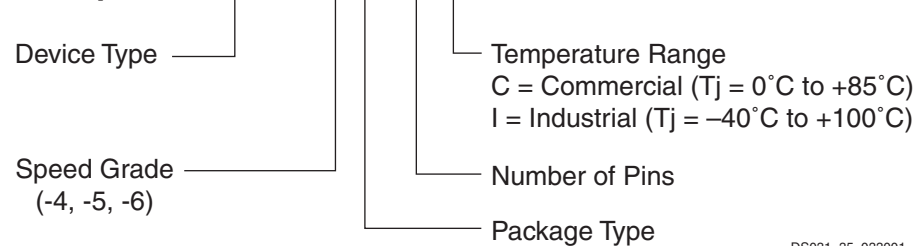
Package ^(1,2)	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Notes:

1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See [Virtex-II Ordering Examples](#) for details on how to order.

Virtex-II Ordering Examples

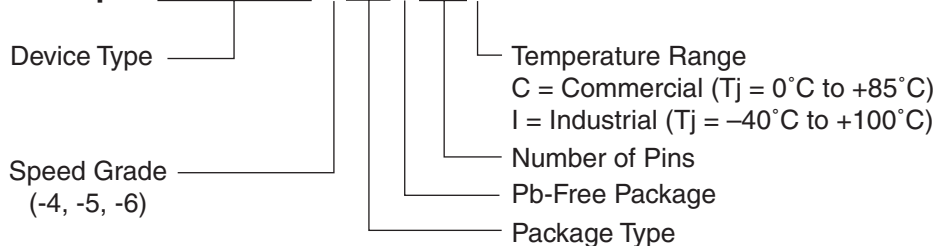
Example: XC2V1000-5FG456C



DS031_35_033001

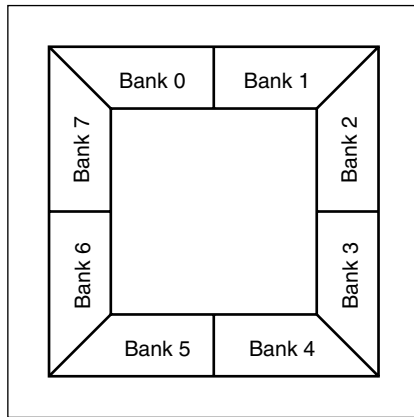
Figure 2: Virtex-II Ordering Example. Regular Package

Example: XC2V3000-6BGG728C



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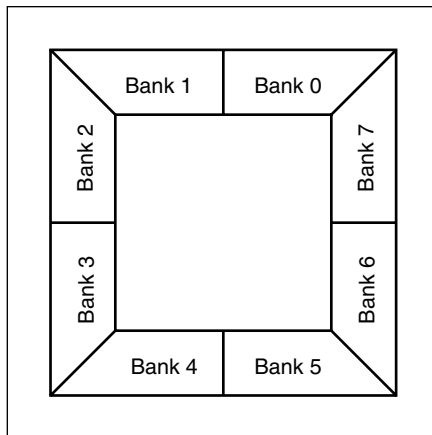
Figure 3: Virtex-II Ordering Example. Pb-Free Package



ug002_c2_014_112900

Figure 7: Virtex-II I/O Banks: Top View for Wire-Bond Packages (CS/CSG, FG/FGG, & BG/BGG)

Some input standards require a user-supplied threshold voltage (V_{REF}), and certain user I/O pins are automatically configured as V_{REF} inputs. Approximately one in six of the I/O pins in the bank assume this role.



ds031_66_112900

Figure 8: Virtex-II I/O Banks: Top View for Flip-Chip Packages (FF & BF)

V_{REF} pins within a bank are interconnected internally, and consequently only one V_{REF} voltage can be used within each bank. However, for correct operation, all V_{REF} pins in the bank must be connected to the external reference voltage source.

The V_{CCO} and the V_{REF} pins for each bank appear in the device pinout tables. Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary.

All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage and not used for I/O. In smaller

devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or, if necessary, they can be connected to V_{CCO} to permit migration to a larger device.

Rules for Combining I/O Standards in the Same Bank

The following rules must be obeyed to combine different input, output, and bi-directional standards in the same bank:

1. **Combining output standards only.** Output standards with the same output V_{CCO} requirement can be combined in the same bank.

Compatible example:

SSTL2_I and LVDS_25_DCI outputs

Incompatible example:

SSTL2_I (output V_{CCO} = 2.5V) and
LVCMOS33 (output V_{CCO} = 3.3V) outputs

2. **Combining input standards only.** Input standards with the same input V_{CCO} and input V_{REF} requirements can be combined in the same bank.

Compatible example:

LVCMOS15 and HSTL_IV inputs

Incompatible example:

LVCMOS15 (input V_{CCO} = 1.5V) and
LVCMOS18 (input V_{CCO} = 1.8V) inputs

Incompatible example:

HSTL_I_DCI_18 (V_{REF} = 0.9V) and
HSTL_IV_DCI_18 (V_{REF} = 1.1V) inputs

3. **Combining input standards and output standards.** Input standards and output standards with the same input V_{CCO} and output V_{CCO} requirement can be combined in the same bank.

Compatible example:

LVDS_25 output and HSTL_I input

Incompatible example:

LVDS_25 output (output V_{CCO} = 2.5V) and
HSTL_I_DCI_18 input (input V_{CCO} = 1.8V)

4. **Combining bi-directional standards with input or output standards.** When combining bi-directional I/O with other standards, make sure the bi-directional standard can meet rules 1 through 3 above.

5. **Additional rules for combining DCI I/O standards.**

- a. No more than one Single Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_IV_DCI input and HSTL_III_DCI input

- b. No more than one Split Termination type (input or output) is allowed in the same bank.

Incompatible example:

HSTL_I_DCI input and HSTL_II_DCI input

The implementation tools will enforce these design rules.

Table 5 summarizes all standards and voltage supplies.

Table 8: SelectI/O-Ultra Differential Buffers With On-Chip Termination

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
LVDS 2.5V	LVDS_25	LVDS_25_DCI
LVDS Extended 2.5V	LVDSEXT_25	LVDSEXT_25_DCI

Figure 11 provides examples illustrating the use of the HSTL_I_DCI, HSTL_II_DCI, HSTL_III_DCI, and HSTL_IV_DCI I/O standards. For a complete list, see the [Virtex-II Platform FPGA User Guide](#).

	HSTL_I	HSTL_II	HSTL_III	HSTL_IV
Conventional				
DCI Transmit Conventional Receive				
Conventional Transmit DCI Receive				
DCI Transmit DCI Receive				
Bidirectional	N/A		N/A	
Reference Resistor	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$	$VRN = VRP = R = Z_0$
Recommended $Z_0^{(1)}$	50 Ω	50 Ω	50 Ω	50 Ω

Note:

1. Z_0 is the recommended PCB trace impedance.

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Figure 11: HSTL DCI Usage Examples

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new

IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: Virtex-II Configuration Mode Pin Settings

Configuration Mode ⁽¹⁾	M2	M1	M0	CCLK Direction	Data Width	Serial D _{OUT} ⁽²⁾
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:

1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: Virtex-II Bitstream Lengths

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V,

and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Date	Version	Revision
03/01/05 (cont'd)	3.4 (cont'd)	Table 15, Table 17, Table 18, and Table 19: Restructured these I/O-related tables to include descriptions, as well as the actual IOSTANDARD attributes (used in Xilinx ISE™ software) for all I/O standards. Table 15: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18, LVDSEXT_25, LVDSEXT_33, BLVDS_25, LVDS_25_DCI, LVDS_33_DCI, LVDSEXT_25_DCI, LVDSEXT_33_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Rearranged I/O standards in a more logical order. Table 16: Added parameter T_{RPW} (Minimum Pulse Width, SR Input). Table 17: Added data for the following I/O standards: SSTL18_I, SSTL18_II, SSTL18_I_DCI, SSTL18_II_DCI, HSLVDCI_15, HSLVDCI_18, HSLVDCI_25, HSLVDCI_33. Changed “Csl” to “C_{REF}” to agree with Figure 1 and Table 19. Rearranged I/O standards in a more logical order. Table 18: Added data for the following I/O standards: SSTL18_I, SSTL18_II, HSTL_I_18, HSTL_II_18, HSTL_III_18, HSTL_IV_18. Added footnote defining equivalents for DCI standards. Table 19: Added Footnotes (2) and (3) to PCI/PCI-X capacitive load (C_{REF}) values. Added HSLVDCI callouts to LVDCI parameter rows (same values). Table 28: Added parameter T_{BCCS}, CLKA to CLKB Setup Time. Table 31: Added Footnote (1) indicating that F_{CC_SERIAL} should not exceed $F_{CC_STARTUP}$ if no provision is made to adjust the speed of CCLK. Table 33: T_{TCKTDO} corrected from a “Min” to a “Max” specification.
11/05/07	3.5	Updated copyright notice and legal disclaimer.

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Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: Virtex-II Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled “IO_LXXY_#”, where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = P/N for the positive and negative sides of the differential pair. # indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled “IO_LXXY_#/ZZZ”, where ZZZ can be one of the following pins: Per Bank - VRP , VRN , or VREF Globally - GCLKX(S/P) , BUSY/DOUT , INIT_B , D0/DIN – D7 , RDWR_B , or CS_B
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	<i>In SelectMAP mode</i>, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. <i>In bit-serial modes</i>, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	<i>In SelectMAP mode</i>, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. <i>In bit-serial modes</i>, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V _{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins⁽¹⁾		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 5: CS144/CSG144 — XC2V40, XC2V80, and XC2V250

Bank	Pin Description	Pin Number	No Connect in the XC2V40
2	IO_L96N_2	G11	
2	IO_L96P_2	G13	
3	IO_L96N_3	G12	
3	IO_L96P_3	H12	
3	IO_L94N_3	H11	
3	IO_L94P_3	J13	
3	IO_L03N_3/VREF_3	J10	
3	IO_L03P_3	K13	
3	IO_L02N_3/VRP_3	K12	
3	IO_L02P_3/VRN_3	K11	
3	IO_L01N_3	K10	
3	IO_L01P_3	L13	
4	IO_L01N_4/BUSY/DOUT ⁽¹⁾	M11	
4	IO_L01P_4/INIT_B	N11	
4	IO_L02N_4/D0/DIN ⁽¹⁾	L10	
4	IO_L02P_4/D1	M10	
4	IO_L03N_4/D2/ALT_VRP_4	N10	
4	IO_L03P_4/D3/ALT_VRN_4	K9	
4	IO_L94N_4/VREF_4	N9	
4	IO_L94P_4	K8	
4	IO_L95N_4/GCLK3S	L8	
4	IO_L95P_4/GCLK2P	M8	
4	IO_L96N_4/GCLK1S	N8	
4	IO_L96P_4/GCLK0P	K7	
5	IO_L96N_5/GCLK7S	N7	
5	IO_L96P_5/GCLK6P	M7	
5	IO_L95N_5/GCLK5S	N6	
5	IO_L95P_5/GCLK4P	M6	
5	IO_L94N_5	L6	
5	IO_L94P_5/VREF_5	K6	
5	IO_L03N_5/D4/ALT_VRP_5	L5	
5	IO_L03P_5/D5/ALT_VRN_5	K5	
5	IO_L02N_5/D6	N4	
5	IO_L02P_5/D7	M4	
5	IO_L01N_5/RDWR_B	L4	
5	IO_L01P_5/CS_B	K4	

Table 8: FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	DONE	AD22		
NA	M0	AD4		
NA	M1	AA5		
NA	M2	AD5		
NA	HSWAP_EN	D5		
NA	TCK	E21		
NA	TDI	F5		
NA	TDO	F22		
NA	TMS	D22		
NA	PWRDWN_B	AD23		
NA	DXN	F7		
NA	DXP	C5		
NA	VBATT	C23		
NA	RSVD	C22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC24		
NA	VCCAUX	AC3		
NA	VCCAUX	P24		
NA	VCCAUX	N3		
NA	VCCAUX	D24		
NA	VCCAUX	D3		
NA	VCCAUX	C14		
NA	VCCINT	W19		
NA	VCCINT	W8		
NA	VCCINT	V18		
NA	VCCINT	V17		
NA	VCCINT	V10		
NA	VCCINT	V9		
NA	VCCINT	U18		
NA	VCCINT	U9		
NA	VCCINT	K18		
NA	VCCINT	K9		
NA	VCCINT	J18		
NA	VCCINT	J17		
NA	VCCINT	J10		
NA	VCCINT	J9		

Table 9: BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
2	IO_L70P_2	N19
2	IO_L72N_2	M22
2	IO_L72P_2	M23
2	IO_L73N_2	M24
2	IO_L73P_2	N24
2	IO_L75N_2	M26
2	IO_L75P_2/VREF_2	M27
2	IO_L76N_2	N20
2	IO_L76P_2	N21
2	IO_L78N_2	N22
2	IO_L78P_2	N23
2	IO_L91N_2	N25
2	IO_L91P_2	P25
2	IO_L93N_2	N26
2	IO_L93P_2/VREF_2	N27
2	IO_L94N_2	P20
2	IO_L94P_2	P21
2	IO_L96N_2	P22
2	IO_L96P_2	P23
3	IO_L96N_3	R27
3	IO_L96P_3	R26
3	IO_L94N_3	R25
3	IO_L94P_3	R24
3	IO_L93N_3/VREF_3	R23
3	IO_L93P_3	T23
3	IO_L91N_3	R22
3	IO_L91P_3	R21
3	IO_L78N_3	R20
3	IO_L78P_3	R19
3	IO_L76N_3	T27
3	IO_L76P_3	T26
3	IO_L75N_3/VREF_3	T24
3	IO_L75P_3	U24
3	IO_L73N_3	T22
3	IO_L73P_3	U22

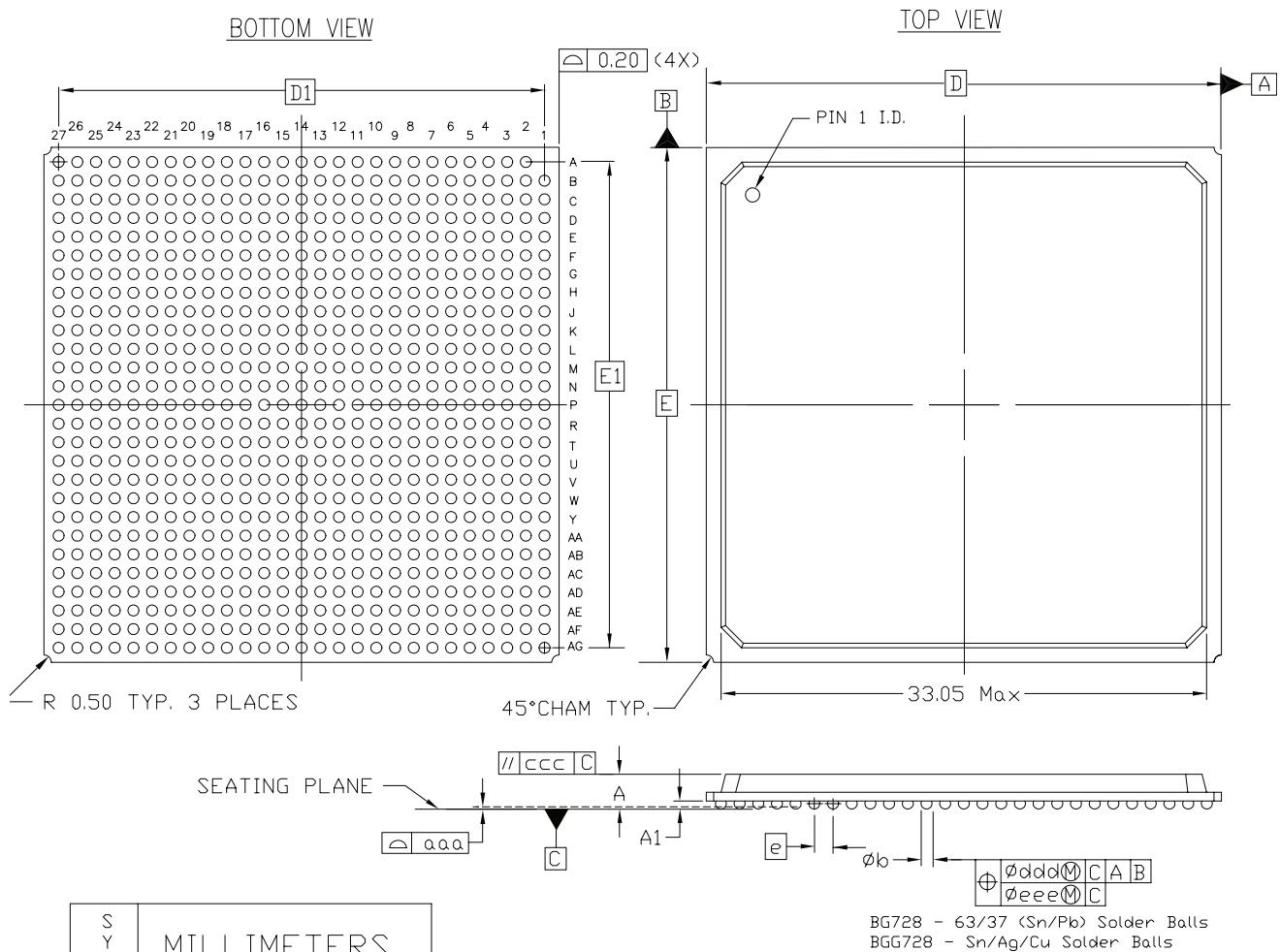
Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
6	IO_L52N_6	V3
6	IO_L54P_6	V2
6	IO_L54N_6	V1
6	IO_L67P_6	U8
6	IO_L67N_6	T8
6	IO_L69P_6	U6
6	IO_L69N_6/VREF_6	U7
6	IO_L70P_6	U4
6	IO_L70N_6	U3
6	IO_L72P_6	U2
6	IO_L72N_6	U1
6	IO_L73P_6	T9
6	IO_L73N_6	R9
6	IO_L75P_6	T5
6	IO_L75N_6/VREF_6	T6
6	IO_L76P_6	T4
6	IO_L76N_6	R4
6	IO_L78P_6	T2
6	IO_L78N_6	T1
6	IO_L91P_6	R7
6	IO_L91N_6	R8
6	IO_L93P_6	R5
6	IO_L93N_6/VREF_6	R6
6	IO_L94P_6	R3
6	IO_L94N_6	P3
6	IO_L96P_6	R2
6	IO_L96N_6	R1
7	IO_L96P_7	P5
7	IO_L96N_7	P6
7	IO_L94P_7	P7
7	IO_L94N_7	P8
7	IO_L93P_7/VREF_7	N1
7	IO_L93N_7	N2
7	IO_L91P_7	N3
7	IO_L91N_7	N4

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
NA	GND	T12
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	P27
NA	GND	P24
NA	GND	P19
NA	GND	P16
NA	GND	P15
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P9
NA	GND	P4
NA	GND	P1
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	L23
NA	GND	L5
NA	GND	J14
NA	GND	H26
NA	GND	H20
NA	GND	H8
NA	GND	H2
NA	GND	G21
NA	GND	G7

BG728/BGG728 Standard BGA Package Specifications (1.27mm pitch)



NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
- SYMBOL 'M' IS THE BALL MATRIX SIZE.
- CONFORMS TO JEDEC MS-034-BAR-1
- NO SOLDER BALL AND LAND ON A1.

728-BALL MOLDED BGA (BG728/BGG728)

Figure 6: BG728/BGG728 Standard BGA Package Specifications

Table 11: FF896 BGA — XC2V1000, XC2V1500, and XC2V2000

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L51N_2	L6	
2	IO_L51P_2/VREF_2	M6	
2	IO_L52N_2	M3	
2	IO_L52P_2	L3	
2	IO_L53N_2	L4	
2	IO_L53P_2	K4	
2	IO_L54N_2	N4	
2	IO_L54P_2	M4	
2	IO_L67N_2	M2	
2	IO_L67P_2	L2	
2	IO_L68N_2	N8	
2	IO_L68P_2	P8	
2	IO_L69N_2	N6	
2	IO_L69P_2/VREF_2	P6	
2	IO_L70N_2	P5	
2	IO_L70P_2	N5	
2	IO_L71N_2	P10	
2	IO_L71P_2	R10	
2	IO_L72N_2	P3	
2	IO_L72P_2	N3	
2	IO_L73N_2	M1	
2	IO_L73P_2	L1	
2	IO_L74N_2	P9	
2	IO_L74P_2	R9	
2	IO_L75N_2	P2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	R4	
2	IO_L76P_2	P4	
2	IO_L77N_2	R8	
2	IO_L77P_2	T8	
2	IO_L78N_2	T3	
2	IO_L78P_2	R3	
2	IO_L79N_2	P1	NC
2	IO_L79P_2	N1	NC
2	IO_L80N_2	T11	NC
2	IO_L80P_2	U11	NC

Table 12: FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	AB17	
NA	VCCINT	AB16	
NA	VCCINT	AB15	
NA	VCCINT	AB14	
NA	VCCINT	AB13	
NA	VCCINT	AA22	
NA	VCCINT	AA13	
NA	VCCINT	Y22	
NA	VCCINT	Y13	
NA	VCCINT	W22	
NA	VCCINT	W13	
NA	VCCINT	V22	
NA	VCCINT	V13	
NA	VCCINT	U22	
NA	VCCINT	U13	
NA	VCCINT	T22	
NA	VCCINT	T13	
NA	VCCINT	R22	
NA	VCCINT	R13	
NA	VCCINT	P22	
NA	VCCINT	P13	
NA	VCCINT	N22	
NA	VCCINT	N21	
NA	VCCINT	N20	
NA	VCCINT	N19	
NA	VCCINT	N18	
NA	VCCINT	N17	
NA	VCCINT	N16	
NA	VCCINT	N15	
NA	VCCINT	N14	
NA	VCCINT	N13	
NA	VCCINT	M23	
NA	VCCINT	M12	
NA	VCCINT	L24	
NA	VCCINT	L11	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L09N_1/VREF_1	G9	NC	
1	IO_L09P_1	G10	NC	
1	IO_L08N_1	K13	NC	
1	IO_L08P_1	K12	NC	
1	IO_L07N_1	A4	NC	
1	IO_L07P_1	A5	NC	
1	IO_L06N_1	F8		
1	IO_L06P_1	E8		
1	IO_L05N_1	J11		
1	IO_L05P_1	K11		
1	IO_L04N_1	C5		
1	IO_L04P_1/VREF_1	C6		
1	IO_L03N_1/VRP_1	D6		
1	IO_L03P_1/VRN_1	D7		
1	IO_L02N_1	H10		
1	IO_L02P_1	J10		
1	IO_L01N_1	C4		
1	IO_L01P_1	B4		
2	IO_L01N_2	E3		
2	IO_L01P_2	D2		
2	IO_L02N_2/VRP_2	L13		
2	IO_L02P_2/VRN_2	M13		
2	IO_L03N_2	F4		
2	IO_L03P_2/VREF_2	E4		
2	IO_L04N_2	E1		
2	IO_L04P_2	D1		
2	IO_L05N_2	L12		
2	IO_L05P_2	M11		
2	IO_L06N_2	G6		
2	IO_L06P_2	F5		
2	IO_L07N_2	F2	NC	
2	IO_L07P_2	E2	NC	
2	IO_L08N_2	M12	NC	
2	IO_L08P_2	N12	NC	
2	IO_L09N_2	H6	NC	

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L82N_3	AA4		
3	IO_L82P_3	AB4		
3	IO_L81N_3/VREF_3	AB11		
3	IO_L81P_3	AA11		
3	IO_L80N_3	AC1		
3	IO_L80P_3	AD1		
3	IO_L79N_3	AA7		
3	IO_L79P_3	AB7		
3	IO_L78N_3	AB12		
3	IO_L78P_3	AA12		
3	IO_L77N_3	AC2		
3	IO_L77P_3	AC3		
3	IO_L76N_3	AB5		
3	IO_L76P_3	AC5		
3	IO_L75N_3/VREF_3	AD9		
3	IO_L75P_3	AC9		
3	IO_L74N_3	AD2		
3	IO_L74P_3	AE2		
3	IO_L73N_3	AB6		
3	IO_L73P_3	AC6		
3	IO_L72N_3	AD10		
3	IO_L72P_3	AC10		
3	IO_L71N_3	AD3		
3	IO_L71P_3	AE3		
3	IO_L70N_3	AC7		
3	IO_L70P_3	AD7		
3	IO_L69N_3/VREF_3	AE8		
3	IO_L69P_3	AD8		
3	IO_L68N_3	AE1		
3	IO_L68P_3	AF1		
3	IO_L67N_3	AD4		
3	IO_L67P_3	AE4		
3	IO_L60N_3	AD12		
3	IO_L60P_3	AC12		
3	IO_L59N_3	AF3		
3	IO_L59P_3	AG3		

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	VCCO_3	AA13		
4	VCCO_4	AV14		
4	VCCO_4	AU18		
4	VCCO_4	AR11		
4	VCCO_4	AN13		
4	VCCO_4	AL15		
4	VCCO_4	AJ17		
4	VCCO_4	AG19		
4	VCCO_4	AG18		
4	VCCO_4	AG17		
4	VCCO_4	AG16		
4	VCCO_4	AG15		
4	VCCO_4	AG14		
4	VCCO_4	AF19		
4	VCCO_4	AF18		
4	VCCO_4	AF17		
4	VCCO_4	AF16		
4	VCCO_4	AF15		
5	VCCO_5	AV26		
5	VCCO_5	AU22		
5	VCCO_5	AR29		
5	VCCO_5	AN27		
5	VCCO_5	AL25		
5	VCCO_5	AJ23		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AG24		
5	VCCO_5	AG23		
5	VCCO_5	AG22		
5	VCCO_5	AG21		
5	VCCO_5	AF25		
5	VCCO_5	AF24		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
6	VCCO_6	AJ35		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	
7	IO_L06P_7	F28	