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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	172
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-6fgg256c

Date	Version	Revision
07/16/02	2.0	• Updated compatible input standards listed in Table 6.
09/26/02	2.1	• Changed number of resources available to the XC2V40 device in Table 13. • Clarified Power On Reset information under Configuration Sequence.
12/06/02	2.1.1	• Cosmetic edits.
05/07/03	2.1.2	• Added qualification note to Figure 13, page 11. • Corrected sentence in section Input/Output Individual Options, page 4, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Corrected typographical errors in Table 3 for names of HSTL_[x]_DCI_18 standards.
06/19/03	2.2	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 5, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Added section Rules for Combining I/O Standards in the Same Bank, page 6.
08/01/03	3.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
10/14/03	3.1	• Added section Local Clocking, page 29. • Table 1, page 1: - Added SSTL18_I and SSTL18_II. - Corrected names of 1.8V HSTL_I-IV standards to “HSTL_I-IV_18”. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. - Changed “N/A” to “N/R” (no requirement). • Table 2, page 2: - Changed “N/A” to “N/R” (no requirement). • Table 3, page 2: - Added SSTL18_I_DCI, SSTL18_II_DCI, LVDS_33_DCI, LVDSEXT_33_DCI, LVDS_25_DCI, and LVDSEXT_25_DCI. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. • Sections Slave-Serial Mode and Master-Serial Mode, page 36: Changed "rising" to "falling" edge with respect to DOUT. • Added verbiage to section Bitstream Encryption, page 38: “For devices that support this feature, please contact your sales representative for specific ordering part number.”
03/29/04	3.2	• Table 2, page 2, and Table 5, page 7: Removed LVDS_33_DCI and LVDSEXT_33_DCI from tables. • Table 26, page 37: Updated bitstream lengths. • Section BUFGMUX, page 29: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 44 and associated text from CLK0 and CLK1 to I0 and I1. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1, page 1: Added example to Footnote (1) regarding V_{CCO} rules for GTL and GTLP. • Added reference to Pb-free package types in Figure 7, page 6.
03/01/05	3.4	• Reassigned heading hierarchies for better agreement with content. • Table 2: Corrected V_{OD} output voltages. • Table 26: Updated bitstream lengths.
11/05/07	3.5	• Updated copyright statement and legal disclaimer. • Boundary-Scan (JTAG, IEEE 1532) Mode, page 37: Updated IEEE 1149.1 compliance statement.

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8

Table 15: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{ILVDCI\_DV2\_33}$	0.00	0.00	0.00	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.11	0.11	0.12	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.42	0.43	0.49	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.98	1.00	1.14	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.42	0.42	0.48	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.52	0.53	0.60	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.42	0.42	0.48	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.42	0.42	0.48	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.42	0.42	0.48	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{ISSTL3\_I\_DCI}$	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{ISSTL3\_II\_DCI}$	0.35	0.35	0.40	ns
LVDS (Low-Voltage Differential Signaling), 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.60	0.60	0.69	ns
LVDS, 3.3V, with DCI	LVDS_33_DCI	$T_{ILVDS\_33\_DCI}$	0.60	0.60	0.69	ns
LVDSEXT (LVDS Extended Mode), 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.58	0.59	0.79	ns
LVDSEXT, 3.3V, with DCI	LVDSEXT_33_DCI	$T_{ILVDSEXT\_33\_DCI}$	0.56	0.56	0.65	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see Table 18.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

Table 18: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – (0.2 x V_{CCO})	V_{REF} + (0.2 x V_{CCO})	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS, 3.3V	LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT, 3.3V	LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

Miscellaneous Timing Parameters

Table 42: **Miscellaneous Timing Parameters**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade			Units
			-6	-5	-4	
Time Required to Achieve LOCK						
Using DLL outputs(1)	LOCK_DLL					
	LOCK_DLL_60	> 60MHz	20.0	20.0	20.0	µs
	LOCK_DLL_50_60	50 - 60 MHz	25.0	25.0	25.0	µs
	LOCK_DLL_40_50	40 - 50 MHz	50.0	50.0	50.0	µs
	LOCK_DLL_30_40	30 - 40 MHz	90.0	90.0	90.0	µs
	LOCK_DLL_24_30	24 - 30 MHz	120.0	120.0	120.0	µs
Using CLKFX outputs	LOCK_FX_MIN		10.0	10.0	10.0	ms
	LOCK_FX_MAX		10.0	10.0	10.0	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT		50.0	50.0	50.0	µs
Fine-Phase Shifting						
Absolute shifting range	FINE_SHIFT_RANGE		10.0	10.0	10.0	ns
Delay Lines						
Tap delay resolution	DCM_TAP_MIN		30.0	30.0	30.0	ps
	DCM_TAP_MAX		60.0	60.0	60.0	ps

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. Specification also applies to PSCLK.

Frequency Synthesis

Table 43: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	32
CLKFX_DIVIDE	1	32

Parameter Cross Reference

Table 44: **Parameter Cross Reference**

Libraries Guide	Data Sheet
DLL_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_{1X|2X|DV}_LF
DFS_CLKOUT_{MIN|MAX}_LF	CLKOUT_FREQ_FX_LF
DLL_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_DLL_LF
DFS_CLKIN_{MIN|MAX}_LF	CLKIN_FREQ_FX_LF
DLL_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_{1X|DV}_HF
DFS_CLKOUT_{MIN|MAX}_HF	CLKOUT_FREQ_FX_HF
DLL_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_DLL_HF
DFS_CLKIN_{MIN|MAX}_HF	CLKIN_FREQ_FX_HF

Table 47: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	500	500	550	ps
		XC2V80	500	500	550	ps
		XC2V250	500	500	550	ps
		XC2V500	500	500	550	ps
		XC2V1000	500	500	550	ps
		XC2V1500	500	500	550	ps
		XC2V2000	500	500	550	ps
		XC2V3000	500	500	550	ps
		XC2V4000	500	500	550	ps
		XC2V6000	500	500	550	ps
		XC2V8000		500	550	ps

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 48: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V80	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V250	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V2000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V3000	0.2/0.5	0.2/0.5	0.2/0.6	ns
		XC2V4000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V6000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V8000		0.2/0.6	0.2/0.7	ns

Notes:
1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
6	IO_L46P_6	R2		
6	IO_L46N_6	R1		
6	IO_L48P_6	P6		
6	IO_L48N_6	P5		
6	IO_L49P_6	P4	NC	
6	IO_L49N_6	P3	NC	
6	IO_L51P_6	P2	NC	
6	IO_L51N_6/VREF_6	P1	NC	
6	IO_L52P_6	N6	NC	
6	IO_L52N_6	N5	NC	
6	IO_L54P_6	N4	NC	
6	IO_L54N_6	N3	NC	
6	IO_L91P_6	N2		
6	IO_L91N_6	N1		
6	IO_L93P_6	M6		
6	IO_L93N_6/VREF_6	M5		
6	IO_L94P_6	M4		
6	IO_L94N_6	M3		
6	IO_L96P_6	M2		
6	IO_L96N_6	M1		
7	IO_L96P_7	L2		
7	IO_L96N_7	L3		
7	IO_L94P_7	L4		
7	IO_L94N_7	L5		
7	IO_L93P_7/VREF_7	K1		
7	IO_L93N_7	K2		
7	IO_L91P_7	K3		
7	IO_L91N_7	K4		
7	IO_L54P_7	L6	NC	
7	IO_L54N_7	K6	NC	
7	IO_L52P_7	K5	NC	
7	IO_L52N_7	J5	NC	
7	IO_L51P_7/VREF_7	J1	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

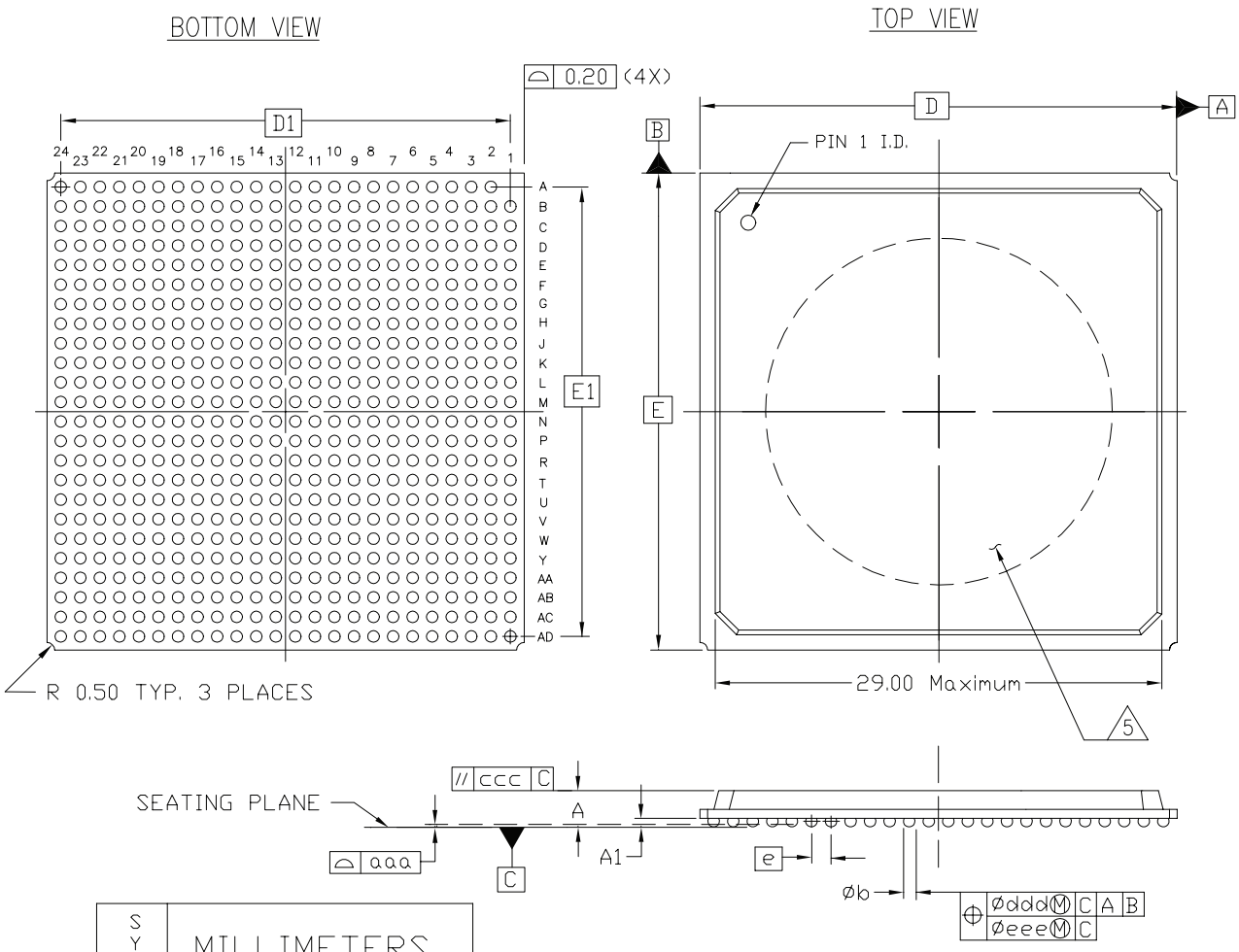
Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	IO_L46P_7	H2		
7	IO_L46N_7	G2		
7	IO_L45P_7/VREF_7	H3		
7	IO_L45N_7	H4		
7	IO_L43P_7	G3		
7	IO_L43N_7	G4		
7	IO_L24P_7	H5		
7	IO_L24N_7	H6		
7	IO_L22P_7	J6		
7	IO_L22N_7	J7		
7	IO_L21P_7/VREF_7	K7		
7	IO_L21N_7	K8		
7	IO_L19P_7	E1		
7	IO_L19N_7	E2		
7	IO_L06P_7	D2		
7	IO_L06N_7	D3		
7	IO_L04P_7	E3		
7	IO_L04N_7	E4		
7	IO_L03P_7/VREF_7	F4		
7	IO_L03N_7	F5		
7	IO_L02P_7/VRN_7	G5		
7	IO_L02N_7/VRP_7	G6		
7	IO_L01P_7	H7		
7	IO_L01N_7	J8		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	J10		
0	VCCO_0	F11		
0	VCCO_0	C6		
0	VCCO_0	B11		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	J13		
1	VCCO_1	F14		
1	VCCO_1	C19		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	D15		
NA	GND	D10		
NA	GND	D4		
NA	GND	C22		
NA	GND	C3		
NA	GND	B24		
NA	GND	B23		
NA	GND	B2		
NA	GND	B1		
NA	GND	A24		
NA	GND	A23		
NA	GND	A18		
NA	GND	A7		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOUT(1)	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN(1)	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
6	VCCO_6	V9
6	VCCO_6	U10
6	VCCO_6	U9
6	VCCO_6	T10
6	VCCO_6	T7
6	VCCO_6	T3
6	VCCO_6	R10
7	VCCO_7	M10
7	VCCO_7	M7
7	VCCO_7	M3
7	VCCO_7	L10
7	VCCO_7	L9
7	VCCO_7	K9
7	VCCO_7	G4
7	VCCO_7	N10
NA	CCLK	AA22
NA	PROG_B	C4
NA	DONE	AC22
NA	M0	AC6
NA	M1	Y7
NA	M2	AE4
NA	HSWAP_EN	D5
NA	TCK	G20
NA	TDI	H7
NA	TDO	G22
NA	TMS	F21
NA	PWRDWN_B	AE24
NA	DXN	G8
NA	DXP	F7
NA	VBATT	D23
NA	RSVD	C24
NA	VCCAUX	AF14
NA	VCCAUX	AE26
NA	VCCAUX	AE2

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	AC1		
NA	GND	AA28		
NA	GND	AA3		
NA	GND	W26		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	W15		
NA	GND	W14		
NA	GND	W13		
NA	GND	W12		
NA	GND	W5		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	V15		
NA	GND	V14		
NA	GND	V13		
NA	GND	V12		
NA	GND	U24		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U15		
NA	GND	U14		
NA	GND	U13		
NA	GND	U12		
NA	GND	U7		
NA	GND	T19		
NA	GND	T18		
NA	GND	T17		
NA	GND	T16		
NA	GND	T15		
NA	GND	T14		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L57P_2/VREF_2	P7		
2	IO_L58N_2	R3		
2	IO_L58P_2	P3		
2	IO_L59N_2	T10		
2	IO_L59P_2	U10		
2	IO_L60N_2	P4		
2	IO_L60P_2	N4		
2	IO_L67N_2	T6		
2	IO_L67P_2	R6		
2	IO_L68N_2	T9		
2	IO_L68P_2	U9		
2	IO_L69N_2	T5		
2	IO_L69P_2/VREF_2	R5		
2	IO_L70N_2	R1		
2	IO_L70P_2	P1		
2	IO_L71N_2	V12		
2	IO_L71P_2	W12		
2	IO_L72N_2	T4		
2	IO_L72P_2	R4		
2	IO_L73N_2	T2		
2	IO_L73P_2	R2		
2	IO_L74N_2	V11		
2	IO_L74P_2	W11		
2	IO_L75N_2	U7		
2	IO_L75P_2/VREF_2	T7		
2	IO_L76N_2	U3		
2	IO_L76P_2	T3		
2	IO_L77N_2	V10		
2	IO_L77P_2	W10		
2	IO_L78N_2	V6		
2	IO_L78P_2	U6		
2	IO_L79N_2	U1		
2	IO_L79P_2	T1		
2	IO_L80N_2	V9		
2	IO_L80P_2	W9		
2	IO_L81N_2	V5		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L50P_7	P32		
7	IO_L50N_7	N32		
7	IO_L49P_7	L37		
7	IO_L49N_7	M37		
7	IO_L48P_7	N34		
7	IO_L48N_7	P34		
7	IO_L47P_7	P31		
7	IO_L47N_7	N31		
7	IO_L46P_7	M35		
7	IO_L46N_7	N35		
7	IO_L45P_7/VREF_7	L36		
7	IO_L45N_7	M36		
7	IO_L44P_7	R28		
7	IO_L44N_7	P28		
7	IO_L43P_7	K39		
7	IO_L43N_7	L39		
7	IO_L36P_7	L34	NC	
7	IO_L36N_7	M34	NC	
7	IO_L35P_7	P29	NC	
7	IO_L35N_7	N29	NC	
7	IO_L34P_7	J38	NC	
7	IO_L34N_7	K38	NC	
7	IO_L33P_7/VREF_7	L33	NC	
7	IO_L33N_7	M33	NC	
7	IO_L32P_7	M32	NC	
7	IO_L32N_7	L32	NC	
7	IO_L31P_7	H39	NC	
7	IO_L31N_7	J39	NC	
7	IO_L30P_7	J36		
7	IO_L30N_7	K36		
7	IO_L29P_7	N30		
7	IO_L29N_7	M30		
7	IO_L28P_7	J37		
7	IO_L28N_7	K37		
7	IO_L27P_7/VREF_7	J35		
7	IO_L27N_7	K35		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L23N_2	E2	
2	IO_L23P_2	F2	
2	IO_L24N_2	H4	
2	IO_L24P_2	J4	
2	IO_L25N_2	K8	NC
2	IO_L25P_2	L8	NC
2	IO_L27N_2	J7	NC
2	IO_L27P_2/VREF_2	K7	NC
2	IO_L43N_2	F1	
2	IO_L43P_2	G1	
2	IO_L44N_2	L9	
2	IO_L44P_2	M9	
2	IO_L45N_2	G2	
2	IO_L45P_2/VREF_2	J2	
2	IO_L46N_2	H3	
2	IO_L46P_2	J3	
2	IO_L47N_2	J6	
2	IO_L47P_2	L6	
2	IO_L48N_2	J5	
2	IO_L48P_2	K5	
2	IO_L49N_2	H1	
2	IO_L49P_2	J1	
2	IO_L50N_2	N10	
2	IO_L50P_2	P10	
2	IO_L51N_2	L7	
2	IO_L51P_2/VREF_2	M7	
2	IO_L52N_2	K3	
2	IO_L52P_2	L3	
2	IO_L53N_2	M8	
2	IO_L53P_2	N8	
2	IO_L54N_2	L5	
2	IO_L54P_2	M5	
2	IO_L67N_2	K2	
2	IO_L67P_2	L2	
2	IO_L68N_2	M6	
2	IO_L68P_2	N6	
2	IO_L69N_2	L4	
2	IO_L69P_2/VREF_2	M4	