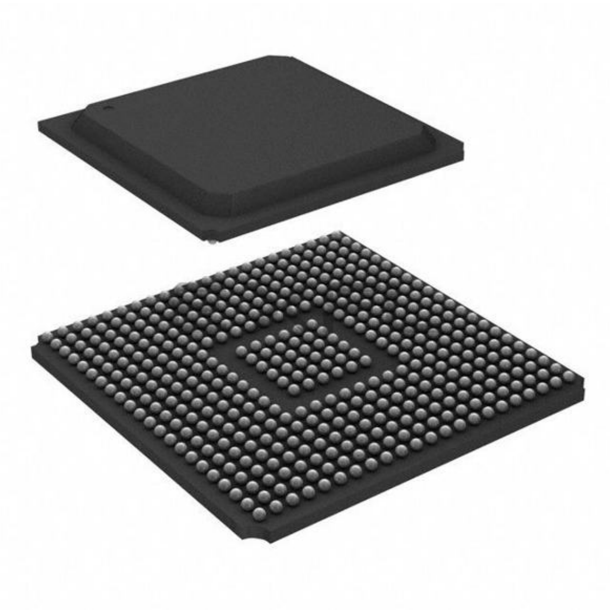

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1280
Number of Logic Elements/Cells	-
Total RAM Bits	737280
Number of I/O	324
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1000-6fgg456c

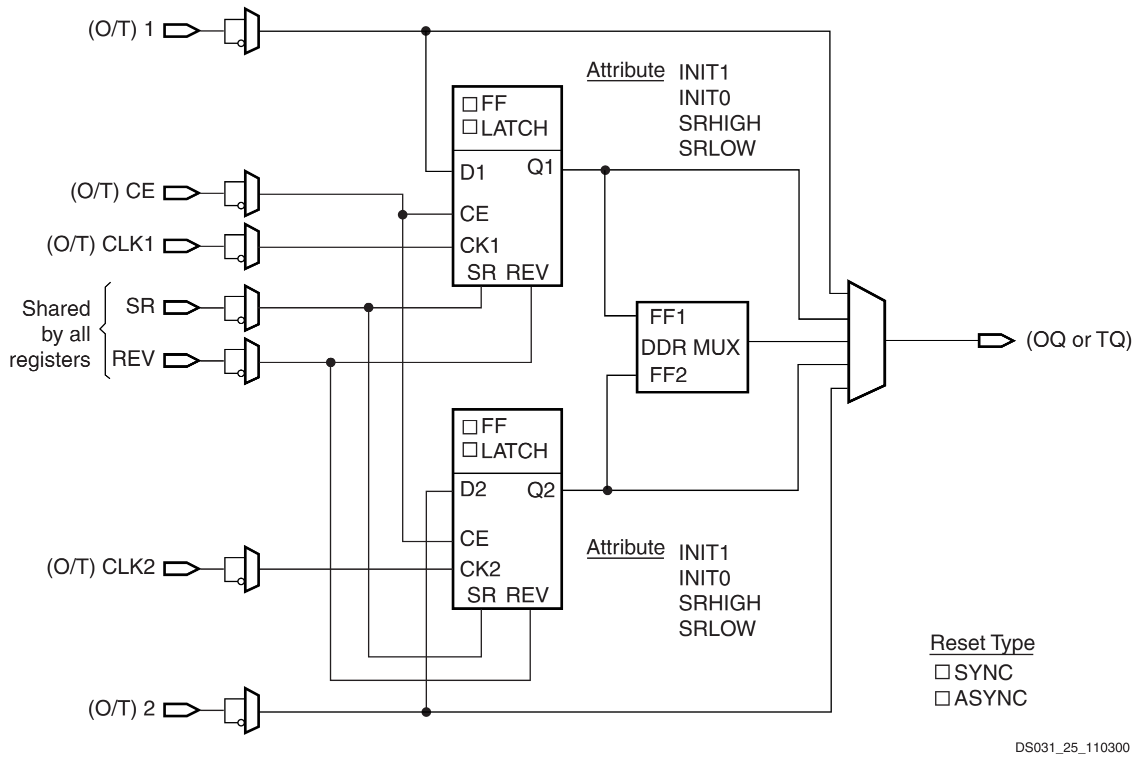

Figure 4: **Register / Latch Configuration in an IOB Block**

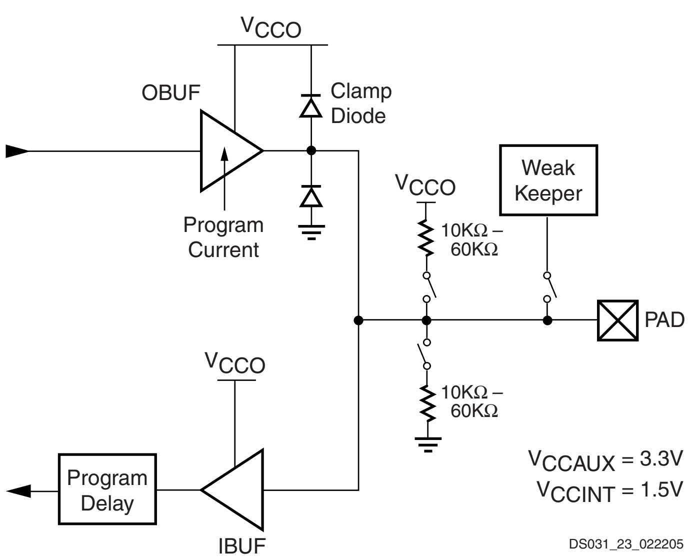

Figure 5: **LVTTL, LVCMOS or PCI SelectI/O-Ultra Standards**

Input/Output Individual Options

Each device pad has optional pull-up and pull-down in all SelectI/O-Ultra configurations. Each device pad has optional weak-keeper in LVTTL, LVCMOS, and PCI SelectI/O-Ultra configurations, as illustrated in Figure 5. Values of the optional pull-up and pull-down resistors are in the range 10 - 60 KΩ, which is the specification for V_{CCO} when operating at 3.3V (from 3.0 to 3.6V only). The clamp diode is always present, even when power is not.

The optional weak-keeper circuit is connected to each user I/O pad. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low. If the pin is connected to a multiple-source signal, the weak-keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter. An enabled pull-up or pull-down overrides the weak-keeper circuit.

LVTTL sinks and sources current up to 24 mA. The current is programmable for LVTTL and LVCMOS SelectI/O-Ultra standards (see Table 4). Drive-strength and slew-rate controls for each output driver, minimize bus transients. For LVDCI and LVDCI_DV2 standards, drive strength and slew-rate controls are not available.

Configurable Logic Blocks (CLBs)

The Virtex-II configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 14. A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

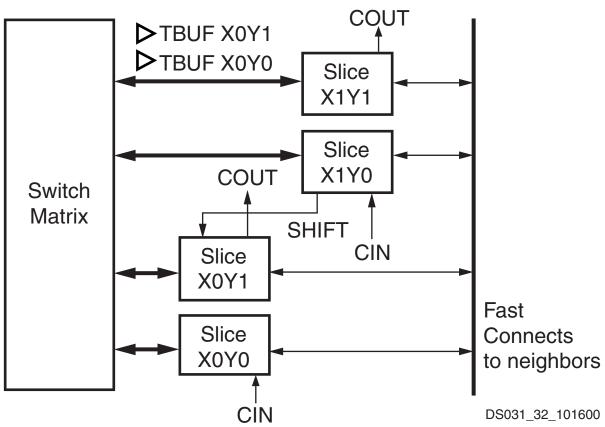

Figure 14: **Virtex-II CLB Element**

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 15, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM memory, or a 16-bit variable-tap shift register element.

The output from the function generator in each slice drives both the slice output and the D input of the storage element. Figure 16 shows a more detailed view of a single slice.

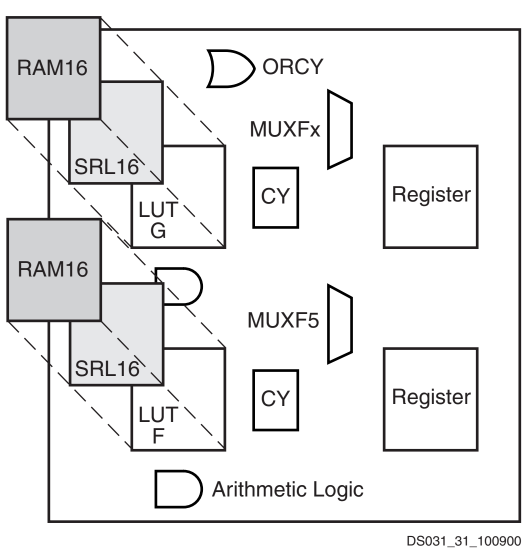

Figure 15: **Virtex-II Slice Configuration**

Configurations

Look-Up Table

Virtex-II function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in Figure 16).

In addition to the basic LUTs, the Virtex-II slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX are either MUXF6, MUXF7 or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexers to map any functions of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by the X or Y output via the DX or DY input, or by the slice inputs bypassing the function generators via the BX or BY input. The clock enable signal (CE) is active High by default. If left unconnected, the clock enable for that storage element defaults to the active state.

In addition to clock (CK) and clock enable (CE) signals, each slice has set and reset signals (SR and BY slice inputs). SR forces the storage element into the state specified by the attribute SRHIGH or SRLOW. SRHIGH forces a logic “1” when SR is asserted. SRLOW forces a logic “0”. When SR is used, a second input (BY) forces the storage element into the opposite state. The reset condition is predominant over the set condition. (See Figure 17.)

The initial state after configuration or global initial state is defined by a separate INIT0 and INIT1 attribute. By default, setting the SRLOW attribute sets INIT0, and setting the SRHIGH attribute sets INIT1. For each slice, set and reset can be set to be synchronous or asynchronous. Virtex-II devices also have the ability to set INIT0 and INIT1 independent of SRHIGH and SRLOW.

The control signals clock (CLK), clock enable (CE) and set/reset (SR) are common to both storage elements in one slice. All of the control signals have independent polarity. Any inverter placed on a control input is automatically absorbed.

Date	Version	Revision
07/16/02	2.0	• Updated compatible input standards listed in Table 6.
09/26/02	2.1	• Changed number of resources available to the XC2V40 device in Table 13. • Clarified Power On Reset information under Configuration Sequence.
12/06/02	2.1.1	• Cosmetic edits.
05/07/03	2.1.2	• Added qualification note to Figure 13, page 11. • Corrected sentence in section Input/Output Individual Options, page 4, to read "The optional weak-keeper circuit is connected to each *user I/O pad*." • Corrected typographical errors in Table 3 for names of HSTL_[x]_DCI_18 standards.
06/19/03	2.2	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 5, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Added section Rules for Combining I/O Standards in the Same Bank, page 6.
08/01/03	3.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
10/14/03	3.1	• Added section Local Clocking, page 29. • Table 1, page 1: - Added SSTL18_I and SSTL18_II. - Corrected names of 1.8V HSTL_I-IV standards to "HSTL_I-IV_18". - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. - Changed "N/A" to "N/R" (no requirement). • Table 2, page 2: - Changed "N/A" to "N/R" (no requirement). • Table 3, page 2: - Added SSTL18_I_DCI, SSTL18_II_DCI, LVDS_33_DCI, LVDSEXT_33_DCI, LVDS_25_DCI, and LVDSEXT_25_DCI. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. • Sections Slave-Serial Mode and Master-Serial Mode, page 36: Changed "rising" to "falling" edge with respect to DOUT. • Added verbiage to section Bitstream Encryption, page 38: "For devices that support this feature, please contact your sales representative for specific ordering part number."
03/29/04	3.2	• Table 2, page 2, and Table 5, page 7: Removed LVDS_33_DCI and LVDSEXT_33_DCI from tables. • Table 26, page 37: Updated bitstream lengths. • Section BUFGMUX, page 29: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 44 and associated text from CLK0 and CLK1 to I0 and I1. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1, page 1: Added example to Footnote (1) regarding V_{CCO} rules for GTL and GTLP. • Added reference to Pb-free package types in Figure 7, page 6.
03/01/05	3.4	• Reassigned heading hierarchies for better agreement with content. • Table 2: Corrected V_{OD} output voltages. • Table 26: Updated bitstream lengths.
11/05/07	3.5	• Updated copyright statement and legal disclaimer. • Boundary-Scan (JTAG, IEEE 1532) Mode, page 37: Updated IEEE 1149.1 compliance statement.

Table 14: **IOB Input Switching Characteristics** ***(Continued)***

Description	Symbol	Device	Speed Grade -6	Speed Grade -5	Speed Grade -4	Units
Propagation Delays						
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.83	0.91	1.05	ns, Max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XC2V40	3.23	3.55	4.09	ns, Max
		XC2V80	3.23	3.55	4.09	ns, Max
		XC2V250	3.23	3.55	4.09	ns, Max
		XC2V500	3.23	3.55	4.09	ns, Max
		XC2V1000	3.23	3.55	4.09	ns, Max
		XC2V1500	3.23	3.55	4.09	ns, Max
		XC2V2000	3.23	3.55	4.09	ns, Max
		XC2V3000	3.32	3.65	4.20	ns, Max
		XC2V4000	3.32	3.65	4.20	ns, Max
		XC2V6000	3.60	3.95	4.55	ns, Max
		XC2V8000		3.95	4.55	ns, Max
Clock CLK to output IQ	T_{IOCKIQ}	All		0.67	0.77	ns, Max
Setup and Hold Times With Respect to Clock at IOB Input Register						
Pad, no delay	T_{IOPICK}/T_{IOICKP}	All	0.84/–0.36	0.92/–0.39	1.06/–0.45	ns, Min
Pad, with delay	$T_{IOPICKD}/T_{IOICKPD}$	XC2V40	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V80	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V250	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V1500	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V2000	3.24/–2.04	3.57/–2.24	4.10/–2.58	ns, Min
		XC2V3000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V4000	3.33/–2.10	3.67/–2.31	4.22/–2.66	ns, Min
		XC2V6000	3.61/–2.29	3.97/–2.52	4.56/–2.90	ns, Min
		XC2V8000		3.97/–2.52	4.56/–2.90	ns, Min
ICE input	$T_{IOICECK}/T_{IOCKICE}$	All		0.21/ 0.04	0.24/ 0.04	ns, Min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.27	0.30	0.34	ns, Min
Set/Reset Delays						
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	1.11	1.22	1.40	ns, Max
GSR to output IQ	T_{GSRQ}	All	5.44	5.98	6.88	ns, Max

Notes:
1. Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 18.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 18 shows the test setup parameters used for measuring Input standard adjustments (see Table 15, page 11).

Table 18: **Input Delay Measurement Methodology**

Description	IOSTANDARD Attribute	V_L (1,2)	V_H (1,2)	V_{MEAS} (1,4,5)	V_{REF} (1,3,5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – (0.2 x V_{CCO})	V_{REF} + (0.2 x V_{CCO})	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDS, 3.3V	LVDS_33	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	1.2	
LVDSEXT, 3.3V	LVDSEXT_33	1.2 – 0.125	1.2 + 0.125	1.2	
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	0.6 – 0.125	0.6 + 0.125	0.6	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:
1. Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVCMOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical. See **Virtex-II Platform FPGA User Guide** for min/max specifications.
4. Input voltage level from which measurement starts.
5. Note that this is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.

Input Clock Tolerances

Table 39: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade -6 Min	-6 Max	-5 Min	-5 Max	-4 Min	-4 Max	Units
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN[(3)]	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)[(1)]	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)[(2)]	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)[(1)]	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)[(2)]	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)[(1)]	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)[(2)]	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)[(1)]	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)[(2)]	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

T_X = Data Period - [Jitter[(1)] + Duty Cycle Distortion[(2)] + TCKSKEW[(3)] + TPKGSKEW[(4)]]

Notes:

1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 45.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

R_X = [TSAMP[(1)] + TCKSKEW[(2)] + TPKGSKEW[(3)]]

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Table 18, “Delay Measurement Methodology”
04/23/01	1.5	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L21P_7/VREF_7	F3		
7	IO_L21N_7	F2		
7	IO_L19P_7	H6		
7	IO_L19N_7	H7		
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	D1		
7	IO_L04N_7	D2		
7	IO_L03P_7/VREF_7	C1		
7	IO_L03N_7	C2		
7	IO_L02P_7/VRN_7	E3		
7	IO_L02N_7/VRP_7	E4		
7	IO_L01P_7	G5		
7	IO_L01N_7	F4		
0	VCCO_0	J13		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	H10		
0	VCCO_0	H9		
0	VCCO_0	B10		
0	VCCO_0	B7		
1	VCCO_1	B17		
1	VCCO_1	J16		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	H18		
1	VCCO_1	H17		
1	VCCO_1	B20		
2	VCCO_2	N18		
2	VCCO_2	M18		
2	VCCO_2	L18		
2	VCCO_2	K25		
2	VCCO_2	K19		
2	VCCO_2	J19		
2	VCCO_2	G25		
3	VCCO_3	Y25		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L72N_3	T20
3	IO_L72P_3	T19
3	IO_L70N_3	U27
3	IO_L70P_3	U26
3	IO_L69N_3/VREF_3	U25
3	IO_L69P_3	V25
3	IO_L67N_3	U21
3	IO_L67P_3	U20
3	IO_L54N_3	V27
3	IO_L54P_3	V26
3	IO_L52N_3	V24
3	IO_L52P_3	V23
3	IO_L51N_3/VREF_3	V22
3	IO_L51P_3	W22
3	IO_L49N_3	V21
3	IO_L49P_3	V20
3	IO_L48N_3	W27
3	IO_L48P_3	Y27
3	IO_L46N_3	W26
3	IO_L46P_3	W25
3	IO_L45N_3/VREF_3	W24
3	IO_L45P_3	W23
3	IO_L43N_3	W21
3	IO_L43P_3	W20
3	IO_L28N_3	W19
3	IO_L28P_3	Y19
3	IO_L27N_3/VREF_3	Y25
3	IO_L27P_3	Y24
3	IO_L25N_3	Y23
3	IO_L25P_3	AA23
3	IO_L24N_3	Y22
3	IO_L24P_3	Y21
3	IO_L22N_3	AA27
3	IO_L22P_3	AB27
3	IO_L21N_3/VREF_3	AA26
3	IO_L21P_3	AA25

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	VCCO_1	G16
1	VCCO_1	D21
1	VCCO_1	C16
2	VCCO_2	N18
2	VCCO_2	M25
2	VCCO_2	M21
2	VCCO_2	M18
2	VCCO_2	L19
2	VCCO_2	L18
2	VCCO_2	K19
2	VCCO_2	G24
3	VCCO_3	AA24
3	VCCO_3	V19
3	VCCO_3	U19
3	VCCO_3	U18
3	VCCO_3	T25
3	VCCO_3	T21
3	VCCO_3	T18
3	VCCO_3	R18
4	VCCO_4	AE16
4	VCCO_4	AD21
4	VCCO_4	AA16
4	VCCO_4	W18
4	VCCO_4	W17
4	VCCO_4	V17
4	VCCO_4	V16
4	VCCO_4	V15
5	VCCO_5	AE12
5	VCCO_5	AD7
5	VCCO_5	AA12
5	VCCO_5	W11
5	VCCO_5	W10
5	VCCO_5	V13
5	VCCO_5	V12
5	VCCO_5	V11
6	VCCO_6	AA4

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	VCCO_2	R11	
2	VCCO_2	R5	
2	VCCO_2	P12	
2	VCCO_2	P11	
2	VCCO_2	N12	
2	VCCO_2	N11	
2	VCCO_2	M11	
2	VCCO_2	K1	
2	VCCO_2	G4	
3	VCCO_3	AH4	
3	VCCO_3	AE1	
3	VCCO_3	AC11	
3	VCCO_3	AB12	
3	VCCO_3	AB11	
3	VCCO_3	AA12	
3	VCCO_3	AA11	
3	VCCO_3	Y12	
3	VCCO_3	Y11	
3	VCCO_3	Y5	
3	VCCO_3	W12	
3	VCCO_3	W1	
3	VCCO_3	V12	
4	VCCO_4	AP16	
4	VCCO_4	AP10	
4	VCCO_4	AL7	
4	VCCO_4	AK15	
4	VCCO_4	AD15	
4	VCCO_4	AD14	
4	VCCO_4	AD13	
4	VCCO_4	AD12	
4	VCCO_4	AC17	
4	VCCO_4	AC16	
4	VCCO_4	AC15	
4	VCCO_4	AC14	
4	VCCO_4	AC13	
5	VCCO_5	AP25	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	B34	
NA	GND	B33	
NA	GND	B20	
NA	GND	B15	
NA	GND	B2	
NA	GND	B1	
NA	GND	A33	
NA	GND	A32	
NA	GND	A27	
NA	GND	A8	
NA	GND	A3	
NA	GND	A2	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L09P_2/VREF_2	H7	NC	
2	IO_L10N_2	G3	NC	
2	IO_L10P_2	F3	NC	
2	IO_L11N_2	J8	NC	
2	IO_L11P_2	K8	NC	
2	IO_L12N_2	H5	NC	
2	IO_L12P_2	G5	NC	
2	IO_L19N_2	G1		
2	IO_L19P_2	F1		
2	IO_L20N_2	K9		
2	IO_L20P_2	L10		
2	IO_L21N_2	K7		
2	IO_L21P_2/VREF_2	J7		
2	IO_L22N_2	H2		
2	IO_L22P_2	G2		
2	IO_L23N_2	L9		
2	IO_L23P_2	M9		
2	IO_L24N_2	H4		
2	IO_L24P_2	G4		
2	IO_L25N_2	J3		
2	IO_L25P_2	H3		
2	IO_L26N_2	M10		
2	IO_L26P_2	N10		
2	IO_L27N_2	K6		
2	IO_L27P_2/VREF_2	J6		
2	IO_L28N_2	K5		
2	IO_L28P_2	J5		
2	IO_L29N_2	N11		
2	IO_L29P_2	P11		
2	IO_L30N_2	M7		
2	IO_L30P_2	L7		
2	IO_L31N_2	J1	NC	
2	IO_L31P_2	H1	NC	
2	IO_L32N_2	L8	NC	
2	IO_L32P_2	M8	NC	
2	IO_L33N_2	K4	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L71P_1	B12	
1	IO_L70N_1	C13	
1	IO_L70P_1	C12	
1	IO_L69N_1/VREF_1	H13	
1	IO_L69P_1	H12	
1	IO_L68N_1	D12	
1	IO_L68P_1	D11	
1	IO_L67N_1	B11	
1	IO_L67P_1	B10	
1	IO_L54N_1	E12	
1	IO_L54P_1	E11	
1	IO_L53N_1	A11	
1	IO_L53P_1	A10	
1	IO_L52N_1	G12	
1	IO_L52P_1	G11	
1	IO_L51N_1/VREF_1	K13	
1	IO_L51P_1	K12	
1	IO_L50N_1	C11	
1	IO_L50P_1	C10	
1	IO_L49N_1	B9	
1	IO_L49P_1	B7	
1	IO_L30N_1	F11	NC
1	IO_L30P_1	F9	NC
1	IO_L29N_1	A9	NC
1	IO_L29P_1	A8	NC
1	IO_L27N_1/VREF_1	D9	NC
1	IO_L27P_1	D8	NC
1	IO_L26N_1	J12	NC
1	IO_L26P_1	J11	NC
1	IO_L25N_1	C9	NC
1	IO_L25P_1	C8	NC
1	IO_L24N_1	E10	
1	IO_L24P_1	E9	
1	IO_L23N_1	H11	
1	IO_L23P_1	H10	
1	IO_L22N_1	A7	
1	IO_L22P_1	A6	
1	IO_L21N_1/VREF_1	A5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	VCCO_5	AJ18	
5	VCCO_5	AJ25	
6	VCCO_6	U20	
6	VCCO_6	U21	
6	VCCO_6	V20	
6	VCCO_6	V21	
6	VCCO_6	V24	
6	VCCO_6	V29	
6	VCCO_6	W20	
6	VCCO_6	W21	
6	VCCO_6	Y21	
6	VCCO_6	AB26	
6	VCCO_6	AE29	
7	VCCO_7	G29	
7	VCCO_7	K26	
7	VCCO_7	M21	
7	VCCO_7	N20	
7	VCCO_7	N21	
7	VCCO_7	P20	
7	VCCO_7	P21	
7	VCCO_7	P24	
7	VCCO_7	P29	
7	VCCO_7	R20	
7	VCCO_7	R21	
NA	CCLK	AJ4	
NA	PROG_B	D27	
NA	DONE	AG6	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AG26	
NA	HSWAP_EN	E26	
NA	TCK	K11	
NA	TDI	C28	
NA	TDO	C4	
NA	TMS	J10	
NA	PWRDWN_B	AH5	
NA	DXN	F25	