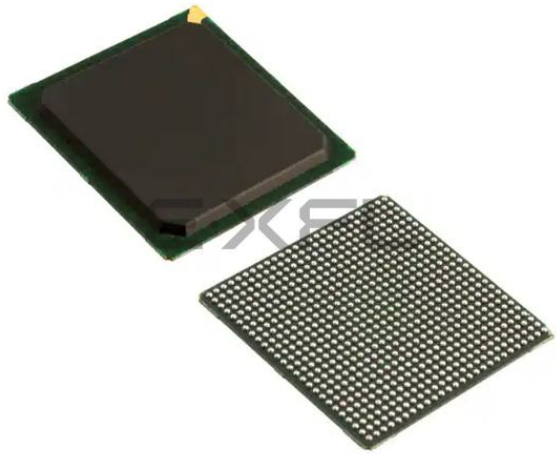

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	-
Total RAM Bits	884736
Number of I/O	392
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1500-4fgg676i

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

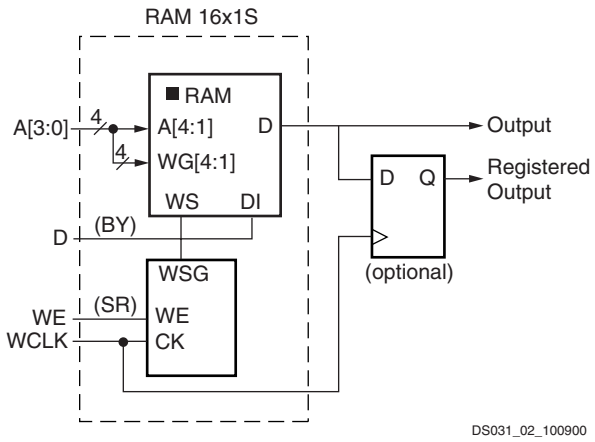


Figure 18: **Distributed SelectRAM (RAM16x1S)**

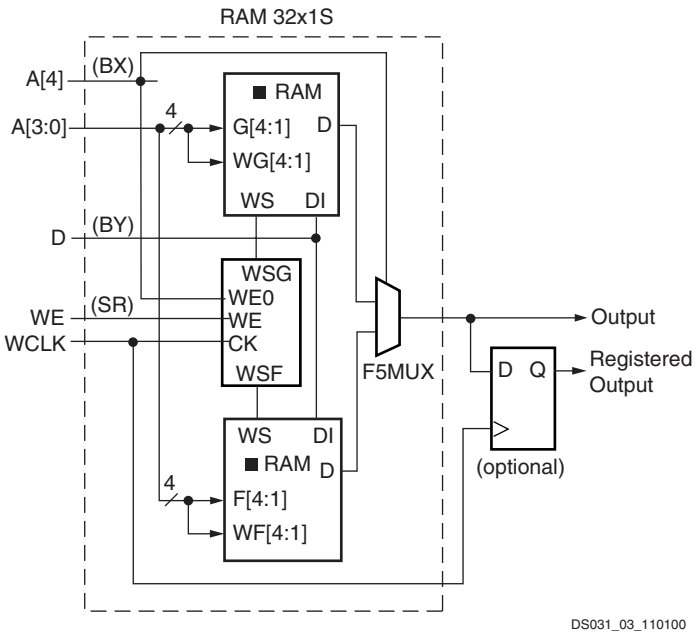


Figure 19: **Single-Port Distributed SelectRAM (RAM32x1S)**

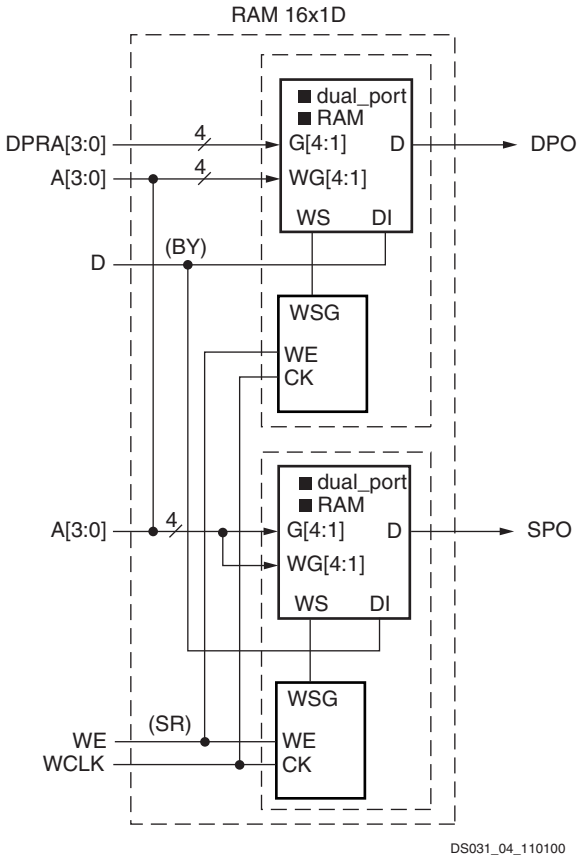


Figure 20: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

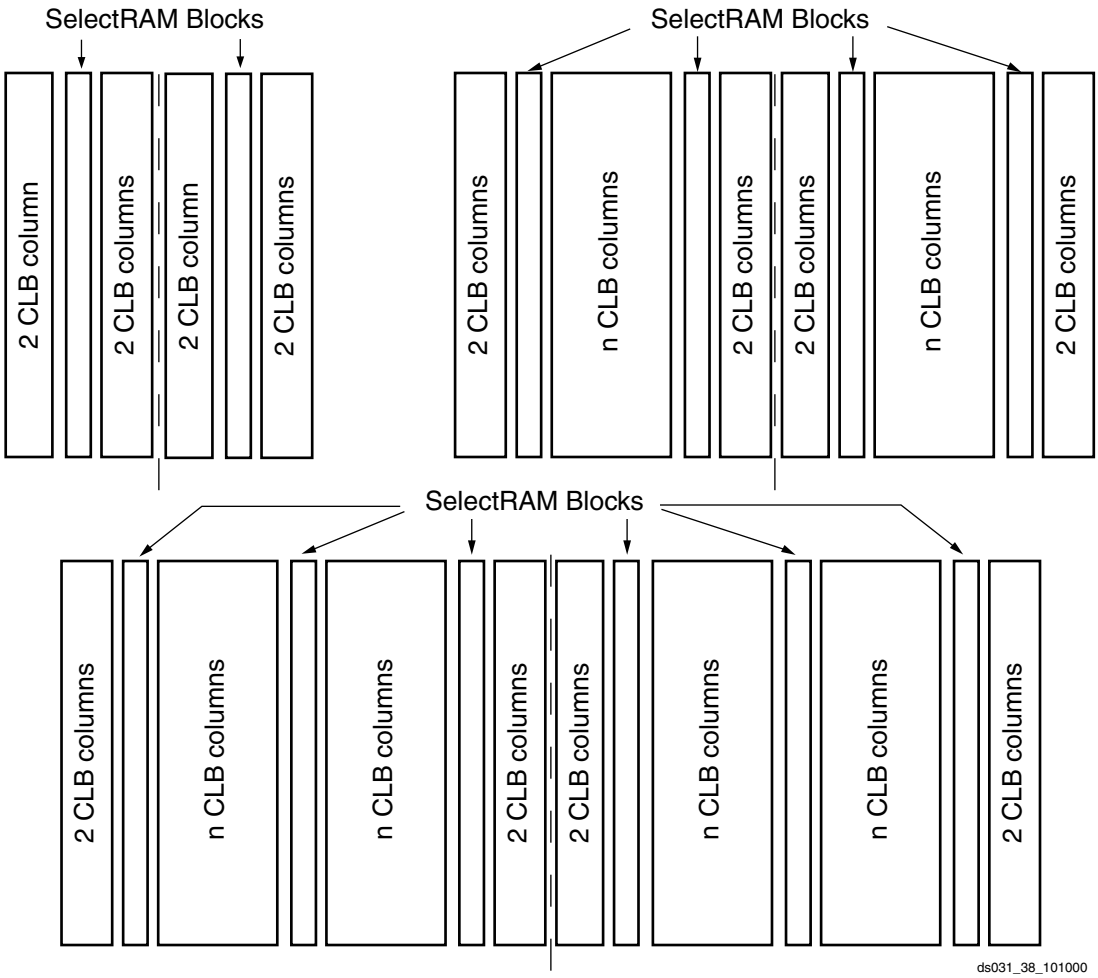


Figure 34: **Block SelectRAM (2-column, 4-column, and 6-column)**

Total Amount of SelectRAM Memory

Table 19 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18 Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 19: **Virtex-II SelectRAM Memory Available**

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
XC2V40	4	72	73,728
XC2V80	8	144	147,456
XC2V250	24	432	442,368
XC2V500	32	576	589,824
XC2V1000	40	720	737,280
XC2V1500	48	864	884,736
XC2V2000	56	1,008	1,032,192
XC2V3000	96	1,728	1,769,472
XC2V4000	120	2,160	2,211,840
XC2V6000	144	2,592	2,654,208
XC2V8000	168	3,024	3,096,576

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

IOB Input Switching Characteristics Standard Adjustments

Table 15 gives all standard-specific data input delay adjustments.

Table 15: **IOB Input Switching Characteristics Standard Adjustments**

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	T_{ILVTTL}	0.00	0.00	0.00	ns
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	$T_{ILVCMOS33}$	0.00	0.00	0.00	ns
LVCMOS, 2.5V	LVCMOS25	$T_{ILVCMOS25}$	0.11	0.11	0.12	ns
LVCMOS, 1.8V	LVCMOS18	$T_{ILVCMOS18}$	0.42	0.43	0.49	ns
LVCMOS, 1.5V	LVCMOS15	$T_{ILVCMOS15}$	0.98	1.00	1.15	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{ILVDS_25}	0.60	0.60	0.69	ns
LVDS, 3.3V	LVDS_33	T_{ILVDS_33}	0.60	0.60	0.69	ns
LVDSEXT (Extended Mode), 2.5V	LVDSEXT_25	$T_{ILVDSEXT\_25}$	0.68	0.69	0.79	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{ILVDSEXT\_33}$	0.56	0.56	0.65	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{IULVDS_25}	0.48	0.49	0.56	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{IBLVDS_25}	0.68	0.69	0.79	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{ILDT_25}	0.48	0.49	0.56	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{ILVPECL\_33}$	0.60	0.60	0.69	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{IPCI33_3}	0.00	0.00	0.00	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{IPCI66_3}	0.00	0.00	0.00	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{IPCIX}	0.00	0.00	0.00	ns
GTL (Gunning Transceiver Logic)	GTL	T_{IGTL}	0.42	0.42	0.48	ns
GTL Plus	GTLP	T_{IGTLP}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{IHSTL_I}	0.42	0.42	0.48	ns
HSTL, Class II	HSTL_II	T_{IHSTL_II}	0.42	0.42	0.48	ns
HSTL, Class III	HSTL_III	T_{IHSTL_III}	0.42	0.42	0.48	ns
HSTL, Class IV	HSTL_IV	T_{IHSTL_IV}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{IHSTL\_I\_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V	HSTL_II_18	$T_{IHSTL\_II\_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{IHSTL\_III\_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{IHSTL\_IV\_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{ISSTL18\_I}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{ISSTL18\_II}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{ISSTL2_I}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{ISSTL2_II}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{ISSTL3_I}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V	SSTL3_ II	T_{ISSTL3_II}	0.35	0.35	0.40	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{IAGP}	0.35	0.35	0.40	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{ILVDCI_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V	LVDCI_25	T_{ILVDCI_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V	LVDCI_18	T_{ILVDCI_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V	LVDCI_15	T_{ILVDCI_15}	0.98	1.00	1.14	ns

Table 17: **IOB Output Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVCMOS, 2.5V, Fast, 16 mA	LVCMOS25_F16	$T_{OLVCMOS25\_F16}$	–0.18	–0.19	–0.21	ns
LVCMOS, 2.5V, Fast, 24 mA	LVCMOS25_F24	$T_{OLVCMOS25\_F24}$	–0.35	–0.36	–0.40	ns
LVCMOS, 1.8V, Slow, 2 mA	LVCMOS18_S2	$T_{OLVCMOS18\_S2}$	15.62	16.10	17.71	ns
LVCMOS, 1.8V, Slow, 4 mA	LVCMOS18_S4	$T_{OLVCMOS18\_S4}$	10.20	10.51	11.57	ns
LVCMOS, 1.8V, Slow, 6 mA	LVCMOS18_S6	$T_{OLVCMOS18\_S6}$	7.52	7.75	8.53	ns
LVCMOS, 1.8V, Slow, 8 mA	LVCMOS18_S8	$T_{OLVCMOS18\_S8}$	6.87	7.08	7.78	ns
LVCMOS, 1.8V, Slow, 12 mA	LVCMOS18_S12	$T_{OLVCMOS18\_S12}$	5.54	5.71	6.28	ns
LVCMOS, 1.8V, Slow, 16 mA	LVCMOS18_S16	$T_{OLVCMOS18\_S16}$	5.31	5.47	6.02	ns
LVCMOS, 1.8V, Fast, 2 mA	LVCMOS18_F2	$T_{OLVCMOS18\_F2}$	5.55	5.72	6.30	ns
LVCMOS, 1.8V, Fast, 4 mA	LVCMOS18_F4	$T_{OLVCMOS18\_F4}$	1.89	1.95	2.15	ns
LVCMOS, 1.8V, Fast, 6 mA	LVCMOS18_F6	$T_{OLVCMOS18\_F6}$	0.83	0.85	0.94	ns
LVCMOS, 1.8V, Fast, 8 mA	LVCMOS18_F8	$T_{OLVCMOS18\_F8}$	0.70	0.72	0.80	ns
LVCMOS, 1.8V, Fast, 12 mA	LVCMOS18_F12	$T_{OLVCMOS18\_F12}$	0.26	0.27	0.30	ns
LVCMOS, 1.8V, Fast, 16 mA	LVCMOS18_F16	$T_{OLVCMOS18\_F16}$	0.23	0.23	0.26	ns
LVCMOS, 1.5V, Slow, 2 mA	LVCMOS15_S2	$T_{OLVCMOS15\_S2}$	18.96	19.55	21.50	ns
LVCMOS, 1.5V, Slow, 4 mA	LVCMOS15_S4	$T_{OLVCMOS15\_S4}$	12.77	13.17	14.48	ns
LVCMOS, 1.5V, Slow, 6 mA	LVCMOS15_S6	$T_{OLVCMOS15\_S6}$	12.05	12.42	13.66	ns
LVCMOS, 1.5V, Slow, 8 mA	LVCMOS15_S8	$T_{OLVCMOS15\_S8}$	9.75	10.06	11.06	ns
LVCMOS, 1.5V, Slow, 12 mA	LVCMOS15_S12	$T_{OLVCMOS15\_S12}$	9.04	9.32	10.25	ns
LVCMOS, 1.5V, Slow, 16 mA	LVCMOS15_S16	$T_{OLVCMOS15\_S16}$	8.21	8.46	9.31	ns
LVCMOS, 1.5V, Fast, 2 mA	LVCMOS15_F2	$T_{OLVCMOS15\_F2}$	5.09	5.25	5.78	ns
LVCMOS, 1.5V, Fast, 4 mA	LVCMOS15_F4	$T_{OLVCMOS15\_F4}$	2.01	2.07	2.27	ns
LVCMOS, 1.5V, Fast, 6 mA	LVCMOS15_F6	$T_{OLVCMOS15\_F6}$	1.46	1.51	1.66	ns
LVCMOS, 1.5V, Fast, 8 mA	LVCMOS15_F8	$T_{OLVCMOS15\_F8}$	0.93	0.96	1.05	ns
LVCMOS, 1.5V, Fast, 12 mA	LVCMOS15_F12	$T_{OLVCMOS15\_F12}$	0.74	0.77	0.84	ns
LVCMOS, 1.5V, Fast, 16 mA	LVCMOS15_F16	$T_{OLVCMOS15\_F16}$	0.67	0.69	0.75	ns
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	T_{OLVDS_25}	–0.31	–0.32	–0.36	ns
LVDS, 3.3V	LVDS_33	T_{OLVDS_33}	–0.25	–0.26	–0.29	ns
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	$T_{OLVDSEXT\_25}$	–0.18	–0.19	–0.21	ns
LVDSEXT, 3.3V	LVDSEXT_33	$T_{OLVDSEXT\_33}$	–0.17	–0.18	–0.19	ns
ULVDS (Ultra LVDS), 2.5V	ULVDS_25	T_{OULVDS_25}	–0.20	–0.21	–0.23	ns
BLVDS (Bus LVDS), 2.5V	BLVDS_25	T_{OBLVDS_25}	0.67	0.69	0.76	ns
LDT (HyperTransport), 2.5V	LDT_25	T_{OLDT_25}	–0.20	–0.21	–0.23	ns
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	$T_{OLVPECL\_33}$	0.29	0.30	0.33	ns
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	T_{OPCI33_3}	1.15	1.19	1.31	ns
PCI, 66 MHz, 3.3V	PCI66_3	T_{OPCI66_3}	–0.01	–0.01	–0.01	ns
PCI-X, 133 MHz, 3.3V	PCIX	T_{OPCIX}	–0.01	–0.01	–0.01	ns
GTL (Gunning Transceiver Logic)	GTL	T_{OGTL}	–0.31	–0.32	–0.36	ns
GTL Plus	GTLP	T_{OGTLP}	–0.17	–0.18	–0.20	ns
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	T_{OHSTL_I}	0.26	0.27	0.29	ns
HSTL, Class II	HSTL_II	T_{OHSTL_II}	–0.15	–0.16	–0.17	ns
HSTL, Class III	HSTL_III	T_{OHSTL_III}	–0.17	–0.17	–0.19	ns
HSTL, Class IV	HSTL_IV	T_{OHSTL_IV}	–0.40	–0.41	–0.45	ns
HSTL, Class I, 1.8V	HSTL_I_18	$T_{OHSTL\_I\_18}$	0.03	0.03	0.04	ns

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. (See ***Virtex-II Platform FPGA User Guide*** for details.) The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in Figure 1.

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. (IBIS models can be found on the web at **http://support.xilinx.com/support/sw_ibis.htm**.) Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 19.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Output Standard Adjustment value (Table 17) to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

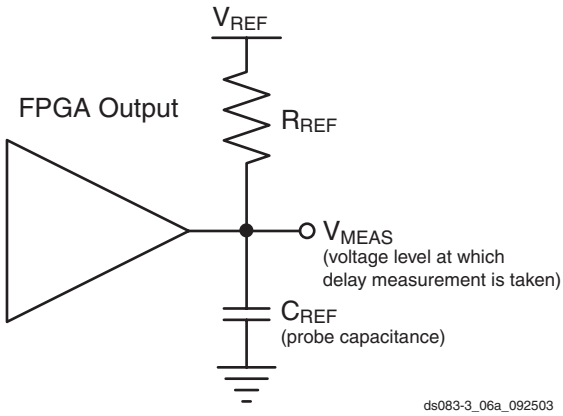


Figure 1: **Generalized Test Setup**

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 (2)	0.94	0
	PCI66_3 (falling edge)	25	10 (2)	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 (3)	0.94	
	PCIX (falling edge	25	10 (3)	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8

Input Clock Tolerances

Table 39: **Input Clock Tolerances**

Description	Symbol	Constraints F_{CLKIN}	Speed Grade						Units
			-6		-5		-4		
			Min	Max	Min	Max	Min	Max	
Input Clock Low/High Pulse Width									
PSCLK	PSCLK_PULSE	< 1MHz	25.00		25.00		25.00		ns
PSCLK and CLKIN(3)	PSCLK_PULSE and CLKIN_PULSE	1 – 10 MHz	25.00		25.00		25.00		ns
		10 – 25 MHz	10.00		10.00		10.00		ns
		25 – 50 MHz	5.00		5.00		5.00		ns
		50 – 100 MHz	3.00		3.00		3.00		ns
		100 – 150 MHz	2.40		2.40		2.40		ns
		150 – 200 MHz	2.00		2.00		2.00		ns
		200 – 250 MHz	1.80		1.80		1.80		ns
		250 – 300 MHz	1.50		1.50		1.50		ns
		300 – 350 MHz	1.30		1.30		1.30		ns
		350 – 400 MHz	1.15		1.15		1.15		ns
		> 400 MHz	1.05		1.05		1.05		ns
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_LF			±300		±300		±300	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_LF			±300		±300		±300	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_CYC_JITT_DLL_HF			±150		±150		±150	ps
CLKIN (using CLKFX outputs)(2)	CLKIN_CYC_JITT_FX_HF			±150		±150		±150	ps
Input Clock Period Jitter (Low Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_LF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_LF			±1		±1		±1	ns
Input Clock Period Jitter (High Frequency Mode)									
CLKIN (using DLL outputs)(1)	CLKIN_PER_JITT_DLL_HF			±1		±1		±1	ns
CLKIN (using CLKFX outputs)(2)	CLKIN_PER_JITT_FX_HF			±1		±1		±1	ns
Feedback Clock Path Delay Variation									
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT			±1		±1		±1	ns

Notes:
1. "DLL outputs" is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. If both DLL and CLKFX outputs are used, follow the more restrictive specification.
3. If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
4	IO_L78N_4	Y15	NC	
4	IO_L78P_4	AA15	NC	
4	IO_L91N_4/VREF_4	W15		
4	IO_L91P_4	W16		
4	IO_L92N_4	AB15		
4	IO_L92P_4	AC15		
4	IO_L93N_4	AD15		
4	IO_L93P_4	AE15		
4	IO_L94N_4/VREF_4	W14		
4	IO_L94P_4	Y14		
4	IO_L95N_4/GCLK3S	AA14		
4	IO_L95P_4/GCLK2P	AB14		
4	IO_L96N_4/GCLK1S	AC14		
4	IO_L96P_4/GCLK0P	AD14		
5	IO_L96N_5/GCLK7S	AC13		
5	IO_L96P_5/GCLK6P	AB13		
5	IO_L95N_5/GCLK5S	AA13		
5	IO_L95P_5/GCLK4P	Y13		
5	IO_L94N_5	W13		
5	IO_L94P_5/VREF_5	W12		
5	IO_L93N_5	AF15		
5	IO_L93P_5	AF14		
5	IO_L92N_5	AF13		
5	IO_L92P_5	AF12		
5	IO_L91N_5	AE12		
5	IO_L91P_5/VREF_5	AD12		
5	IO_L78N_5	AC12	NC	
5	IO_L78P_5	AB12	NC	
5	IO_L76N_5	AA12	NC	
5	IO_L76P_5	Y12	NC	
5	IO_L75N_5/VREF_5	AF11	NC	
5	IO_L75P_5	AF10	NC	
5	IO_L73N_5	AE11	NC	
5	IO_L73P_5	AD11	NC	
5	IO_L72N_5	AC11		
5	IO_L72P_5	AB11		

BG575/BGG575 Standard BGA Package

As shown in Table 9, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the BG575/BGG575 BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch).

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
0	IO_L01N_0	A3		
0	IO_L01P_0	A4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	E6		
0	IO_L03P_0/VRN_0	D6		
0	IO_L04N_0/VREF_0	F7		
0	IO_L04P_0	E7		
0	IO_L05N_0	G8		
0	IO_L05P_0	H9		
0	IO_L06N_0	A5		
0	IO_L06P_0	A6		
0	IO_L19N_0	B5		
0	IO_L19P_0	B6		
0	IO_L21N_0	D7		
0	IO_L21P_0/VREF_0	C7		
0	IO_L22N_0	F8		
0	IO_L22P_0	E8		
0	IO_L24N_0	G9		
0	IO_L24P_0	F9		
0	IO_L49N_0	G10		
0	IO_L49P_0	H10		
0	IO_L51N_0	B7		
0	IO_L51P_0/VREF_0	B8		
0	IO_L52N_0	D8		
0	IO_L52P_0	C8		
0	IO_L54N_0	E9		
0	IO_L54P_0	D9		
0	IO_L67N_0	A8	NC	
0	IO_L67P_0	A9	NC	
0	IO_L69N_0	C9	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L91N_6	P4		
6	IO_L93P_6	N4		
6	IO_L93N_6/VREF_6	N3		
6	IO_L94P_6	N6		
6	IO_L94N_6	N5		
6	IO_L96P_6	N8		
6	IO_L96N_6	N7		
7	IO_L96P_7	N2		
7	IO_L96N_7	M1		
7	IO_L94P_7	M2		
7	IO_L94N_7	M3		
7	IO_L93P_7/VREF_7	M4		
7	IO_L93N_7	M5		
7	IO_L91P_7	M6		
7	IO_L91N_7	M7		
7	IO_L73P_7	M8	NC	NC
7	IO_L73N_7	L8	NC	NC
7	IO_L72P_7	L1	NC	
7	IO_L72N_7	K1	NC	
7	IO_L70P_7	K2	NC	
7	IO_L70N_7	K3	NC	
7	IO_L69P_7/VREF_7	L3	NC	
7	IO_L69N_7	L4	NC	
7	IO_L67P_7	L5	NC	
7	IO_L67N_7	L7	NC	
7	IO_L54P_7	J1		
7	IO_L54N_7	H1		
7	IO_L52P_7	J2		
7	IO_L52N_7	J3		
7	IO_L51P_7/VREF_7	J4		
7	IO_L51N_7	J5		
7	IO_L49P_7	K5		
7	IO_L49N_7	K6		
7	IO_L48P_7	F1		
7	IO_L48N_7	F2		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	VBATT	A2		
NA	RSVD	E6		
NA	VCCAUX	AK28		
NA	VCCAUX	AK16		
NA	VCCAUX	AK3		
NA	VCCAUX	T1		
NA	VCCAUX	R30		
NA	VCCAUX	A28		
NA	VCCAUX	A15		
NA	VCCAUX	A3		
NA	VCCINT	AB22		
NA	VCCINT	AB9		
NA	VCCINT	AA21		
NA	VCCINT	AA10		
NA	VCCINT	Y20		
NA	VCCINT	Y19		
NA	VCCINT	Y18		
NA	VCCINT	Y17		
NA	VCCINT	Y16		
NA	VCCINT	Y15		
NA	VCCINT	Y14		
NA	VCCINT	Y13		
NA	VCCINT	Y12		
NA	VCCINT	Y11		
NA	VCCINT	W20		
NA	VCCINT	W11		
NA	VCCINT	V20		
NA	VCCINT	V11		
NA	VCCINT	U20		
NA	VCCINT	U11		
NA	VCCINT	T20		
NA	VCCINT	T11		
NA	VCCINT	R20		
NA	VCCINT	R11		
NA	VCCINT	P20		
NA	VCCINT	P11		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

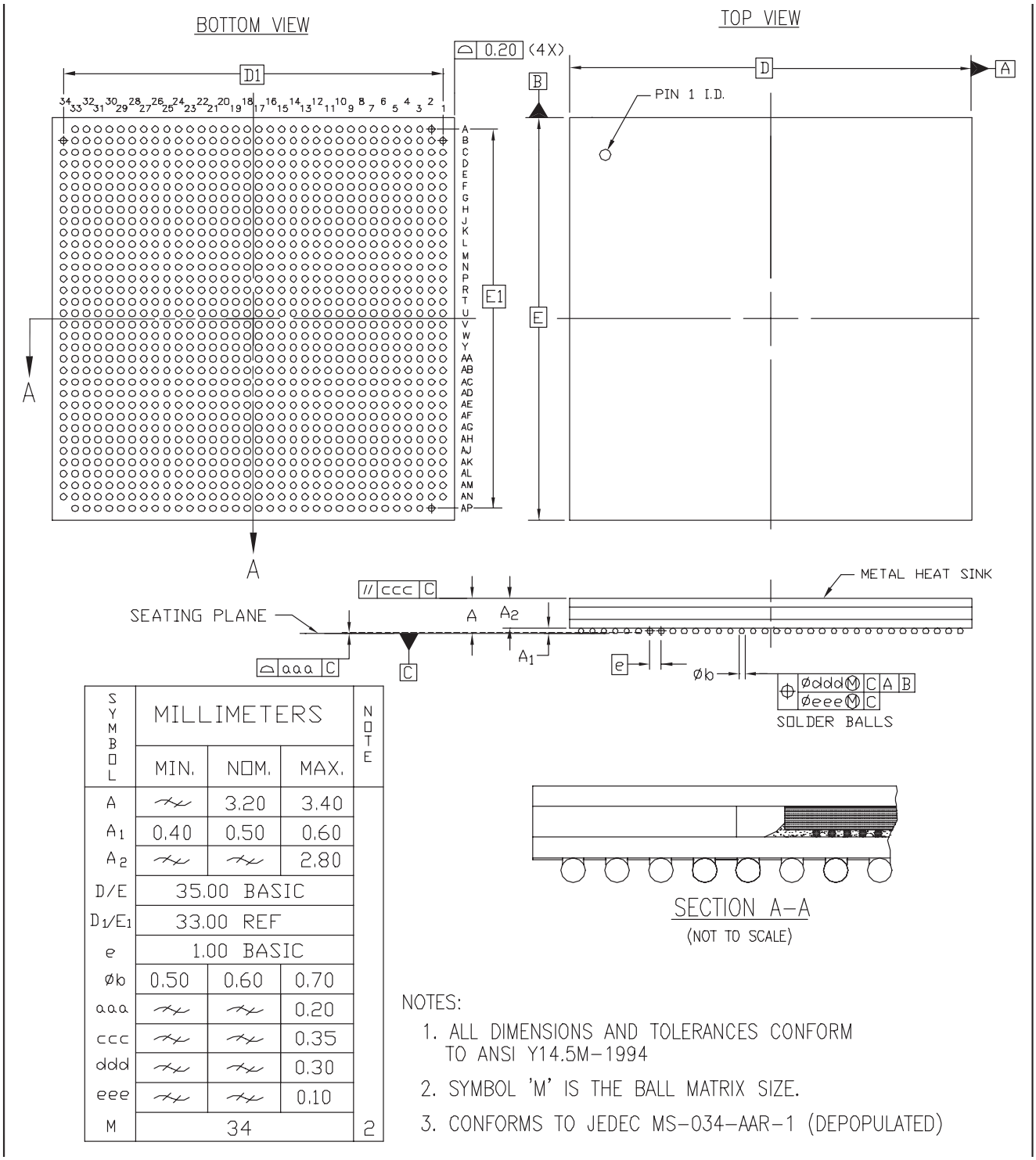
Bank	Pin Description	Pin Number	No Connect in the XC2V3000
1	IO_L93P_1	F17	
1	IO_L92N_1	G16	
1	IO_L92P_1	G17	
1	IO_L91N_1	C16	
1	IO_L91P_1/VREF_1	C15	
1	IO_L84N_1	D14	NC
1	IO_L84P_1	D15	NC
1	IO_L83N_1	J17	NC
1	IO_L83P_1	K17	NC
1	IO_L82N_1	B17	NC
1	IO_L82P_1	A17	NC
1	IO_L81N_1/VREF_1	A15	NC
1	IO_L81P_1	B16	NC
1	IO_L80N_1	L17	NC
1	IO_L80P_1	L16	NC
1	IO_L79N_1	A13	NC
1	IO_L79P_1	A14	NC
1	IO_L78N_1	C13	
1	IO_L78P_1	C14	
1	IO_L77N_1	K16	
1	IO_L77P_1	K15	
1	IO_L76N_1	B13	
1	IO_L76P_1	B14	
1	IO_L75N_1/VREF_1	F15	
1	IO_L75P_1	G15	
1	IO_L74N_1	H15	
1	IO_L74P_1	H14	
1	IO_L73N_1	A11	
1	IO_L73P_1	A12	
1	IO_L72N_1	E13	
1	IO_L72P_1	E14	
1	IO_L71N_1	J15	
1	IO_L71P_1	J14	
1	IO_L70N_1	D12	
1	IO_L70P_1	D13	
1	IO_L69N_1/VREF_1	F14	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	B34	
NA	GND	B33	
NA	GND	B20	
NA	GND	B15	
NA	GND	B2	
NA	GND	B1	
NA	GND	A33	
NA	GND	A32	
NA	GND	A27	
NA	GND	A8	
NA	GND	A3	
NA	GND	A2	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 8: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	VCCO_1	E11		
1	VCCO_1	C18		
1	VCCO_1	B14		
2	VCCO_2	W14		
2	VCCO_2	W13		
2	VCCO_2	V14		
2	VCCO_2	V13		
2	VCCO_2	V3		
2	VCCO_2	U14		
2	VCCO_2	U13		
2	VCCO_2	U11		
2	VCCO_2	T14		
2	VCCO_2	T13		
2	VCCO_2	R14		
2	VCCO_2	R13		
2	VCCO_2	R9		
2	VCCO_2	P13		
2	VCCO_2	P2		
2	VCCO_2	N7		
2	VCCO_2	L5		
3	VCCO_3	AJ5		
3	VCCO_3	AG7		
3	VCCO_3	AF13		
3	VCCO_3	AF2		
3	VCCO_3	AE14		
3	VCCO_3	AE13		
3	VCCO_3	AE9		
3	VCCO_3	AD14		
3	VCCO_3	AD13		
3	VCCO_3	AC14		
3	VCCO_3	AC13		
3	VCCO_3	AC11		
3	VCCO_3	AB14		
3	VCCO_3	AB13		
3	VCCO_3	AB3		
3	VCCO_3	AA14		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	
7	IO_L53P_7	L30	

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules: