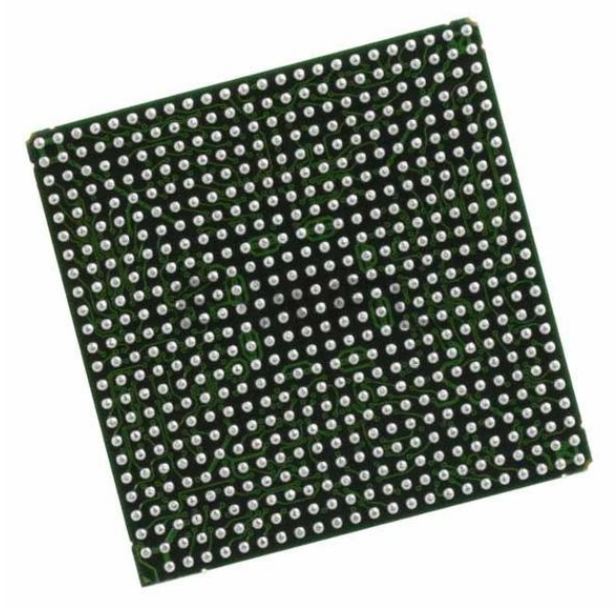
AMD Xilinx - XC2V1500-5BGG575C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	-
Total RAM Bits	884736
Number of I/O	392
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1500-5bgg575c

- HSTL (Class I, II, III, and IV)
- SSTL (3.3V and 2.5V, Class I and II)
- AGP-2X

The digitally controlled impedance (DCI) I/O feature automatically provides on-chip termination for each I/O element.

The IOB elements also support the following differential signaling I/O standards:

- LVDS
- BLVDS (Bus LVDS)
- ULVDS
- LDT
- LVPECL

Two adjacent pads are used for each differential pair. Two or four IOB blocks connect to one switch matrix to access the routing resources.

Configurable Logic Blocks (CLBs)

CLB resources include four slices and two 3-state buffers. Each slice is equivalent and contains:

- Two function generators (F & G)
- Two storage elements
- Arithmetic logic gates
- Large multiplexers
- Wide function capability
- Fast carry look-ahead chain
- Horizontal cascade chain (OR gate)

The function generators F & G are configurable as 4-input look-up tables (LUTs), as 16-bit shift registers, or as 16-bit distributed SelectRAM memory.

In addition, the two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches.

Each CLB has internal fast interconnect and connects to a switch matrix to access general routing resources.

Block SelectRAM Memory

The block SelectRAM memory resources are 18 Kb of dual-port RAM, programmable from 16K x 1 bit to 512 x 36 bits, in various depth and width configurations. Each port is totally synchronous and independent, offering three "read-during-write" modes. Block SelectRAM memory is cascadable to implement large embedded storage blocks. Supported memory configurations for dual-port and single-port modes are shown in Table 3.

Table 3: **Dual-Port And Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

A multiplier block is associated with each SelectRAM memory block. The multiplier block is a dedicated 18 x 18-bit multiplier and is optimized for operations based on the block SelectRAM content on one port. The 18 x 18 multiplier can be used independently of the block SelectRAM resource. Read/multiply/accumulate operations and DSP filter structures are extremely efficient.

Both the SelectRAM memory and the multiplier resource are connected to four switch matrices to access the general routing resources.

Global Clocking

The DCM and global clock multiplexer buffers provide a complete solution for designing high-speed clocking schemes.

Up to 12 DCM blocks are available. To generate de-skewed internal or external clocks, each DCM can be used to eliminate clock distribution delay. The DCM also provides 90-, 180-, and 270-degree phase-shifted versions of its output clocks. Fine-grained phase shifting offers high-resolution phase adjustments in increments of 1/256 of the clock period. Very flexible frequency synthesis provides a clock output frequency equal to any M/D ratio of the input clock frequency, where M and D are two integers. For the exact timing parameters, see Virtex-II Electrical Characteristics.

Virtex-II devices have 16 global clock MUX buffers, with up to eight clock nets per quadrant. Each global clock MUX buffer can select one of the two clock inputs and switch glitch-free from one clock to the other. Each DCM block is able to drive up to four of the 16 global clock MUX buffers.

Routing Resources

The IOB, CLB, block SelectRAM, multiplier, and DCM elements all use the same interconnect scheme and the same access to the global routing matrix. Timing models are shared, greatly improving the predictability of the performance of high-speed designs.

There are a total of 16 global clock lines, with eight available per quadrant. In addition, 24 vertical and horizontal long lines per row or column as well as massive secondary and local routing resources provide fast interconnect. Virtex-II buffered interconnects are relatively unaffected by net fanout and the interconnect layout is designed to minimize crosstalk.

Horizontal and vertical routing resources for each row or column include:

- 24 long lines
- 120 hex lines
- 40 double lines
- 16 direct connect lines (total in all four directions)

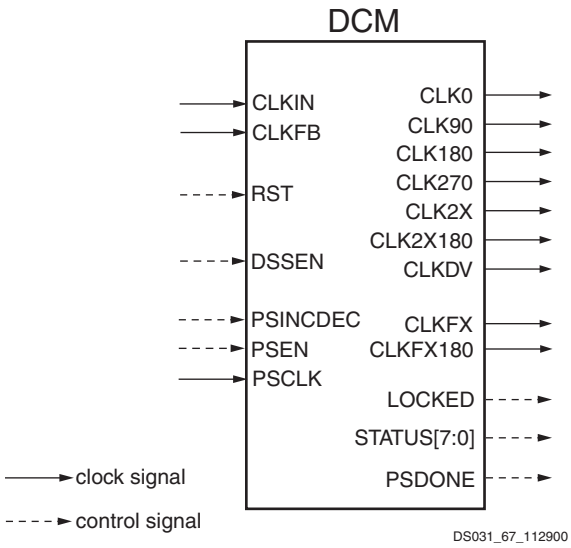

Figure 45: **Digital Clock Manager**

The DCM can be configured to delay the completion of the Virtex-II configuration process until after the DCM has achieved lock. This guarantees that the chip does not begin operating until after the system clocks generated by the DCM have stabilized.

The DCM has the following general control signals:

- RST input pin: resets the entire DCM
- LOCKED output pin: asserted High when all enabled DCM circuits have locked.
- STATUS output pins (active High): shown in Table 21.

Table 21: **DCM Status Pins**

Status Pin	Function
0	Phase Shift Overflow
1	CLKIN Stopped
2	CLKFX Stopped
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A

Clock De-Skew

The DCM de-skews the output clocks relative to the input clock by automatically adjusting a digital delay line. Additional delay is introduced so that clock edges arrive at internal registers and block RAMs simultaneously with the clock edges arriving at the input clock pad. Alternatively, external clocks, which are also de-skewed relative to the input clock, can be generated for board-level routing. All DCM output clocks are phase-aligned to CLK0 and, therefore, are also phase-aligned to the input clock.

To achieve clock de-skew, the CLKFB input must be connected, and its source must be either CLK0 or CLK2X. Note that CLKFB must always be connected, unless only the CLKFX or CLKFX180 outputs are used and de-skew is not required.

Frequency Synthesis

The DCM provides flexible methods for generating new clock frequencies. Each method has a different operating frequency range and different AC characteristics. The CLK2X and CLK2X180 outputs double the clock frequency. The CLKDV output creates divided output clocks with division options of 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

The CLKFX and CLKFX180 outputs can be used to produce clocks at the following frequency:

$$FREQ_{CLKFX} = (M/D) * FREQ_{CLKIN}$$

where M and D are two integers. Specifications for M and D are provided under DCM Timing Parameters in Module 3. By default, M=4 and D=1, which results in a clock output frequency four times faster than the clock input frequency (CLKIN).

CLK2X180 is phase shifted 180 degrees relative to CLK2X. CLKFX180 is phase shifted 180 degrees relative to CLKFX. All frequency synthesis outputs automatically have 50/50 duty cycles (with the exception of the CLKDV output when performing a non-integer divide in high-frequency mode).

Note that CLK2X and CLK2X180 are not available in high-frequency mode.

Phase Shifting

The DCM provides additional control over clock skew through either coarse or fine-grained phase shifting. The CLK0, CLK90, CLK180, and CLK270 outputs are each phase shifted by ¼ of the input clock period relative to each other, providing coarse phase control. Note that CLK90 and CLK270 are not available in high-frequency mode.

Fine-phase adjustment affects all nine DCM output clocks. When activated, the phase shift between the rising edges of CLKIN and CLKFB is a specified fraction of the input clock period.

In variable mode, the PHASE_SHIFT value can also be dynamically incremented or decremented as determined by PSINCDEC synchronously to PSCLK, when the PSEN input is active. Figure 46 illustrates the effects of fine-phase shifting. For more information on DCM features, see the Virtex-II *User Guide*.

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Block SelectRAM Switching Characteristics

Table 28: **Block SelectRAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}	2.10	2.31	2.65	ns, Max
Setup and Hold Times Before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
DIN inputs	T_{BDCK}/T_{BCKD}	0.29/ 0.00	0.32/ 0.00	0.36/ 0.00	ns, Min
EN input	T_{BECK}/T_{BCKE}	0.95/–0.46	1.04/–0.50	1.20/–0.58	ns, Min
RST input	T_{BRCK}/T_{BCKR}	1.31/–0.71	1.44/–0.78	1.65/–0.90	ns, Min
WEN input	T_{BWCK}/T_{BCKW}	0.57/–0.19	0.63/–0.21	0.72/–0.25	ns, Min
Clock CLK					
CLKA to CLKB setup time for different ports	T_{BCCS}	1.0	1.0	1.0	ns, min
Minimum Pulse Width, High	T_{BPWH}	1.17	1.29	1.48	ns, Min
Minimum Pulse Width, Low	T_{BPWL}	1.17	1.29	1.48	ns, Min

TBUF Switching Characteristics

Table 29: **TBUF Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
IN input to OUT output	T_{IO}	0.45	0.50	0.58	ns, Max
TRI input to OUT output high-impedance	T_{OFF}	0.44	0.48	0.55	ns, Max
TRI input to valid data on OUT output	T_{ON}	0.44	0.48	0.55	ns, Max

Date	Version	Revision
07/30/01	1.6	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added values to the Virtex-II Pin-to-Pin Output Parameter Guidelines and Virtex-II Pin-to-Pin Input Parameter Guidelines tables. • Added Frequency Synthesis table.
10/02/01	1.7	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Updated the speed grade designations used in data sheets, and added Table 13, which shows the current speed grade designation for each device.
10/05/01	1.8	• Corrected the speed grade designation for the XC2V1000 device in Table 13.
10/12/01	1.9	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables.
11/28/01	2.0	• Updated values in Table 3, Table 4, Table 5, Virtex-II Performance Characteristics, and Virtex-II Switching Characteristics tables.
01/03/02	2.1	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.96**. • Changed the speed grade designation for the XC2V6000 device in Table 13.
07/16/02	2.2	• Updated values in Table 4, "Quiescent Supply Current." • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.111**. • Added Enhanced Multiplier Switching Characteristics section. • Added footnote to Table 37, "Global Clock Setup and Hold for LVTTL Standard, Without DCM." • Added Source-Synchronous Switching Characteristics section.
09/26/02	2.3	• Removed mention of MIL-M-38510/605 specification. • Added footnotes to Table 2 and Table 6.
12/06/02	2.4	• Revised SSTL2 values in Table 6 to match the latest JEDEC specification. • Added footnote regarding V_{IN} PCI compliance to Table 1. • Added footnote regarding CLKOUT_DUTY_CYCLE_DLL to Table 41.
05/07/03	2.5	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.114**. • Table 4, Quiescent Supply Current, and Table 5, Minimum Power On Current Required for Virtex-II Devices: Added parameters for XC2V8000 device. • Table 16, IOB Output Switching Characteristics: Changed parameter designator T_{IOTON} to T_{IOTP}. • Table 26, Enhanced Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULT\_P[nn]}$ to $T_{MULT1\_P[nn]}$ in order to correspond with designators used in speedsfile. • Table 27, Enhanced Pipelined Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULTCK\_P[nn]}$ to $T_{MULTCK1\_P[nn]}$ in order to correspond with designators used in speedsfile. • Removed old Table 19, **Standard Capacitive Loads**. • Added Figure 1, page 17, showing test configuration for measuring I/O standard adjustments.
06/19/03	2.5.1	• Removed footnotes in Table 34 and Table 36 that stated DCM jitter was included in the measurements.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
2	IO_L45N_2	H23		
2	IO_L45P_2/VREF_2	H24		
2	IO_L46N_2	J21		
2	IO_L46P_2	J20		
2	IO_L48N_2	H25		
2	IO_L48P_2	H26		
2	IO_L49N_2	J22		
2	IO_L49P_2	J23		
2	IO_L51N_2	K21		
2	IO_L51P_2/VREF_2	K22		
2	IO_L52N_2	K20		
2	IO_L52P_2	L20		
2	IO_L54N_2	J24		
2	IO_L54P_2	J25		
2	IO_L67N_2	K23		
2	IO_L67P_2	K24		
2	IO_L69N_2	J26		
2	IO_L69P_2/VREF_2	K26		
2	IO_L70N_2	L22		
2	IO_L70P_2	L21		
2	IO_L72N_2	L25		
2	IO_L72P_2	L26		
2	IO_L73N_2	L19	NC	
2	IO_L73P_2	M19	NC	
2	IO_L75N_2	L23	NC	
2	IO_L75P_2/VREF_2	L24	NC	
2	IO_L76N_2	M22	NC	
2	IO_L76P_2	M21	NC	
2	IO_L78N_2	M23	NC	
2	IO_L78P_2	M24	NC	
2	IO_L91N_2	M25		
2	IO_L91P_2	M26		
2	IO_L93N_2	M20		
2	IO_L93P_2/VREF_2	N20		
2	IO_L94N_2	N22		
2	IO_L94P_2	N21		
2	IO_L96N_2	N24		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	VCCO_3	V19		
3	VCCO_3	U25		
3	VCCO_3	U19		
3	VCCO_3	T18		
3	VCCO_3	R18		
3	VCCO_3	P18		
4	VCCO_4	AE20		
4	VCCO_4	AE17		
4	VCCO_4	W18		
4	VCCO_4	W17		
4	VCCO_4	V16		
4	VCCO_4	V15		
4	VCCO_4	V14		
5	VCCO_5	AE10		
5	VCCO_5	AE7		
5	VCCO_5	W10		
5	VCCO_5	W9		
5	VCCO_5	V13		
5	VCCO_5	V12		
5	VCCO_5	V11		
6	VCCO_6	Y2		
6	VCCO_6	V8		
6	VCCO_6	U8		
6	VCCO_6	U2		
6	VCCO_6	T9		
6	VCCO_6	R9		
6	VCCO_6	P9		
7	VCCO_7	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	K8		
7	VCCO_7	K2		
7	VCCO_7	J8		
7	VCCO_7	G2		
NA	CCLK	AB21		
NA	PROG_B	C4		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	VCCO_1	B14		
2	VCCO_2	M16		
2	VCCO_2	L23		
2	VCCO_2	L19		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	F22		
3	VCCO_3	W22		
3	VCCO_3	R16		
3	VCCO_3	P23		
3	VCCO_3	P19		
3	VCCO_3	P16		
3	VCCO_3	N16		
4	VCCO_4	AC14		
4	VCCO_4	AB19		
4	VCCO_4	W14		
4	VCCO_4	T15		
4	VCCO_4	T14		
4	VCCO_4	T13		
5	VCCO_5	AC11		
5	VCCO_5	AB6		
5	VCCO_5	W11		
5	VCCO_5	T12		
5	VCCO_5	T11		
5	VCCO_5	T10		
6	VCCO_6	W3		
6	VCCO_6	R9		
6	VCCO_6	P9		
6	VCCO_6	P6		
6	VCCO_6	P2		
6	VCCO_6	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	L6		
7	VCCO_7	L2		
7	VCCO_7	K9		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
6	IO_L52N_6	V3
6	IO_L54P_6	V2
6	IO_L54N_6	V1
6	IO_L67P_6	U8
6	IO_L67N_6	T8
6	IO_L69P_6	U6
6	IO_L69N_6/VREF_6	U7
6	IO_L70P_6	U4
6	IO_L70N_6	U3
6	IO_L72P_6	U2
6	IO_L72N_6	U1
6	IO_L73P_6	T9
6	IO_L73N_6	R9
6	IO_L75P_6	T5
6	IO_L75N_6/VREF_6	T6
6	IO_L76P_6	T4
6	IO_L76N_6	R4
6	IO_L78P_6	T2
6	IO_L78N_6	T1
6	IO_L91P_6	R7
6	IO_L91N_6	R8
6	IO_L93P_6	R5
6	IO_L93N_6/VREF_6	R6
6	IO_L94P_6	R3
6	IO_L94N_6	P3
6	IO_L96P_6	R2
6	IO_L96N_6	R1
7	IO_L96P_7	P5
7	IO_L96N_7	P6
7	IO_L94P_7	P7
7	IO_L94N_7	P8
7	IO_L93P_7/VREF_7	N1
7	IO_L93N_7	N2
7	IO_L91P_7	N3
7	IO_L91N_7	N4

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	VCCO_2	L10		
2	VCCO_2	L9		
2	VCCO_2	K9		
2	VCCO_2	E2		
3	VCCO_3	AF2		
3	VCCO_3	AA9		
3	VCCO_3	Y10		
3	VCCO_3	Y9		
3	VCCO_3	W10		
3	VCCO_3	W9		
3	VCCO_3	V10		
3	VCCO_3	V9		
3	VCCO_3	V3		
3	VCCO_3	U10		
3	VCCO_3	T10		
4	VCCO_4	AJ5		
4	VCCO_4	AH13		
4	VCCO_4	AB13		
4	VCCO_4	AB12		
4	VCCO_4	AB11		
4	VCCO_4	AB10		
4	VCCO_4	AA15		
4	VCCO_4	AA14		
4	VCCO_4	AA13		
4	VCCO_4	AA12		
4	VCCO_4	AA11		
5	VCCO_5	AJ26		
5	VCCO_5	AH18		
5	VCCO_5	AB21		
5	VCCO_5	AB20		
5	VCCO_5	AB19		
5	VCCO_5	AB18		
5	VCCO_5	AA20		
5	VCCO_5	AA19		
5	VCCO_5	AA18		
5	VCCO_5	AA17		
5	VCCO_5	AA16		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	M5		
NA	GND	K28		
NA	GND	K3		
NA	GND	H30		
NA	GND	H1		
NA	GND	G17		
NA	GND	G14		
NA	GND	F25		
NA	GND	F6		
NA	GND	E26		
NA	GND	E19		
NA	GND	E12		
NA	GND	E5		
NA	GND	D27		
NA	GND	D4		
NA	GND	C28		
NA	GND	C21		
NA	GND	C10		
NA	GND	C3		
NA	GND	B29		
NA	GND	B2		
NA	GND	A23		
NA	GND	A8		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
3	IO_L23P_3	AJ3	
3	IO_L22N_3	AF7	
3	IO_L22P_3	AG7	
3	IO_L21N_3/VREF_3	AL1	
3	IO_L21P_3	AK1	
3	IO_L20N_3	AH2	
3	IO_L20P_3	AJ2	
3	IO_L19N_3	AJ4	
3	IO_L19P_3	AK4	
3	IO_L06N_3	AE10	
3	IO_L06P_3	AD10	
3	IO_L05N_3	AK2	
3	IO_L05P_3	AL2	
3	IO_L04N_3	AH6	
3	IO_L04P_3	AJ5	
3	IO_L03N_3/VREF_3	AE11	
3	IO_L03P_3	AF11	
3	IO_L02N_3/VRP_3	AK3	
3	IO_L02P_3/VRN_3	AL3	
3	IO_L01N_3	AF10	
3	IO_L01P_3	AG9	
4	IO_L01N_4/BUSY/DOUT(1)	AM4	
4	IO_L01P_4/INIT_B	AL5	
4	IO_L02N_4/D0/DIN(1)	AG10	
4	IO_L02P_4/D1	AH11	
4	IO_L03N_4/D2/ALT_VRP_4	AK7	
4	IO_L03P_4/D3/ALT_VRN_4	AK8	
4	IO_L04N_4/VREF_4	AL6	
4	IO_L04P_4	AM6	
4	IO_L05N_4/VRP_4	AK9	
4	IO_L05P_4/VRN_4	AJ8	
4	IO_L06N_4	AM8	
4	IO_L06P_4	AM7	
4	IO_L19N_4	AN3	
4	IO_L19P_4	AM2	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L95P_6	W30	
6	IO_L95N_6	V30	
6	IO_L96P_6	V32	
6	IO_L96N_6	W32	
7	IO_L96P_7	U31	
7	IO_L96N_7	V31	
7	IO_L95P_7	T28	
7	IO_L95N_7	U28	
7	IO_L94P_7	U33	
7	IO_L94N_7	U34	
7	IO_L93P_7/VREF_7	U29	
7	IO_L93N_7	T29	
7	IO_L92P_7	U27	
7	IO_L92N_7	U26	
7	IO_L91P_7	T30	
7	IO_L91N_7	U30	
7	IO_L84P_7	R32	NC
7	IO_L84N_7	T32	NC
7	IO_L83P_7	U25	NC
7	IO_L83N_7	T25	NC
7	IO_L82P_7	R34	NC
7	IO_L82N_7	T33	NC
7	IO_L81P_7/VREF_7	N34	NC
7	IO_L81N_7	P34	NC
7	IO_L80P_7	U24	NC
7	IO_L80N_7	T24	NC
7	IO_L79P_7	R31	NC
7	IO_L79N_7	T31	NC
7	IO_L78P_7	N32	
7	IO_L78N_7	P32	
7	IO_L77P_7	T27	
7	IO_L77N_7	R27	
7	IO_L76P_7	N33	
7	IO_L76N_7	P33	
7	IO_L75P_7/VREF_7	R29	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	AB17	
NA	VCCINT	AB16	
NA	VCCINT	AB15	
NA	VCCINT	AB14	
NA	VCCINT	AB13	
NA	VCCINT	AA22	
NA	VCCINT	AA13	
NA	VCCINT	Y22	
NA	VCCINT	Y13	
NA	VCCINT	W22	
NA	VCCINT	W13	
NA	VCCINT	V22	
NA	VCCINT	V13	
NA	VCCINT	U22	
NA	VCCINT	U13	
NA	VCCINT	T22	
NA	VCCINT	T13	
NA	VCCINT	R22	
NA	VCCINT	R13	
NA	VCCINT	P22	
NA	VCCINT	P13	
NA	VCCINT	N22	
NA	VCCINT	N21	
NA	VCCINT	N20	
NA	VCCINT	N19	
NA	VCCINT	N18	
NA	VCCINT	N17	
NA	VCCINT	N16	
NA	VCCINT	N15	
NA	VCCINT	N14	
NA	VCCINT	N13	
NA	VCCINT	M23	
NA	VCCINT	M12	
NA	VCCINT	L24	
NA	VCCINT	L11	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
4	IO_L78N_4	AJ13	
4	IO_L78P_4	AK13	
4	IO_L91N_4/VREF_4	AC15	
4	IO_L91P_4	AC16	
4	IO_L92N_4	AG14	
4	IO_L92P_4	AG15	
4	IO_L93N_4	AK14	
4	IO_L93P_4	AK15	
4	IO_L94N_4/VREF_4	AF16	
4	IO_L94P_4	AG16	
4	IO_L95N_4/GCLK3S	AL14	
4	IO_L95P_4/GCLK2P	AL15	
4	IO_L96N_4/GCLK1S	AH15	
4	IO_L96P_4/GCLK0P	AJ15	
5	IO_L96N_5/GCLK7S	AJ16	
5	IO_L96P_5/GCLK6P	AH17	
5	IO_L95N_5/GCLK5S	AD16	
5	IO_L95P_5/GCLK4P	AD17	
5	IO_L94N_5	AL17	
5	IO_L94P_5/VREF_5	AL18	
5	IO_L93N_5	AG17	
5	IO_L93P_5	AF17	
5	IO_L92N_5	AE17	
5	IO_L92P_5	AE18	
5	IO_L91N_5	AK17	
5	IO_L91P_5/VREF_5	AJ17	
5	IO_L78N_5	AK18	
5	IO_L78P_5	AK19	
5	IO_L77N_5	AC17	
5	IO_L77P_5	AB18	
5	IO_L76N_5	AH18	
5	IO_L76P_5	AH19	
5	IO_L75N_5/VREF_5	AL19	
5	IO_L75P_5	AL20	
5	IO_L74N_5	AC18	
5	IO_L74P_5	AC19	
5	IO_L73N_5	AJ19	