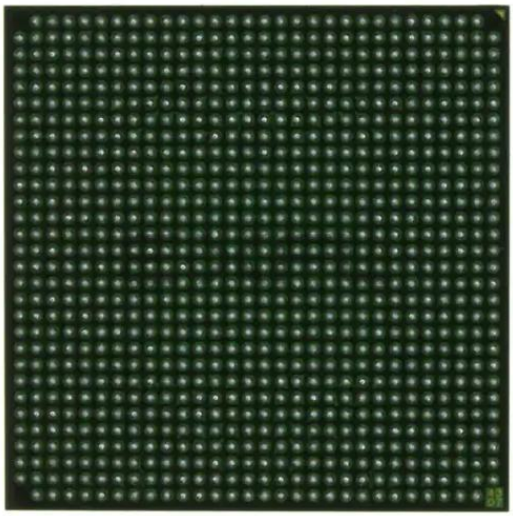

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	-
Total RAM Bits	884736
Number of I/O	528
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1500-5ffg896i

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

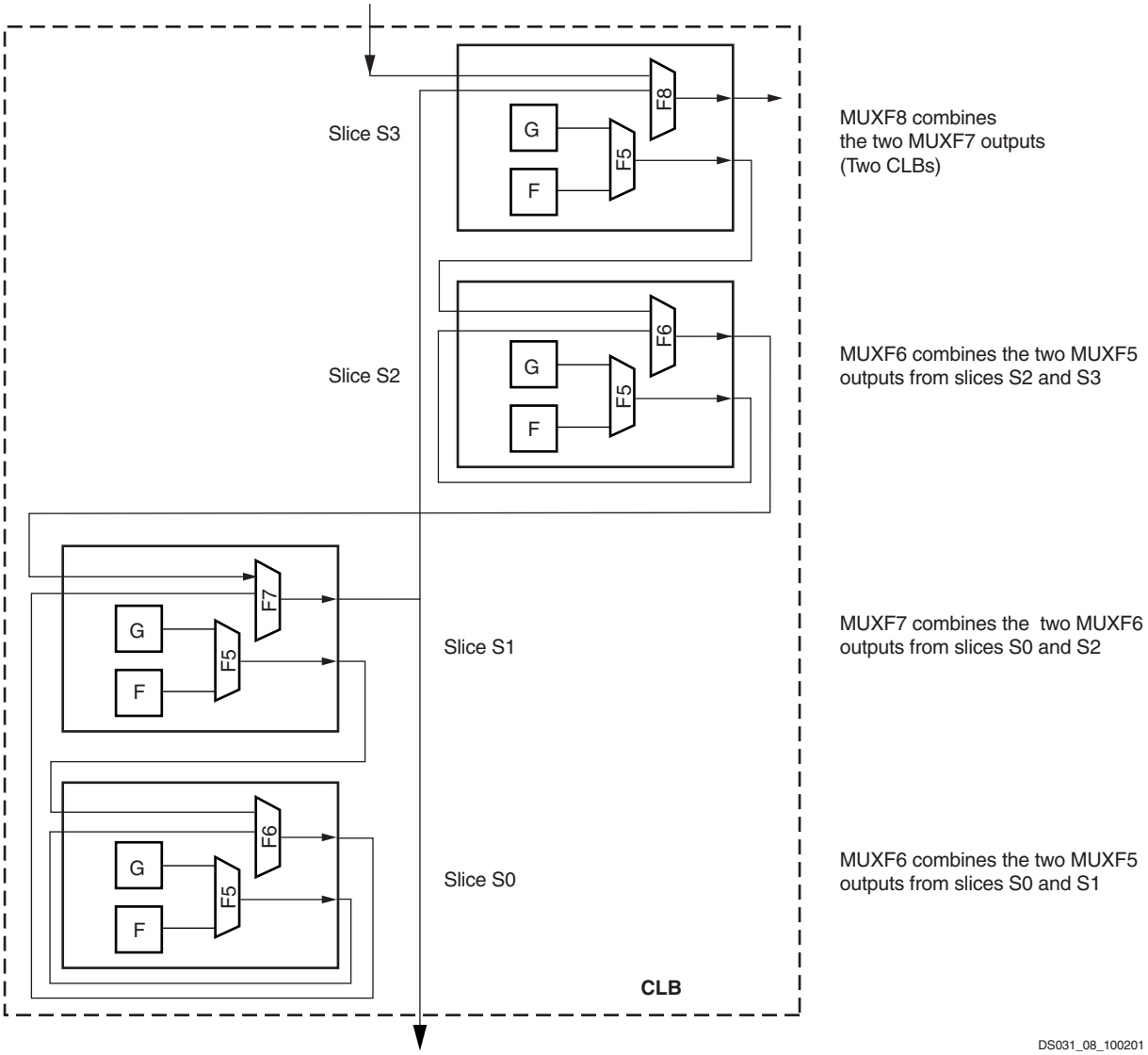


Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

The Virtex-II implementation process is comprised of Synthesis, translation, mapping, place and route, and configuration file generation. While the tools can be run individually, many designers choose to run the entire implementation process with the click of a button. To assist those who prefer to script their design flows, Xilinx provides Xflow, an automated single command line process.

Design Verification

In addition to conventional design verification using static timing analysis or simulation techniques, Xilinx offers powerful in-circuit debugging techniques using ChipScope ILA (Integrated Logic Analysis). The reconfigurable nature of Xilinx FPGAs means that designs can be verified in real time without the need for extensive sets of software simulation vectors.

For simulation, the system extracts post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. The back annotation features a variety of patented Xilinx techniques, resulting in the industry's most powerful simulation flows. Alternatively, timing-critical portions of a design can be verified using the Xilinx static timing analyzer or a third party static timing analysis tool like Synopsys Prime Time™, by exporting timing data in the STAMP data format.

For in-circuit debugging, ChipScope ILA enables designers to analyze the real-time behavior of a device while operating at full system speeds. Logic analysis commands and captured data are transferred between the ChipScope software and ILA cores within the Virtex-II FPGA, using industry standard JTAG protocols. These JTAG transactions are driven over an optional download cable (MultiLINX or JTAG), connecting the Virtex device in the target system to a PC or workstation.

ChipScope ILA was designed to look and feel like a logic analyzer, making it easy to begin debugging a design immediately. Modifications to the desired logic analysis can be downloaded directly into the system in a matter of minutes.

Other Unique Features of Virtex-II Design Flow

Xilinx design flows feature a number of unique capabilities. Among these are efficient incremental HDL design flows; a robust capability that is enabled by Xilinx exclusive hierarchical floorplanning capabilities. Another powerful design capability only available in the Xilinx design flow is "Modular Design", part of the Xilinx suite of team design tools, which enables autonomous design, implementation, and verification of design modules.

Incremental Synthesis

Xilinx unique hierarchical floorplanning capabilities enable designers to create a programmable logic design by isolating design changes within one hierarchical "logic block", and perform synthesis, verification and implementation processes on that specific logic block. By preserving the logic in unchanged portions of a design, Xilinx incremental design makes the high-density design process more efficient.

Xilinx hierarchical floorplanning capabilities can be specified using the high-level floorplanner or a preferred RTL floorplanner (see the Xilinx web site for a list of supported EDA partners). When used in conjunction with one of the EDA partners' floorplanners, higher performance results can be achieved, as many synthesis tools use this more predictable detailed physical implementation information to establish more aggressive and accurate timing estimates when performing their logic optimizations.

Modular Design

Xilinx innovative modular design capabilities take the incremental design process one step further by enabling the designer to delegate responsibility for completing the design, synthesis, verification, and implementation of a hierarchical "logic block" to an arbitrary number of designers - assigning a specific region within the target FPGA for exclusive use by each of the team members.

This team design capability enables an autonomous approach to design modules, changing the hand-off point to the lead designer or integrator from "my module works in simulation" to "my module works in the FPGA". This unique design methodology also leverages the Xilinx hierarchical floorplanning capabilities and enables the Xilinx (or EDA partner) floorplanner to manage the efficient implementation of very high-density FPGAs.

Virtex-II FPGA device. Timing is similar to the Slave Serial-MAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Table 15: **IOB Input Switching Characteristics Standard Adjustments *(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{ILVDCI\_DV2\_33}$	0.00	0.00	0.00	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{ILVDCI\_DV2\_25}$	0.11	0.11	0.12	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{ILVDCI\_DV2\_18}$	0.42	0.43	0.49	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{ILVDCI\_DV2\_15}$	0.98	1.00	1.14	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{IHSLVDCI\_15}$	0.42	0.42	0.48	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{IHSLVDCI\_18}$	0.52	0.53	0.60	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{IHSLVDCI\_25}$	0.42	0.42	0.48	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{IHSLVDCI\_33}$	0.42	0.42	0.48	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{IGTL_DCI}	0.42	0.42	0.48	ns
GTL Plus with DCI	GTLP_DCI	T_{IGTLP_DCI}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{IHSTL\_I\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{IHSTL\_II\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{IHSTL\_III\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{IHSTL\_IV\_DCI}$	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{IHSTL\_I\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{IHSTL\_II\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{IHSTL\_III\_DCI\_18}$	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{IHSTL\_IV\_DCI\_18}$	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{ISSTL18\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{ISSTL18\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{ISSTL2\_I\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{ISSTL2\_II\_DCI}$	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{ISSTL3\_I\_DCI}$	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{ISSTL3\_II\_DCI}$	0.35	0.35	0.40	ns
LVDS (Low-Voltage Differential Signaling), 2.5V, with DCI	LVDS_25_DCI	$T_{ILVDS\_25\_DCI}$	0.60	0.60	0.69	ns
LVDS, 3.3V, with DCI	LVDS_33_DCI	$T_{ILVDS\_33\_DCI}$	0.60	0.60	0.69	ns
LVDSEXT (LVDS Extended Mode), 2.5V, with DCI	LVDSEXT_25_DCI	$T_{ILVDSEXT\_25\_DCI}$	0.58	0.59	0.79	ns
LVDSEXT, 3.3V, with DCI	LVDSEXT_33_DCI	$T_{ILVDSEXT\_33\_DCI}$	0.56	0.56	0.65	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see Table 18.

Clock Distribution Switching Characteristics

Table 20: **Clock Distribution Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Global Clock Buffer I input to O output	T_{GIO}	0.47	0.52	0.59	ns, Max
Global Clock Buffer S input Setup/Hold to I1 an I2 inputs	T_{GSI}/T_{GIS}	0.55/ 0	0.61/ 0	0.70/ 0	ns, Max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used (see Figure 16 in Module 2). The values listed below are worst-case. Precise values are provided by the timing analyzer.

Table 21: **CLB Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.35	0.39	0.44	ns, Max
5-input function: F/G inputs to F5 output	T_{IF5}	0.57	0.63	0.72	ns, Max
5-input function: F/G inputs to X output	T_{IF5X}	0.76	0.83	0.95	ns, Max
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}	0.36	0.39	0.45	ns, Max
FXINA input to FX output via MUXFX	T_{INAFX}	0.26	0.28	0.32	ns, Max
FXINB input to FX output via MUXFX	T_{INBFX}	0.26	0.28	0.32	ns, Max
SOPIN input to SOPOUT output via ORCY	T_{SOPSOP}	0.35	0.38	0.44	ns, Max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.41	0.45	0.51	ns, Max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.45	0.50	0.57	ns, Max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.54	0.59	0.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DY inputs	T_{DYCK}/T_{CKDY}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
DX inputs	T_{DXCK}/T_{CKDX}	0.30/–0.07	0.33/–0.08	0.37/–0.09	ns, Min
CE input	T_{CECK}/T_{CKCE}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}	0.21/–0.02	0.23/–0.03	0.26/–0.03	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{CH}	0.61	0.67	0.77	ns, Min
Minimum Pulse Width, Low	T_{CL}	0.61	0.67	0.77	ns, Min
Set/Reset					
Minimum Pulse Width, SR/BY inputs (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	1.06	1.17	1.34	ns, Max
Toggle Frequency (MHz) (for export control)	F_{TOG}	820	750	650	MHz

Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	$T_{MULTCK1\_P35}$	3.05	3.25	3.74	ns, Max
Clock to Pin 34	$T_{MULTCK1\_P34}$	2.95	3.14	3.61	ns, Max
Clock to Pin 33	$T_{MULTCK1\_P33}$	2.85	3.04	3.49	ns, Max
Clock to Pin 32	$T_{MULTCK1\_P32}$	2.76	2.93	3.37	ns, Max
Clock to Pin 31	$T_{MULTCK1\_P31}$	2.66	2.82	3.25	ns, Max
Clock to Pin 30	$T_{MULTCK1\_P30}$	2.56	2.72	3.12	ns, Max
Clock to Pin 29	$T_{MULTCK1\_P29}$	2.47	2.61	3.00	ns, Max
Clock to Pin 28	$T_{MULTCK1\_P28}$	2.37	2.50	2.88	ns, Max
Clock to Pin 27	$T_{MULTCK1\_P27}$	2.27	2.40	2.75	ns, Max
Clock to Pin 26	$T_{MULTCK1\_P26}$	2.17	2.29	2.63	ns, Max
Clock to Pin 25	$T_{MULTCK1\_P25}$	2.08	2.18	2.51	ns, Max
Clock to Pin 24	$T_{MULTCK1\_P24}$	1.98	2.07	2.38	ns, Max
Clock to Pin 23	$T_{MULTCK1\_P23}$	1.88	1.97	2.26	ns, Max
Clock to Pin 22	$T_{MULTCK1\_P22}$	1.79	1.86	2.14	ns, Max
Clock to Pin 21	$T_{MULTCK1\_P21}$	1.69	1.75	2.02	ns, Max
Clock to Pin 20	$T_{MULTCK1\_P20}$	1.59	1.65	1.89	ns, Max
Clock to Pin 19	$T_{MULTCK1\_P19}$	1.50	1.54	1.77	ns, Max
Clock to Pin 18	$T_{MULTCK1\_P18}$	1.40	1.43	1.65	ns, Max
Clock to Pin 17	$T_{MULTCK1\_P17}$	1.30	1.33	1.52	ns, Max
Clock to Pin 16	$T_{MULTCK1\_P16}$	1.20	1.22	1.40	ns, Max
Clock to Pin 15	$T_{MULTCK1\_P15}$	1.11	1.11	1.28	ns, Max
Clock to Pin 14	$T_{MULTCK1\_P14}$	1.01	1.00	1.15	ns, Max
Clock to Pin 13	$T_{MULTCK1\_P13}$	0.91	1.00	1.15	ns, Max
Clock to Pin 12	$T_{MULTCK1\_P12}$	0.91	1.00	1.15	ns, Max
Clock to Pin 11	$T_{MULTCK1\_P11}$	0.91	1.00	1.15	ns, Max
Clock to Pin 10	$T_{MULTCK1\_P10}$	0.91	1.00	1.15	ns, Max
Clock to Pin 9	$T_{MULTCK1\_P9}$	0.91	1.00	1.15	ns, Max
Clock to Pin 8	$T_{MULTCK1\_P8}$	0.91	1.00	1.15	ns, Max
Clock to Pin 7	$T_{MULTCK1\_P7}$	0.91	1.00	1.15	ns, Max
Clock to Pin 6	$T_{MULTCK1\_P6}$	0.91	1.00	1.15	ns, Max
Clock to Pin 5	$T_{MULTCK1\_P5}$	0.91	1.00	1.15	ns, Max
Clock to Pin 4	$T_{MULTCK1\_P4}$	0.91	1.00	1.15	ns, Max
Clock to Pin 3	$T_{MULTCK1\_P3}$	0.91	1.00	1.15	ns, Max
Clock to Pin 2	$T_{MULTCK1\_P2}$	0.91	1.00	1.15	ns, Max
Clock to Pin 1	$T_{MULTCK1\_P1}$	0.91	1.00	1.15	ns, Max
Clock to Pin 0	$T_{MULTCK1\_P0}$	0.91	1.00	1.15	ns, Max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

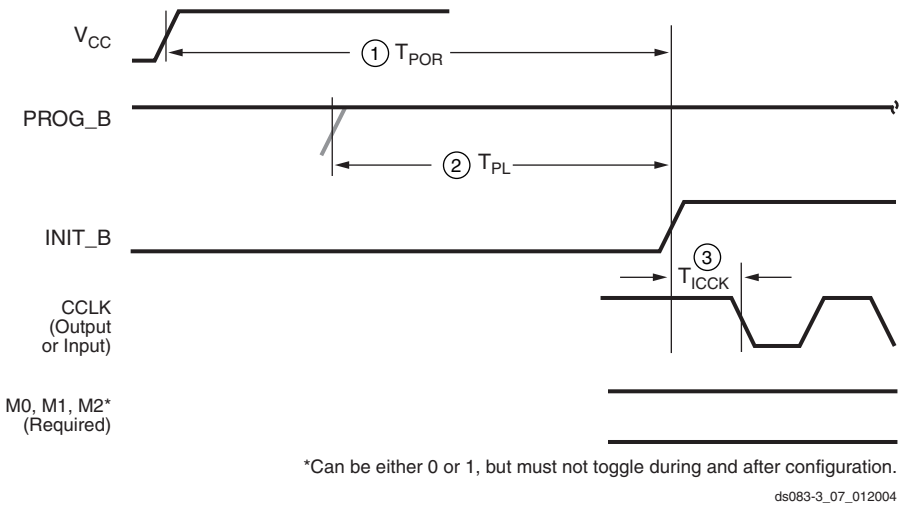


Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	µs, min
			4.0	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM

Table 35: **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *Without* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
LVTTL Global Clock Input to Output Delay using Output flip-flop, 12 mA, Fast Slew Rate, *without* DCM. For data *output* with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.						
Global Clock and OFF without DCM	T_{ICKOF}	XC2V40	3.46	3.58	3.69	ns
		XC2V80	3.62	3.58	3.69	ns
		XC2V250	3.79	3.88	4.47	ns
		XC2V500	3.85	3.88	4.47	ns
		XC2V1000	4.02	4.28	4.62	ns
		XC2V1500	4.16	4.28	4.62	ns
		XC2V2000	4.30	4.43	5.10	ns
		XC2V3000	4.49	4.64	5.34	ns
		XC2V4000	4.82	4.99	5.74	ns
		XC2V6000	5.19	5.38	5.93	ns
		XC2V8000		6.09	7.00	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with test setup shown in Figure 1. For other I/O standards, see Table 19.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

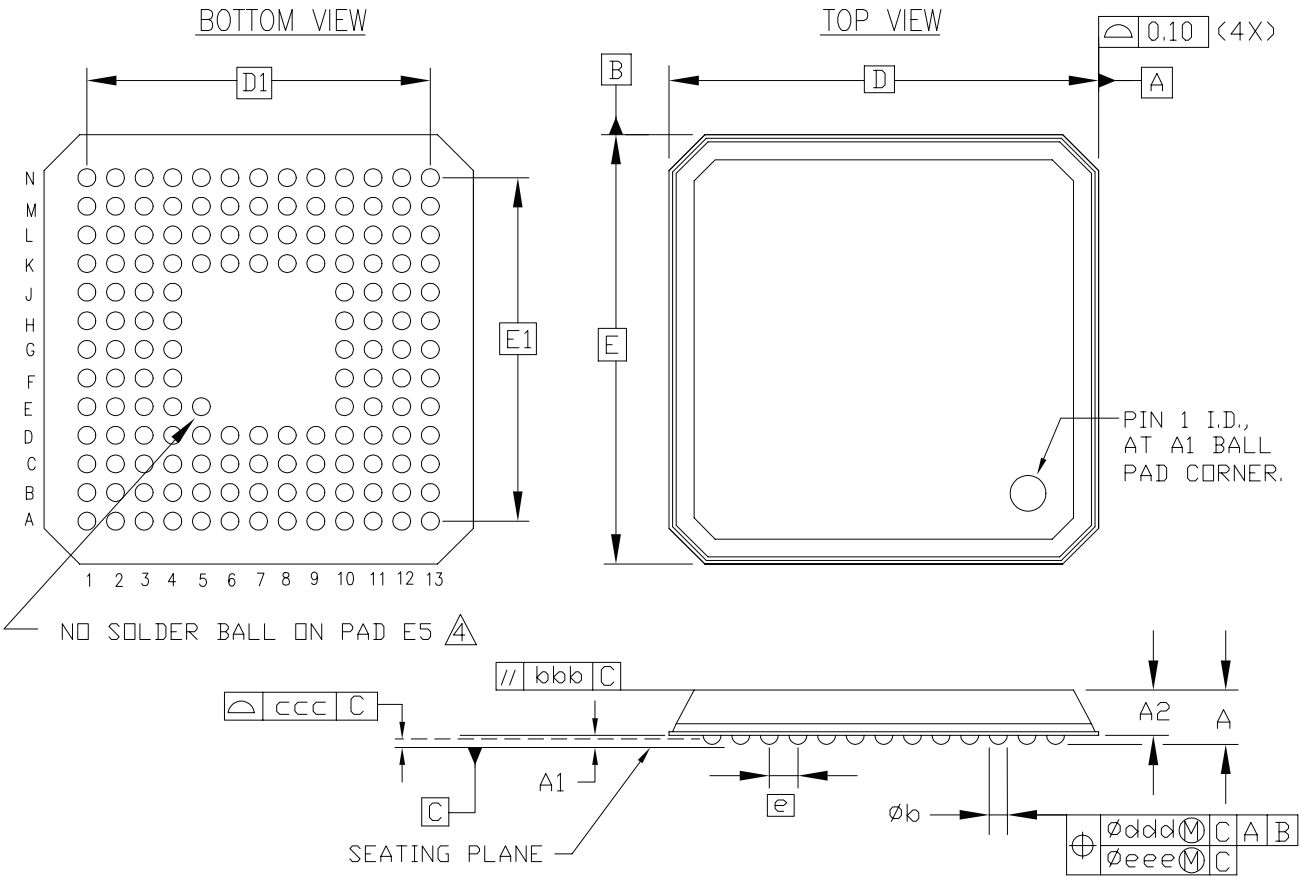
Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 36: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000		1.70/–0.90	1.96/–0.76	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	~	1.20
A_1	0.20	~	~
A_2	0.65	~	~
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.40	0.45	0.50
bbb	~	~	0.20
ccc	~	~	0.12
ddd	~	~	0.15
eee	~	~	0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAG–2 (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144–BALL CHIP SCALE BGA (CS144/CSG144)

Figure 1: **CS144/CSG144 Chip-Scale BGA Package Specifications**

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
NA	GND	T16		
NA	GND	T1		
NA	GND	R15		
NA	GND	R2		
NA	GND	P14		
NA	GND	P3		
NA	GND	L11		
NA	GND	L6		
NA	GND	K10		
NA	GND	K9		
NA	GND	K8		
NA	GND	K7		
NA	GND	J10		
NA	GND	J9		
NA	GND	J8		
NA	GND	J7		
NA	GND	H10		
NA	GND	H9		
NA	GND	H8		
NA	GND	H7		
NA	GND	G10		
NA	GND	G9		
NA	GND	G8		
NA	GND	G7		
NA	GND	F11		
NA	GND	F6		
NA	GND	C14		
NA	GND	C3		
NA	GND	B15		
NA	GND	B2		
NA	GND	A16		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
3	IO_L52P_3	P18	NC	
3	IO_L51N_3/VREF_3	P22	NC	
3	IO_L51P_3	P21	NC	
3	IO_L49N_3	P20	NC	
3	IO_L49P_3	P19	NC	
3	IO_L48N_3	R22		
3	IO_L48P_3	R21		
3	IO_L46N_3	R20		
3	IO_L46P_3	R19		
3	IO_L45N_3/VREF_3	R18		
3	IO_L45P_3	P17		
3	IO_L43N_3	T22		
3	IO_L43P_3	T21		
3	IO_L24N_3	T20	NC	NC
3	IO_L24P_3	T19	NC	NC
3	IO_L22N_3	U22	NC	NC
3	IO_L22P_3	U21	NC	NC
3	IO_L21N_3/VREF_3	U20	NC	NC
3	IO_L21P_3	U19	NC	NC
3	IO_L19N_3	T18	NC	NC
3	IO_L19P_3	U18	NC	NC
3	IO_L06N_3	V22		
3	IO_L06P_3	V21		
3	IO_L04N_3	V20		
3	IO_L04P_3	V19		
3	IO_L03N_3/VREF_3	W22		
3	IO_L03P_3	W21		
3	IO_L02N_3/VRP_3	Y22		
3	IO_L02P_3/VRN_3	Y21		
3	IO_L01N_3	W20		
3	IO_L01P_3	AA20		
4	IO_L01N_4/BUSY/DOUT(1)	AB19		
4	IO_L01P_4/INIT_B	AA19		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L72N_3	T20
3	IO_L72P_3	T19
3	IO_L70N_3	U27
3	IO_L70P_3	U26
3	IO_L69N_3/VREF_3	U25
3	IO_L69P_3	V25
3	IO_L67N_3	U21
3	IO_L67P_3	U20
3	IO_L54N_3	V27
3	IO_L54P_3	V26
3	IO_L52N_3	V24
3	IO_L52P_3	V23
3	IO_L51N_3/VREF_3	V22
3	IO_L51P_3	W22
3	IO_L49N_3	V21
3	IO_L49P_3	V20
3	IO_L48N_3	W27
3	IO_L48P_3	Y27
3	IO_L46N_3	W26
3	IO_L46P_3	W25
3	IO_L45N_3/VREF_3	W24
3	IO_L45P_3	W23
3	IO_L43N_3	W21
3	IO_L43P_3	W20
3	IO_L28N_3	W19
3	IO_L28P_3	Y19
3	IO_L27N_3/VREF_3	Y25
3	IO_L27P_3	Y24
3	IO_L25N_3	Y23
3	IO_L25P_3	AA23
3	IO_L24N_3	Y22
3	IO_L24P_3	Y21
3	IO_L22N_3	AA27
3	IO_L22P_3	AB27
3	IO_L21N_3/VREF_3	AA26
3	IO_L21P_3	AA25

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
NA	GND	F22
NA	GND	F6
NA	GND	E23
NA	GND	E17
NA	GND	E11
NA	GND	E5
NA	GND	D24
NA	GND	D14
NA	GND	D4
NA	GND	C25
NA	GND	C3
NA	GND	B27
NA	GND	B26
NA	GND	B20
NA	GND	B8
NA	GND	B2
NA	GND	B1
NA	GND	A27
NA	GND	A26
NA	GND	A14
NA	GND	A2

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
1	IO_L68P_1	G12	NC	
1	IO_L67N_1	A9	NC	
1	IO_L67P_1	A10	NC	
1	IO_L54N_1	E10		
1	IO_L54P_1	E11		
1	IO_L53N_1	H12		
1	IO_L53P_1	H11		
1	IO_L52N_1	D9		
1	IO_L52P_1	D10		
1	IO_L51N_1/VREF_1	C9		
1	IO_L51P_1	C8		
1	IO_L50N_1	F11		
1	IO_L50P_1	F10		
1	IO_L49N_1	B8		
1	IO_L49P_1	B9		
1	IO_L24N_1	E8		
1	IO_L24P_1	E9		
1	IO_L23N_1	G11		
1	IO_L23P_1	H10		
1	IO_L22N_1	B7		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	D8		
1	IO_L21P_1	E7		
1	IO_L20N_1	G10		
1	IO_L20P_1	G9		
1	IO_L19N_1	A5		
1	IO_L19P_1	A6		
1	IO_L06N_1	C6		
1	IO_L06P_1	C7		
1	IO_L05N_1	F9		
1	IO_L05P_1	G8		
1	IO_L04N_1	B6		
1	IO_L04P_1/VREF_1	C5		
1	IO_L03N_1/VRP_1	D7		
1	IO_L03P_1/VRN_1	D6		
1	IO_L02N_1	F8		
1	IO_L02P_1	F7		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
NA	GND	M5		
NA	GND	K28		
NA	GND	K3		
NA	GND	H30		
NA	GND	H1		
NA	GND	G17		
NA	GND	G14		
NA	GND	F25		
NA	GND	F6		
NA	GND	E26		
NA	GND	E19		
NA	GND	E12		
NA	GND	E5		
NA	GND	D27		
NA	GND	D4		
NA	GND	C28		
NA	GND	C21		
NA	GND	C10		
NA	GND	C3		
NA	GND	B29		
NA	GND	B2		
NA	GND	A23		
NA	GND	A8		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
0	IO_L49N_0	C23	
0	IO_L49P_0	C22	
0	IO_L50N_0	E22	
0	IO_L50P_0	E21	
0	IO_L51N_0	F21	
0	IO_L51P_0/VREF_0	F20	
0	IO_L52N_0	A24	
0	IO_L52P_0	A23	
0	IO_L53N_0	E20	
0	IO_L53P_0	E19	
0	IO_L54N_0	B22	
0	IO_L54P_0	B21	
0	IO_L67N_0	D21	
0	IO_L67P_0	D20	
0	IO_L68N_0	J20	
0	IO_L68P_0	J19	
0	IO_L69N_0	F19	
0	IO_L69P_0/VREF_0	F18	
0	IO_L70N_0	A22	
0	IO_L70P_0	A21	
0	IO_L71N_0	H19	
0	IO_L71P_0	H17	
0	IO_L72N_0	C21	
0	IO_L72P_0	C20	
0	IO_L73N_0	B20	
0	IO_L73P_0	B19	
0	IO_L74N_0	G18	
0	IO_L74P_0	G17	
0	IO_L75N_0	E18	
0	IO_L75P_0/VREF_0	D17	
0	IO_L76N_0	A20	
0	IO_L76P_0	A19	
0	IO_L77N_0	D19	
0	IO_L77P_0	D18	
0	IO_L78N_0	C19	
0	IO_L78P_0	C17	
0	IO_L91N_0/VREF_0	K18	
0	IO_L91P_0	J18	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U13	
NA	VCCINT	U19	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V19	
NA	VCCINT	W13	
NA	VCCINT	W14	
NA	VCCINT	W15	
NA	VCCINT	W16	
NA	VCCINT	W17	
NA	VCCINT	W18	
NA	VCCINT	W19	
NA	VCCINT	Y12	
NA	VCCINT	Y16	
NA	VCCINT	Y20	
NA	VCCINT	AA11	
NA	VCCINT	AA16	
NA	VCCINT	AA21	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	GND	A2	
NA	GND	A3	
NA	GND	A16	
NA	GND	A29	
NA	GND	A30	
NA	GND	B1	
NA	GND	B2	
NA	GND	B8	
NA	GND	B24	
NA	GND	B30	
NA	GND	B31	
NA	GND	C1	
NA	GND	C3	
NA	GND	C29	
NA	GND	C31	
NA	GND	D4	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	
NA	GND	AG5	