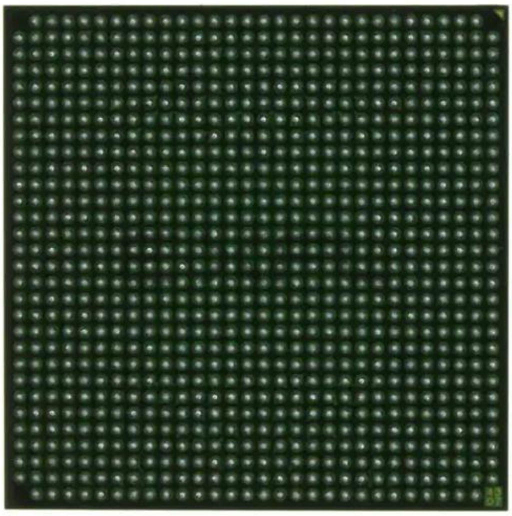

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	-
Total RAM Bits	884736
Number of I/O	528
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1500-6ffg896c

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

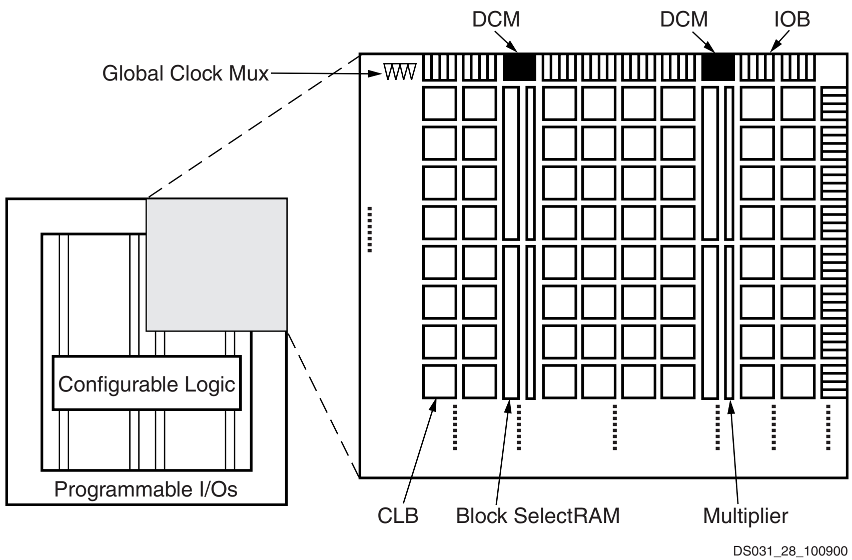

Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Shift Registers

Each function generator can also be configured as a 16-bit shift register. The write operation is synchronous with a clock input (CLK) and an optional clock enable, as shown in Figure 21. A dynamic read access is performed through the 4-bit address bus, A[3:0]. The configurable 16-bit shift register cannot be set or reset. The read is asynchronous, however the storage element or flip-flop is available to implement a synchronous read. The storage element should always be used with a constant address. For example, when building an 8-bit shift register and configuring the addresses to point to the 7th bit, the 8th bit can be the flip-flop. The overall system performance is improved by using the superior clock-to-out of the flip-flops.

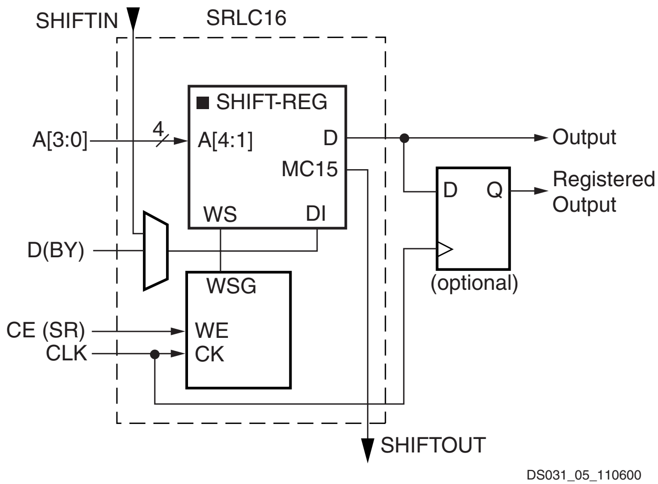

Figure 21: **Shift Register Configurations**

An additional dedicated connection between shift registers allows connecting the last bit of one shift register to the first bit of the next, without using the ordinary LUT output. (See Figure 22.) Longer shift registers can be built with dynamic access to any bit in the chain. The shift register chaining and the MUXF5, MUXF6, and MUXF7 multiplexers allow up to a 128-bit shift register with addressable access to be implemented in one CLB.

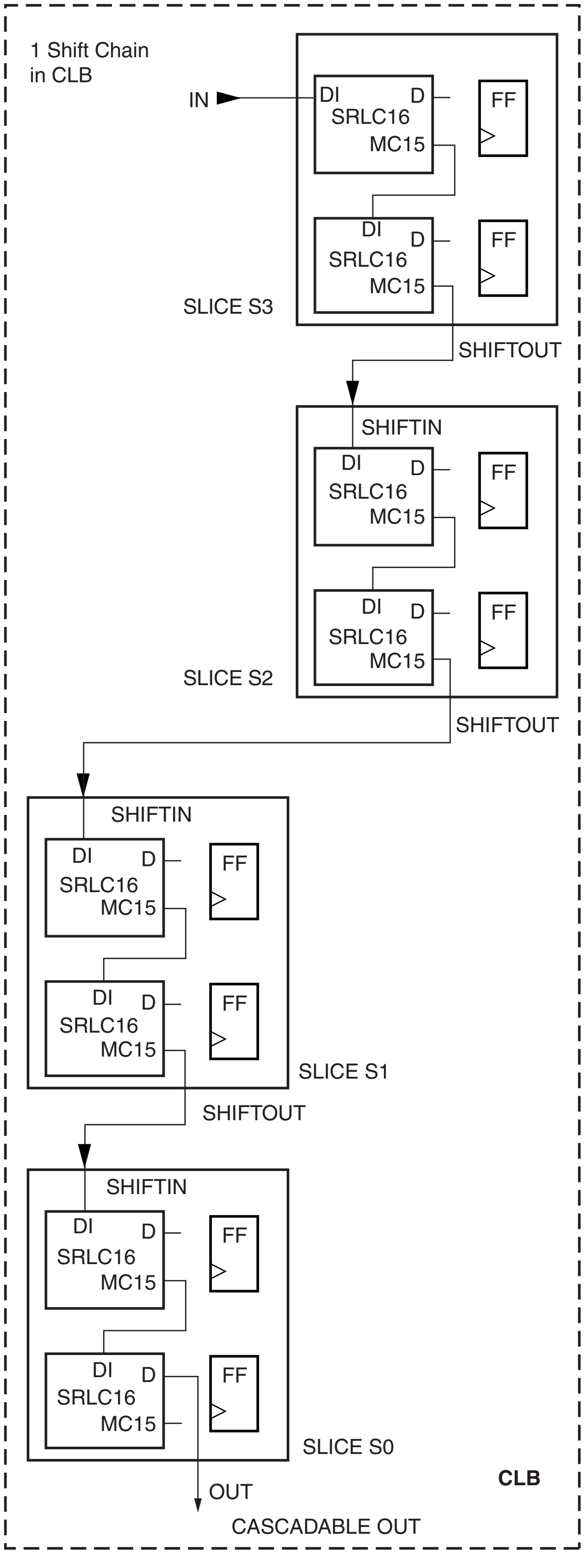

Figure 22: **Cascadable Shift Register**

Sum of Products

Each Virtex-II slice has a dedicated OR gate named ORCY, ORing together outputs from the slices carryout and the ORCY from an adjacent slice. The ORCY gate with the dedicated Sum of Products (SOP) chain are designed for implementing large, flexible SOP chains. One input of each ORCY is connected through the fast SOP chain to the output of the previous ORCY in the same slice row. The second input is connected to the output of the top MUXCY in the same slice, as shown in Figure 25.

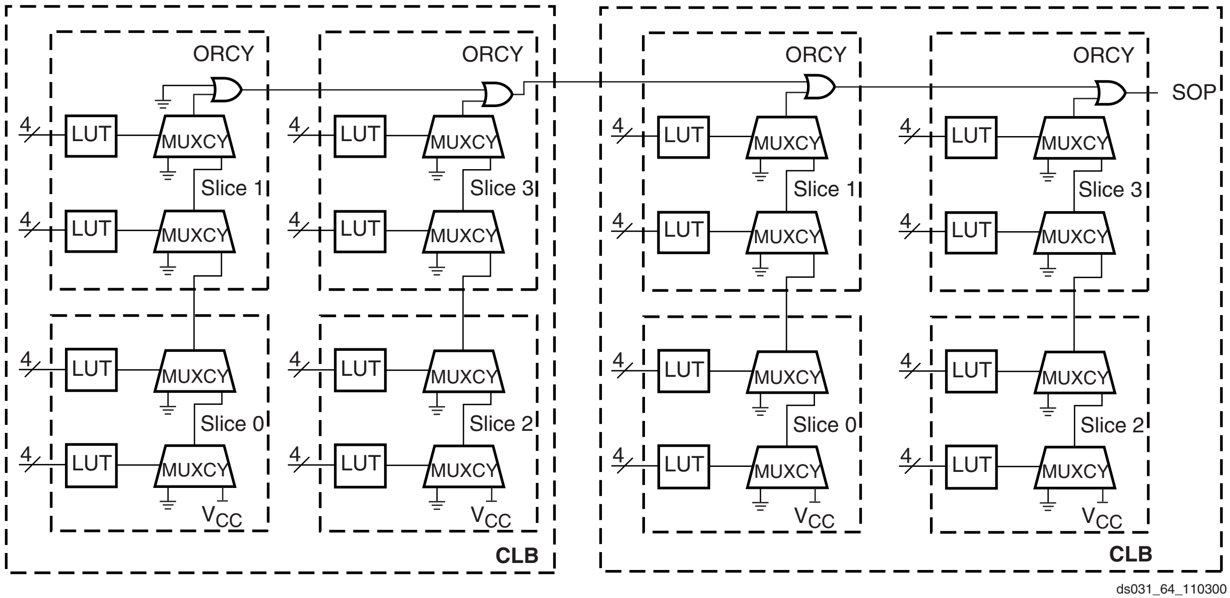

Figure 25: **Horizontal Cascade Chain**

LUTs and MUXCYs can implement large AND gates or other combinatorial logic functions. Figure 26 illustrates LUT and MUXCY resources configured as a 16-input AND gate.

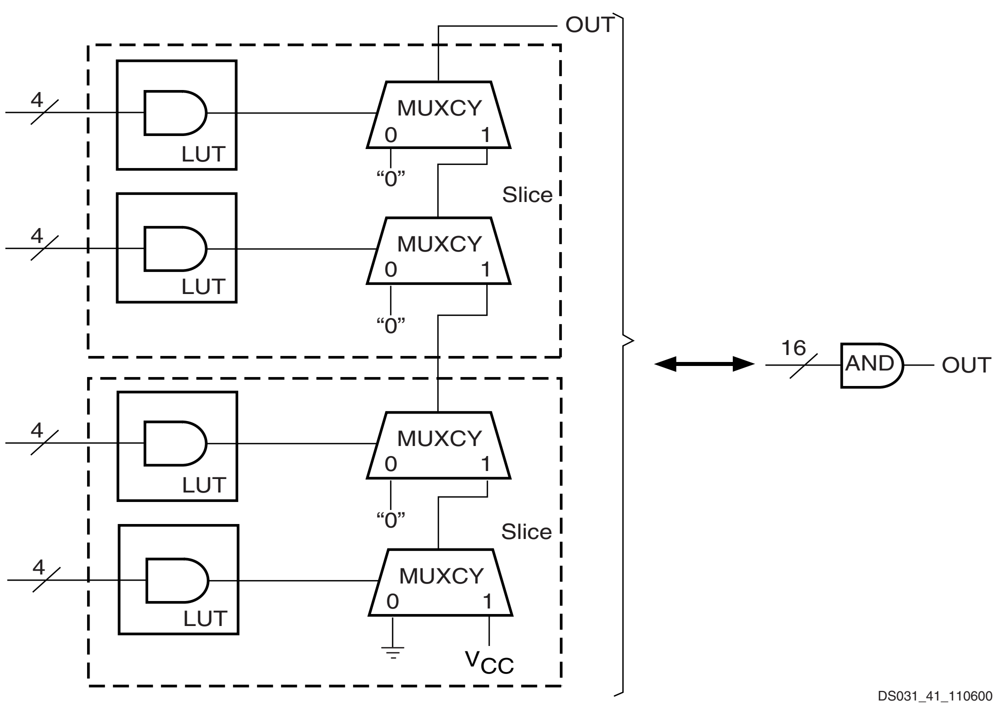

Figure 26: **Wide-Input AND Gate (16 Inputs)**

Table 13: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains[(1)]	Number of SOP Chains[(1)]
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Table 17: **IOB Output Switching Characteristics Standard Adjustments** ***(Continued)***

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
HSTL, Class II, 1.8V	HSTL_II_18	$T_{OHSTL\_II\_18}$	–0.17	–0.18	–0.20	ns
HSTL, Class III, 1.8V	HSTL_III_18	$T_{OHSTL\_III\_18}$	–0.16	–0.16	–0.18	ns
HSTL, Class IV, 1.8V	HSTL_IV_18	$T_{OHSTL\_IV\_18}$	–0.39	–0.40	–0.44	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	$T_{OSSTL18\_I}$	0.20	0.20	0.22	ns
SSTL, Class II, 1.8V	SSTL18_II	$T_{OSSTL18\_II}$	–0.05	–0.05	–0.06	ns
SSTL, Class I, 2.5V	SSTL2_I	T_{OSSTL2_I}	0.21	0.22	0.24	ns
SSTL, Class II, 2.5V	SSTL2_II	T_{OSSTL2_II}	–0.15	–0.16	–0.18	ns
SSTL, Class I, 3.3V	SSTL3_I	T_{OSSTL3_I}	0.29	0.30	0.33	ns
SSTL, Class II, 3.3V	SSTL3_II	T_{OSSTL3_II}	–0.05	–0.05	–0.05	ns
AGP-2X/AGP (Accelerated Graphics Port)	AGP	T_{OAGP}	–0.27	–0.28	–0.31	ns
LVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33	T_{OLVDCI_33}	0.74	0.77	0.84	ns
LVDCI, 2.5V	LVDCI_25	T_{OLVDCI_25}	0.78	0.80	0.88	ns
LVDCI, 1.8V	LVDCI_18	T_{OLVDCI_18}	0.84	0.87	0.95	ns
LVDCI, 1.5V	LVDCI_15	T_{OLVDCI_15}	1.82	1.88	2.06	ns
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	$T_{OLVDCI\_DV2\_33}$	0.12	0.12	0.13	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	$T_{OLVDCI\_DV2\_25}$	0.03	0.03	0.03	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	$T_{OLVDCI\_DV2\_18}$	0.42	0.43	0.48	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	$T_{OLVDCI\_DV2\_15}$	1.20	1.23	1.36	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	$T_{OHSLVDCI\_15}$	1.82	1.88	2.06	ns
HSLVDCI, 1.8V	HSLVDCI_18	$T_{OHSLVDCI\_18}$	1.05	1.08	1.24	ns
HSLVDCI, 2.5V	HSLVDCI_25	$T_{OHSLVDCI\_25}$	0.78	0.80	0.88	ns
HSLVDCI, 3.3V	HSLVDCI_33	$T_{OHSLVDCI\_33}$	0.74	0.77	0.84	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T_{OGTL_DCI}	–0.31	–0.32	–0.35	ns
GTL Plus with DCI	GTLP_DCI	T_{OGTLP_DCI}	–0.15	–0.16	–0.17	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	$T_{OHSTL\_I\_DCI}$	0.23	0.23	0.26	ns
HSTL, Class II, with DCI	HSTL_II_DCI	$T_{OHSTL\_II\_DCI}$	0.06	0.06	0.07	ns
HSTL, Class III, with DCI	HSTL_III_DCI	$T_{OHSTL\_III\_DCI}$	–0.17	–0.18	–0.20	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	$T_{OHSTL\_IV\_DCI}$	–0.46	–0.47	–0.52	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	$T_{OHSTL\_I\_DCI\_18}$	0.05	0.05	0.06	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	$T_{OHSTL\_II\_DCI\_18}$	–0.03	–0.03	–0.03	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	$T_{OHSTL\_III\_DCI\_18}$	–0.14	–0.14	–0.16	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	$T_{OHSTL\_IV\_DCI\_18}$	–0.41	–0.42	–0.47	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	$T_{OSSTL18\_I\_DCI}$	0.36	0.37	0.40	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	$T_{OSSTL18\_II\_DCI}$	0.06	0.06	0.07	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	$T_{OSSTL2\_I\_DCI}$	0.12	0.13	0.14	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	$T_{OSSTL2\_II\_DCI}$	–0.10	–0.10	–0.11	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	$T_{OSSTL3\_I\_DCI}$	0.15	0.16	0.17	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	$T_{OSSTL3\_II\_DCI}$	0.08	0.08	0.09	ns

CLB Distributed RAM Switching Characteristics

Table 22: **CLB Distributed RAM Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs (WE active) in 16 x 1 mode	$T_{SHCKO16}$	1.63	1.79	2.05	ns, Max
Clock CLK to X/Y outputs (WE active) in 32 x 1 mode	$T_{SHCKO32}$	1.97	2.17	2.49	ns, Max
Clock CLK to F5 output	$T_{SHCKOF5}$	1.77	1.94	2.23	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.53/–0.09	0.58/–0.10	0.67/–0.11	ns, Min
F/G address inputs	T_{AS}/T_{AH}	0.40/ 0.00	0.44/ 0.00	0.50/ 0.00	ns, Min
SR input (WS)	T_{WES}/T_{WEH}	0.42/–0.01	0.46/–0.01	0.53/–0.01	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{WPL}	0.57	0.63	0.72	ns, Min
Minimum clock period to meet address write cycle time	T_{WC}	1.14	1.25	1.44	ns, Min

CLB Shift Register Switching Characteristics

Table 23: **CLB Shift Register Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Sequential Delays					
Clock CLK to X/Y outputs	T_{REG}	2.31	2.54	2.92	ns, Max
Clock CLK to X/Y outputs	T_{REG32}	2.65	2.92	3.35	ns, Max
Clock CLK to XB output via MC15 LUT output	T_{REGXB}	2.23	2.46	2.82	ns, Max
Clock CLK to YB output via MC15 LUT output	T_{REGYB}	2.18	2.40	2.75	ns, Max
Clock CLK to Shiftout	T_{CKSH}	1.92	2.11	2.43	ns, Max
Clock CLK to F5 output	T_{REGF5}	2.45	2.69	3.09	ns, Max
Setup and Hold Times Before/After Clock CLK					
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}	0.53/–0.07	0.58/–0.08	0.67/–0.09	ns, Min
SR input (WS)	T_{WSS}/T_{WSH}	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
Clock CLK					
Minimum Pulse Width, High	T_{SRPH}	0.57	0.63	0.72	ns, Min
Minimum Pulse Width, Low	T_{SRPL}	0.57	0.63	0.72	ns, Min

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from "Operating junction temperature" to "Maximum junction temperature". • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word "monotonically" to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L06N_6	V6		
6	IO_L19P_6	U7		
6	IO_L19N_6	T8		
6	IO_L21P_6	AA1		
6	IO_L21N_6/VREF_6	Y2		
6	IO_L22P_6	Y1		
6	IO_L22N_6	W1		
6	IO_L24P_6	W2		
6	IO_L24N_6	V2		
6	IO_L43P_6	V4		
6	IO_L43N_6	V3		
6	IO_L45P_6	U6		
6	IO_L45N_6/VREF_6	U5		
6	IO_L46P_6	T7		
6	IO_L46N_6	T6		
6	IO_L48P_6	R8		
6	IO_L48N_6	R7		
6	IO_L49P_6	U2		
6	IO_L49N_6	U1		
6	IO_L51P_6	U4		
6	IO_L51N_6/VREF_6	U3		
6	IO_L52P_6	T1		
6	IO_L52N_6	R1		
6	IO_L54P_6	T3		
6	IO_L54N_6	T2		
6	IO_L67P_6	T5	NC	
6	IO_L67N_6	T4	NC	
6	IO_L69P_6	R6	NC	
6	IO_L69N_6/VREF_6	R5	NC	
6	IO_L70P_6	P8	NC	
6	IO_L70N_6	P7	NC	
6	IO_L72P_6	R2	NC	
6	IO_L72N_6	P1	NC	
6	IO_L73P_6	R3	NC	NC
6	IO_L73N_6	P3	NC	NC
6	IO_L91P_6	P5		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	Y5		
NA	GND	W19		
NA	GND	W6		
NA	GND	V24		
NA	GND	V18		
NA	GND	V7		
NA	GND	V1		
NA	GND	R21		
NA	GND	R4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	K21		
NA	GND	K4		
NA	GND	G24		
NA	GND	G18		
NA	GND	G7		
NA	GND	G1		
NA	GND	F19		
NA	GND	F6		
NA	GND	E20		
NA	GND	E5		
NA	GND	D21		

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L95P_6	W30	
6	IO_L95N_6	V30	
6	IO_L96P_6	V32	
6	IO_L96N_6	W32	
7	IO_L96P_7	U31	
7	IO_L96N_7	V31	
7	IO_L95P_7	T28	
7	IO_L95N_7	U28	
7	IO_L94P_7	U33	
7	IO_L94N_7	U34	
7	IO_L93P_7/VREF_7	U29	
7	IO_L93N_7	T29	
7	IO_L92P_7	U27	
7	IO_L92N_7	U26	
7	IO_L91P_7	T30	
7	IO_L91N_7	U30	
7	IO_L84P_7	R32	NC
7	IO_L84N_7	T32	NC
7	IO_L83P_7	U25	NC
7	IO_L83N_7	T25	NC
7	IO_L82P_7	R34	NC
7	IO_L82N_7	T33	NC
7	IO_L81P_7/VREF_7	N34	NC
7	IO_L81N_7	P34	NC
7	IO_L80P_7	U24	NC
7	IO_L80N_7	T24	NC
7	IO_L79P_7	R31	NC
7	IO_L79N_7	T31	NC
7	IO_L78P_7	N32	
7	IO_L78N_7	P32	
7	IO_L77P_7	T27	
7	IO_L77N_7	R27	
7	IO_L76P_7	N33	
7	IO_L76N_7	P33	
7	IO_L75P_7/VREF_7	R29	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	AE32	
NA	GND	AE3	
NA	GND	AC30	
NA	GND	AC5	
NA	GND	AA28	
NA	GND	AA21	
NA	GND	AA20	
NA	GND	AA19	
NA	GND	AA18	
NA	GND	AA17	
NA	GND	AA16	
NA	GND	AA15	
NA	GND	AA14	
NA	GND	AA7	
NA	GND	Y33	
NA	GND	Y21	
NA	GND	Y20	
NA	GND	Y19	
NA	GND	Y18	
NA	GND	Y17	
NA	GND	Y16	
NA	GND	Y15	
NA	GND	Y14	
NA	GND	Y2	
NA	GND	W26	
NA	GND	W21	
NA	GND	W20	
NA	GND	W19	
NA	GND	W18	
NA	GND	W17	
NA	GND	W16	
NA	GND	W15	
NA	GND	W14	
NA	GND	W9	
NA	GND	V21	
NA	GND	V20	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L09P_2/VREF_2	H7	NC	
2	IO_L10N_2	G3	NC	
2	IO_L10P_2	F3	NC	
2	IO_L11N_2	J8	NC	
2	IO_L11P_2	K8	NC	
2	IO_L12N_2	H5	NC	
2	IO_L12P_2	G5	NC	
2	IO_L19N_2	G1		
2	IO_L19P_2	F1		
2	IO_L20N_2	K9		
2	IO_L20P_2	L10		
2	IO_L21N_2	K7		
2	IO_L21P_2/VREF_2	J7		
2	IO_L22N_2	H2		
2	IO_L22P_2	G2		
2	IO_L23N_2	L9		
2	IO_L23P_2	M9		
2	IO_L24N_2	H4		
2	IO_L24P_2	G4		
2	IO_L25N_2	J3		
2	IO_L25P_2	H3		
2	IO_L26N_2	M10		
2	IO_L26P_2	N10		
2	IO_L27N_2	K6		
2	IO_L27P_2/VREF_2	J6		
2	IO_L28N_2	K5		
2	IO_L28P_2	J5		
2	IO_L29N_2	N11		
2	IO_L29P_2	P11		
2	IO_L30N_2	M7		
2	IO_L30P_2	L7		
2	IO_L31N_2	J1	NC	
2	IO_L31P_2	H1	NC	
2	IO_L32N_2	L8	NC	
2	IO_L32P_2	M8	NC	
2	IO_L33N_2	K4	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
7	IO_L74P_7	U31		
7	IO_L74N_7	T31		
7	IO_L73P_7	R38		
7	IO_L73N_7	T38		
7	IO_L72P_7	T33		
7	IO_L72N_7	U33		
7	IO_L71P_7	U30		
7	IO_L71N_7	T30		
7	IO_L70P_7	R37		
7	IO_L70N_7	T37		
7	IO_L69P_7/VREF_7	R36		
7	IO_L69N_7	T36		
7	IO_L68P_7	T32		
7	IO_L68N_7	R32		
7	IO_L67P_7	P39		
7	IO_L67N_7	R39		
7	IO_L60P_7	R35		
7	IO_L60N_7	T35		
7	IO_L59P_7	U28		
7	IO_L59N_7	T28		
7	IO_L58P_7	N37		
7	IO_L58N_7	P37		
7	IO_L57P_7/VREF_7	R34		
7	IO_L57N_7	T34		
7	IO_L56P_7	T29		
7	IO_L56N_7	R29		
7	IO_L55P_7	M39		
7	IO_L55N_7	N39		
7	IO_L54P_7	N36		
7	IO_L54N_7	P36		
7	IO_L53P_7	R30		
7	IO_L53N_7	P30		
7	IO_L52P_7	M38		
7	IO_L52N_7	N38		
7	IO_L51P_7/VREF_7	P33		
7	IO_L51N_7	R33		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
6	VCCO_6	AG33		
6	VCCO_6	AF38		
6	VCCO_6	AF27		
6	VCCO_6	AE31		
6	VCCO_6	AE27		
6	VCCO_6	AE26		
6	VCCO_6	AD27		
6	VCCO_6	AD26		
6	VCCO_6	AC29		
6	VCCO_6	AC27		
6	VCCO_6	AC26		
6	VCCO_6	AB37		
6	VCCO_6	AB27		
6	VCCO_6	AB26		
6	VCCO_6	AA27		
6	VCCO_6	AA26		
7	VCCO_7	W27		
7	VCCO_7	W26		
7	VCCO_7	V37		
7	VCCO_7	V27		
7	VCCO_7	V26		
7	VCCO_7	U29		
7	VCCO_7	U27		
7	VCCO_7	U26		
7	VCCO_7	T27		
7	VCCO_7	T26		
7	VCCO_7	R31		
7	VCCO_7	R27		
7	VCCO_7	R26		
7	VCCO_7	P38		
7	VCCO_7	P27		
7	VCCO_7	N33		
7	VCCO_7	L35		
NA	CCLK	AT5		
NA	PROG_B	H31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	
7	IO_L53P_7	L30	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	