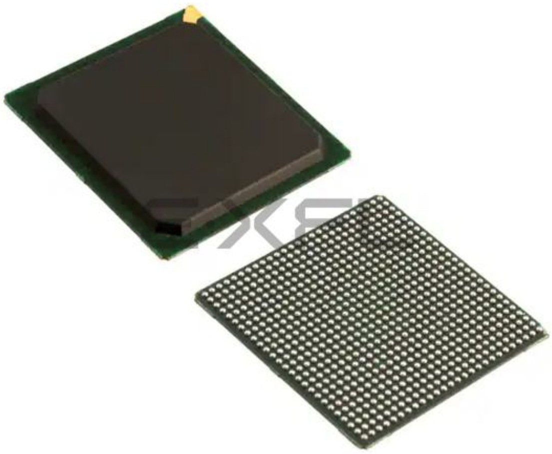

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1920
Number of Logic Elements/Cells	-
Total RAM Bits	884736
Number of I/O	392
Number of Gates	1500000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v1500-6fgg676c

Figure 13 provides examples illustrating the use of the LVDS_DCI and LVDSEXT_DCI I/O standards. For a complete list, see the **Virtex-II Platform FPGA User Guide**.

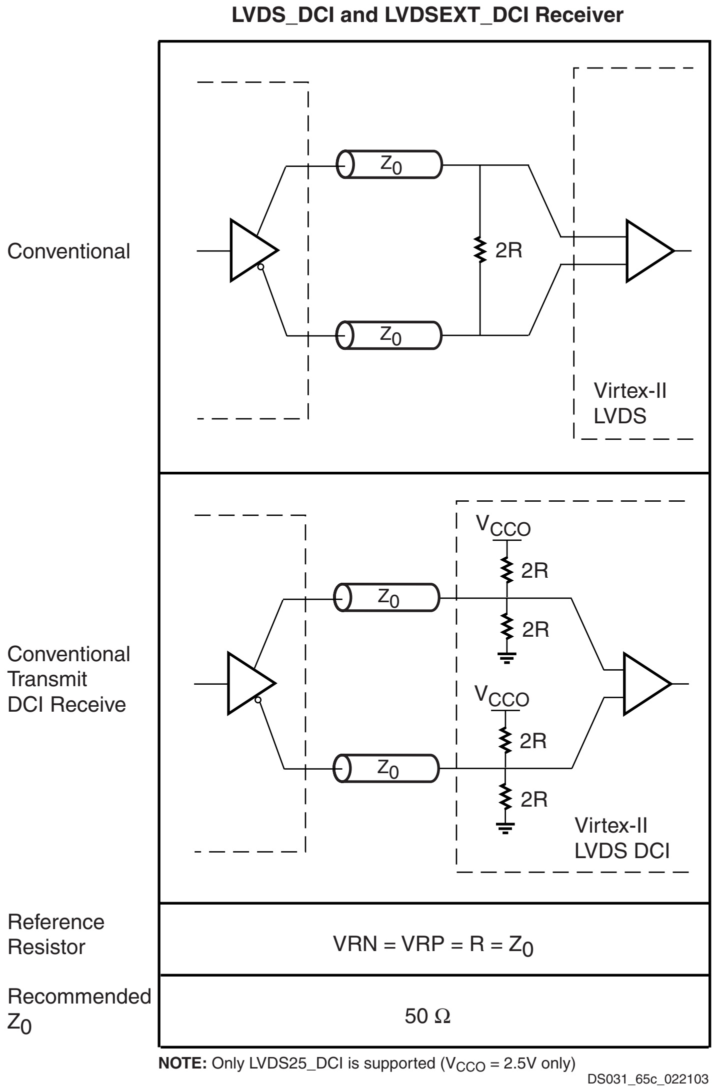

Figure 13: **LVDS DCI Usage Examples**

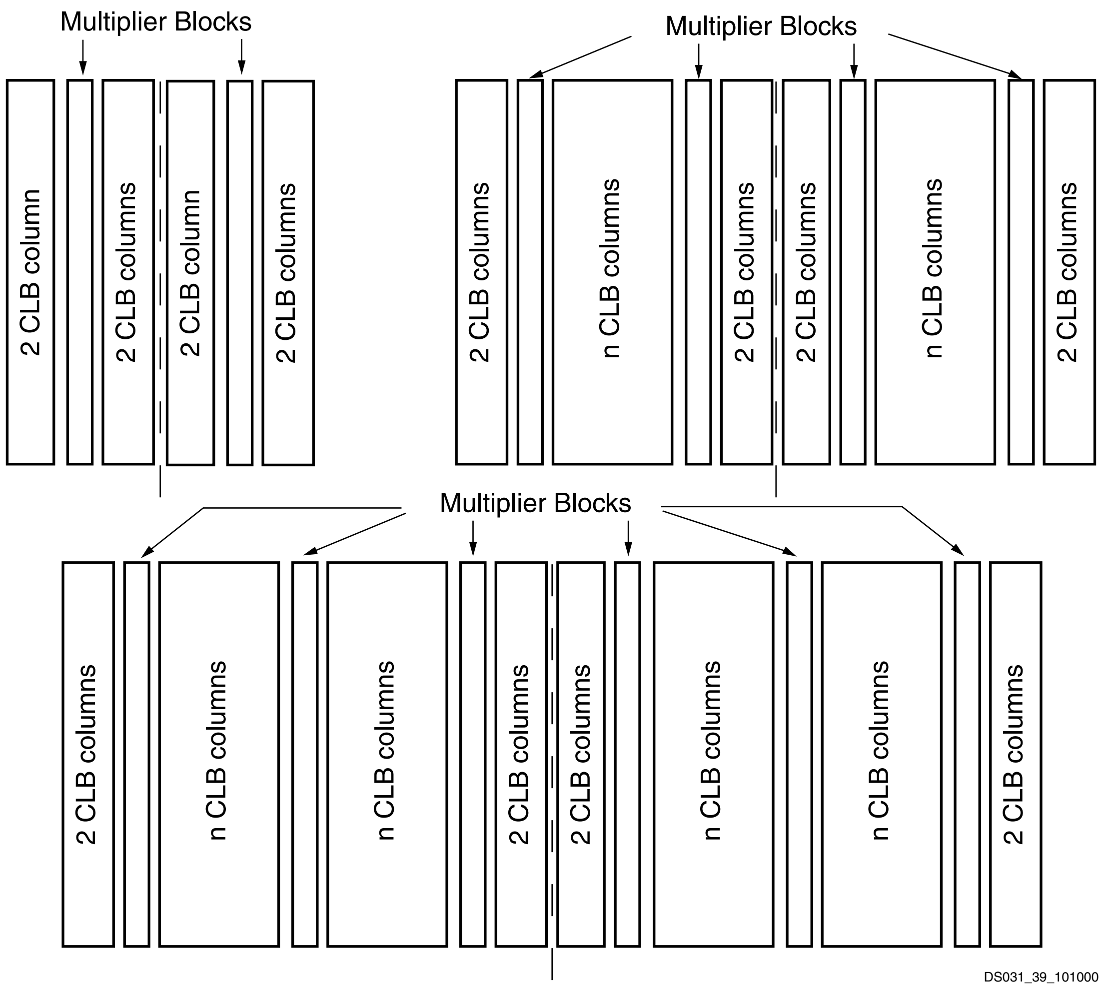

Figure 37: **Multipliers (2-column, 4-column, and 6-column)**

Global Clock Multiplexer Buffers

Virtex-II devices have 16 clock input pins that can also be used as regular user I/Os. Eight clock pads are on the top edge of the device, in the middle of the array, and eight are on the bottom edge, as illustrated in Figure 38.

The global clock multiplexer buffer represents the input to dedicated low-skew clock tree distribution in Virtex-II devices. Like the clock pads, eight global clock multiplexer buffers are on the top edge of the device and eight are on the bottom edge.

Each global clock buffer can either be driven by the clock pad to distribute a clock directly to the device, or driven by the Digital Clock Manager (DCM), discussed in Digital Clock Manager (DCM), page 29. Each global clock buffer can also be driven by local interconnects. The DCM has clock output(s) that can be connected to global clock buffer inputs, as shown in Figure 39.

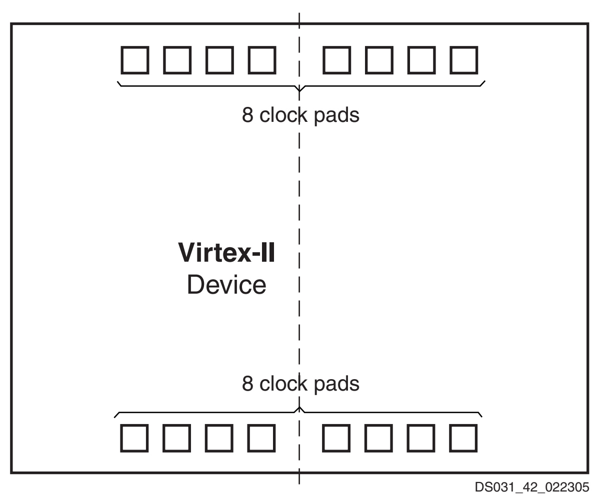

Figure 38: **Virtex-II Clock Pads**

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as Virtex-II Switching Characteristics, page 9 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	6.3	ns
32-bit Address Decoder	XC2V1000 -5	7.7	ns
64-bit Address Decoder	XC2V1000 -5	9.3	ns
4:1 MUX	XC2V1000 -5	5.7	ns
8:1 MUX	XC2V1000 -5	6.5	ns
16:1 MUX	XC2V1000 -5	6.7	ns
32:1 MUX	XC2V1000 -5	8.7	ns
Combinatorial (pad to LUT to pad)	XC2V1000 -5	5.0	ns
Memory			
Block RAM			
Pad to setup		1.6	ns
Clock to Pad		9.5	ns
Distributed RAM			
Pad to setup	XC2V1000 -5	2.7	ns
Clock to Pad	XC2V1000 -5	5.1 (no clk skew)	ns

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: **Register-to-Register Performance**

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	398	MHz
32-bit Address Decoder	XC2V1000 -5	291	MHz
64-bit Address Decoder	XC2V1000 -5	274	MHz
4:1 MUX	XC2V1000 -5	563	MHz
8:1 MUX	XC2V1000 -5	454	MHz
16:1 MUX	XC2V1000 -5	414	MHz
32:1 MUX	XC2V1000 -5	323	MHz
Register to LUT to Register	XC2V1000 -5	613	MHz

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-II source-synchronous transmitter and receiver data-valid windows.

Table 45: **Duty Cycle Distortion and Clock-Tree Skew**

Description	Symbol	Device	Speed Grade -6	Speed Grade -5	Speed Grade -4	Units
Duty Cycle Distortion(1)	T_{DCD_CLK0}	All	140	140	140	ps
	T_{DCD_CLK180}	All	50	50	50	ps
Clock Tree Skew(2)	T_{CKSKEW}	XC2V40	50	50	60	ps
		XC2V80	50	50	60	ps
		XC2V250	50	50	60	ps
		XC2V500	50	50	60	ps
		XC2V1000	80	80	90	ps
		XC2V1500	80	80	90	ps
		XC2V2000	100	100	110	ps
		XC2V3000	100	100	110	ps
		XC2V4000	400	400	450	ps
		XC2V6000	500	500	550	ps
		XC2V8000		600	650	ps

Notes:
1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
   T_{DCD_CLK0} applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O.
   T_{DCD_CLK180} applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 46: **Package Skew**

Description	Symbol	Device/Package	Value	Units
Package Skew(1)	$T_{PKGSKEW}$	XC2V1000 / FF896	130	ps
		XC2V3000 / FF1152	115	ps
		XC2V3000 / BF957	130	ps
		XC2V4000 / FF1152	130	ps
		XC2V4000 / FF1517	200	ps
		XC2V4000 / BF957	140	ps
		XC2V6000 / FF1152	90	ps
		XC2V6000 / FF1517	105	ps
		XC2V6000 / BF957	105	ps

Notes:
1. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball (7.1ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Source Synchronous Timing Budgets

This section describes how to use the parameters provided in the Source-Synchronous Switching Characteristics section to develop system-specific timing budgets. The following analysis provides information necessary for determining Virtex-II contributions to an overall system timing analysis; no assumptions are made about the effects of Inter-Symbol Interference or PCB skew.

Virtex-II Transmitter Data-Valid Window (T_X)

T_X is the minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

T_X = Data Period - [Jitter(1) + Duty Cycle Distortion(2) + TCKSKEW(3) + TPKGSKEW(4)]

Notes:
1. Jitter values and accumulation methodology to be provided in a future release of this document. The absolute period jitter values found in the DCM Timing Parameters section of the particular DCM output clock used to clock the IOB FF can be used for a best case analysis.
2. This value depends on the clocking methodology used. See Note1 for Table 45.
3. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
4. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Virtex-II Receiver Data-Valid Window (R_X)

R_X is the required minimum aggregate valid data period for a source-synchronous data bus at the pins of the device and is calculated as follows:

R_X = [TSAMP(1) + TCKSKEW(2) + TPKGSKEW(3)]

Notes:
1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter in a quiet system
   - Worst-case duty-cycle distortion
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.
2. This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
3. These values represent the worst-case skew between any two balls of the package: shortest flight time to longest flight time from Pad to Ball.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	• The data sheet was divided into four modules (per the current style standard). • Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Table 18, “Delay Measurement Methodology”
04/23/01	1.5	• Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. • Added T_{REG32} symbol to Table 23. • Skipped v1.4 to sync with other modules. Reverted to traditional double-column format.

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: **Virtex-II Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = P/N** for the positive and negative sides of the differential pair. **#** indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled "**IO_LXXY_#/ZZZ**", where **ZZZ** can be one of the following pins: Per Bank - **VRP, VRN,** or **VREF** Globally - **GCLKX(S/P), BUSY/DOUT, INIT_B, D0/DIN – D7, RDWR_B,** or **CS_B**
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	• *In* SelectMAP *mode,* D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	• *In* SelectMAP *mode,* BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. • *In bit-serial modes,* DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V_{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins(1)		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
5	IO_L70N_5	W11		
5	IO_L70P_5	Y10		
5	IO_L69N_5/VREF_5	Y11		
5	IO_L69P_5	AA11		
5	IO_L67N_5	AF9		
5	IO_L67P_5	AF8		
5	IO_L54N_5	AE9		
5	IO_L54P_5	AD9		
5	IO_L52N_5	AB10		
5	IO_L52P_5	AA10		
5	IO_L51N_5/VREF_5	AD10		
5	IO_L51P_5	AC10		
5	IO_L49N_5	AE8		
5	IO_L49P_5	AF7		
5	IO_L28N_5	AD8	NC	NC
5	IO_L28P_5	AC8	NC	NC
5	IO_L27N_5/VREF_5	AB9	NC	NC
5	IO_L27P_5	AC9	NC	NC
5	IO_L25N_5	AA9	NC	NC
5	IO_L25P_5	Y9	NC	NC
5	IO_L24N_5	AF6		
5	IO_L24P_5	AE6		
5	IO_L22N_5	AB8		
5	IO_L22P_5	AA8		
5	IO_L21N_5/VREF_5	AC7		
5	IO_L21P_5	AD7		
5	IO_L19N_5	AF5		
5	IO_L19P_5	AE5		
5	IO_L06N_5	AF4		
5	IO_L06P_5	AE4		
5	IO_L05N_5/VRP_5	AF3		
5	IO_L05P_5/VRN_5	AE3		
5	IO_L04N_5	Y8		
5	IO_L04P_5/VREF_5	Y7		
5	IO_L03N_5/D4/ALT_VRP_5	AB7		
5	IO_L03P_5/D5/ALT_VRN_5	AA7		
5	IO_L02N_5/D6	AD6		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	DONE	AD22		
NA	M0	AD4		
NA	M1	AA5		
NA	M2	AD5		
NA	HSWAP_EN	D5		
NA	TCK	E21		
NA	TDI	F5		
NA	TDO	F22		
NA	TMS	D22		
NA	PWRDWN_B	AD23		
NA	DXN	F7		
NA	DXP	C5		
NA	VBATT	C23		
NA	RSVD	C22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC24		
NA	VCCAUX	AC3		
NA	VCCAUX	P24		
NA	VCCAUX	N3		
NA	VCCAUX	D24		
NA	VCCAUX	D3		
NA	VCCAUX	C14		
NA	VCCINT	W19		
NA	VCCINT	W8		
NA	VCCINT	V18		
NA	VCCINT	V17		
NA	VCCINT	V10		
NA	VCCINT	V9		
NA	VCCINT	U18		
NA	VCCINT	U9		
NA	VCCINT	K18		
NA	VCCINT	K9		
NA	VCCINT	J18		
NA	VCCINT	J17		
NA	VCCINT	J10		
NA	VCCINT	J9		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L91P_4	AB14		
4	IO_L92N_4	V14		
4	IO_L92P_4	Y14		
4	IO_L93N_4	AB13		
4	IO_L93P_4	AC13		
4	IO_L94N_4/VREF_4	Y13		
4	IO_L94P_4	AA13		
4	IO_L95N_4/GCLK3S	V13		
4	IO_L95P_4/GCLK2P	W13		
4	IO_L96N_4/GCLK1S	U14		
4	IO_L96P_4/GCLK0P	U13		
5	IO_L96N_5/GCLK7S	AD12		
5	IO_L96P_5/GCLK6P	AD11		
5	IO_L95N_5/GCLK5S	AC12		
5	IO_L95P_5/GCLK4P	AB12		
5	IO_L94N_5	AA12		
5	IO_L94P_5/VREF_5	Y12		
5	IO_L93N_5	W12		
5	IO_L93P_5	V12		
5	IO_L92N_5	U12		
5	IO_L92P_5	U11		
5	IO_L91N_5	AB11		
5	IO_L91P_5/VREF_5	AA11		
5	IO_L73N_5	Y11	NC	NC
5	IO_L73P_5	V11	NC	NC
5	IO_L72N_5	AD10	NC	
5	IO_L72P_5	AD9	NC	
5	IO_L70N_5	AC10	NC	
5	IO_L70P_5	AB10	NC	
5	IO_L69N_5/VREF_5	Y10	NC	
5	IO_L69P_5	W10	NC	
5	IO_L67N_5	V10	NC	
5	IO_L67P_5	U10	NC	
5	IO_L54N_5	AC9		
5	IO_L54P_5	AB9		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L20P_6	AE26		
6	IO_L20N_6	AD26		
6	IO_L21P_6	AG30		
6	IO_L21N_6/VREF_6	AF30		
6	IO_L22P_6	AD25		
6	IO_L22N_6	AC25		
6	IO_L23P_6	AE28		
6	IO_L23N_6	AD28		
6	IO_L24P_6	AD29		
6	IO_L24N_6	AE29		
6	IO_L43P_6	AC24		
6	IO_L43N_6	AB24		
6	IO_L44P_6	AD27		
6	IO_L44N_6	AC27		
6	IO_L45P_6	AC26		
6	IO_L45N_6/VREF_6	AB26		
6	IO_L46P_6	AA23		
6	IO_L46N_6	Y23		
6	IO_L47P_6	AC28		
6	IO_L47N_6	AB28		
6	IO_L48P_6	AD30		
6	IO_L48N_6	AE30		
6	IO_L49P_6	AB25		
6	IO_L49N_6	AA25		
6	IO_L50P_6	AA24		
6	IO_L50N_6	Y24		
6	IO_L51P_6	AC29		
6	IO_L51N_6/VREF_6	AB30		
6	IO_L52P_6	Y25		
6	IO_L52N_6	W25		
6	IO_L53P_6	AB27		
6	IO_L53N_6	AA27		
6	IO_L54P_6	AA29		
6	IO_L54N_6	AB29		
6	IO_L67P_6	W23	NC	
6	IO_L67N_6	V23	NC	
6	IO_L68P_6	AA26	NC	

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L04N_7	D29		
7	IO_L03P_7/VREF_7	E28		
7	IO_L03N_7	D28		
7	IO_L02P_7/VRN_7	H23		
7	IO_L02N_7/VRP_7	G23		
7	IO_L01P_7	B30		
7	IO_L01N_7	C30		
0	VCCO_0	K20		
0	VCCO_0	K19		
0	VCCO_0	K18		
0	VCCO_0	K17		
0	VCCO_0	K16		
0	VCCO_0	J21		
0	VCCO_0	J20		
0	VCCO_0	J19		
0	VCCO_0	J18		
0	VCCO_0	C18		
0	VCCO_0	B26		
1	VCCO_1	K15		
1	VCCO_1	K14		
1	VCCO_1	K13		
1	VCCO_1	K12		
1	VCCO_1	K11		
1	VCCO_1	J13		
1	VCCO_1	J12		
1	VCCO_1	J11		
1	VCCO_1	J10		
1	VCCO_1	C13		
1	VCCO_1	B5		
2	VCCO_2	R10		
2	VCCO_2	P10		
2	VCCO_2	N10		
2	VCCO_2	N9		
2	VCCO_2	N3		
2	VCCO_2	M10		
2	VCCO_2	M9		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
2	IO_L51N_2	L6	
2	IO_L51P_2/VREF_2	M6	
2	IO_L52N_2	M3	
2	IO_L52P_2	L3	
2	IO_L53N_2	L4	
2	IO_L53P_2	K4	
2	IO_L54N_2	N4	
2	IO_L54P_2	M4	
2	IO_L67N_2	M2	
2	IO_L67P_2	L2	
2	IO_L68N_2	N8	
2	IO_L68P_2	P8	
2	IO_L69N_2	N6	
2	IO_L69P_2/VREF_2	P6	
2	IO_L70N_2	P5	
2	IO_L70P_2	N5	
2	IO_L71N_2	P10	
2	IO_L71P_2	R10	
2	IO_L72N_2	P3	
2	IO_L72P_2	N3	
2	IO_L73N_2	M1	
2	IO_L73P_2	L1	
2	IO_L74N_2	P9	
2	IO_L74P_2	R9	
2	IO_L75N_2	P2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	R4	
2	IO_L76P_2	P4	
2	IO_L77N_2	R8	
2	IO_L77P_2	T8	
2	IO_L78N_2	T3	
2	IO_L78P_2	R3	
2	IO_L79N_2	P1	NC
2	IO_L79P_2	N1	NC
2	IO_L80N_2	T11	NC
2	IO_L80P_2	U11	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L75N_7	R28	
7	IO_L74P_7	R26	
7	IO_L74N_7	P26	
7	IO_L73P_7	N31	
7	IO_L73N_7	P31	
7	IO_L72P_7	N30	
7	IO_L72N_7	P30	
7	IO_L71P_7	R25	
7	IO_L71N_7	P25	
7	IO_L70P_7	L34	
7	IO_L70N_7	M34	
7	IO_L69P_7/VREF_7	P29	
7	IO_L69N_7	N29	
7	IO_L68P_7	P27	
7	IO_L68N_7	N27	
7	IO_L67P_7	L32	
7	IO_L67N_7	M32	
7	IO_L54P_7	L31	
7	IO_L54N_7	M31	
7	IO_L53P_7	K29	
7	IO_L53N_7	L30	
7	IO_L52P_7	L33	
7	IO_L52N_7	M33	
7	IO_L51P_7/VREF_7	M29	
7	IO_L51N_7	L29	
7	IO_L50P_7	M28	
7	IO_L50N_7	N28	
7	IO_L49P_7	K30	
7	IO_L49N_7	K31	
7	IO_L48P_7	H32	
7	IO_L48N_7	J32	
7	IO_L47P_7	N26	
7	IO_L47N_7	M26	
7	IO_L46P_7	J33	
7	IO_L46N_7	K33	
7	IO_L45P_7/VREF_7	H33	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	AE32	
NA	GND	AE3	
NA	GND	AC30	
NA	GND	AC5	
NA	GND	AA28	
NA	GND	AA21	
NA	GND	AA20	
NA	GND	AA19	
NA	GND	AA18	
NA	GND	AA17	
NA	GND	AA16	
NA	GND	AA15	
NA	GND	AA14	
NA	GND	AA7	
NA	GND	Y33	
NA	GND	Y21	
NA	GND	Y20	
NA	GND	Y19	
NA	GND	Y18	
NA	GND	Y17	
NA	GND	Y16	
NA	GND	Y15	
NA	GND	Y14	
NA	GND	Y2	
NA	GND	W26	
NA	GND	W21	
NA	GND	W20	
NA	GND	W19	
NA	GND	W18	
NA	GND	W17	
NA	GND	W16	
NA	GND	W15	
NA	GND	W14	
NA	GND	W9	
NA	GND	V21	
NA	GND	V20	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L58N_3	AD5		
3	IO_L58P_3	AE5		
3	IO_L57N_3/VREF_3	AE11		
3	IO_L57P_3	AD11		
3	IO_L56N_3	AG1		
3	IO_L56P_3	AH1		
3	IO_L55N_3	AD6		
3	IO_L55P_3	AE6		
3	IO_L54N_3	AF10		
3	IO_L54P_3	AE10		
3	IO_L53N_3	AG2		
3	IO_L53P_3	AH2		
3	IO_L52N_3	AF4		
3	IO_L52P_3	AG4		
3	IO_L51N_3/VREF_3	AG8		
3	IO_L51P_3	AF8		
3	IO_L50N_3	AH3		
3	IO_L50P_3	AJ3		
3	IO_L49N_3	AE7		
3	IO_L49P_3	AF7		
3	IO_L48N_3	AG9		
3	IO_L48P_3	AF9		
3	IO_L47N_3	AF6		
3	IO_L47P_3	AG6		
3	IO_L46N_3	AG5		
3	IO_L46P_3	AH5		
3	IO_L45N_3/VREF_3	AF12		
3	IO_L45P_3	AE12		
3	IO_L44N_3	AJ1		
3	IO_L44P_3	AK1		
3	IO_L43N_3	AH4		
3	IO_L43P_3	AJ4		
3	IO_L36N_3	AG11	NC	
3	IO_L36P_3	AF11	NC	
3	IO_L35N_3	AK2	NC	
3	IO_L35P_3	AL2	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	DONE	AP7		
NA	M0	AN32		
NA	M1	AP33		
NA	M2	AT35		
NA	HSWAP_EN	E34		
NA	TCK	G8		
NA	TDI	D35		
NA	TDO	E6		
NA	TMS	F7		
NA	PWRDWN_B	AN8		
NA	DXN	G32		
NA	DXP	F33		
NA	VBATT	D5		
NA	RSVD	H9		
NA	VCCAUX	AV20		
NA	VCCAUX	AT37		
NA	VCCAUX	AT3		
NA	VCCAUX	Y38		
NA	VCCAUX	Y2		
NA	VCCAUX	D37		
NA	VCCAUX	D3		
NA	VCCAUX	B20		
NA	VCCINT	AG27		
NA	VCCINT	AG20		
NA	VCCINT	AG13		
NA	VCCINT	AF26		
NA	VCCINT	AF20		
NA	VCCINT	AF14		
NA	VCCINT	AE25		
NA	VCCINT	AE24		
NA	VCCINT	AE23		
NA	VCCINT	AE22		
NA	VCCINT	AE21		
NA	VCCINT	AE20		
NA	VCCINT	AE19		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
2	IO_L70N_2	K1	
2	IO_L70P_2	L1	
2	IO_L71N_2	N9	
2	IO_L71P_2	P9	
2	IO_L72N_2	N5	
2	IO_L72P_2	P5	
2	IO_L73N_2	M3	
2	IO_L73P_2	N3	
2	IO_L74N_2	R8	
2	IO_L74P_2	R9	
2	IO_L75N_2	M2	
2	IO_L75P_2/VREF_2	N2	
2	IO_L76N_2	M1	
2	IO_L76P_2	N1	
2	IO_L77N_2	P7	
2	IO_L77P_2	R7	
2	IO_L78N_2	N4	
2	IO_L78P_2	P4	
2	IO_L91N_2	T8	
2	IO_L91P_2	T9	
2	IO_L92N_2	P6	
2	IO_L92P_2	R6	
2	IO_L93N_2	P2	
2	IO_L93P_2/VREF_2	R2	
2	IO_L94N_2	R5	
2	IO_L94P_2	T5	
2	IO_L95N_2	P1	
2	IO_L95P_2	R1	
2	IO_L96N_2	R4	
2	IO_L96P_2	R3	
3	IO_L96N_3	T6	
3	IO_L96P_3	U5	
3	IO_L95N_3	U6	
3	IO_L95P_3	V6	
3	IO_L94N_3	T3	
3	IO_L94P_3	U3	
3	IO_L93N_3/VREF_3	U1	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U13	
NA	VCCINT	U19	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V19	
NA	VCCINT	W13	
NA	VCCINT	W14	
NA	VCCINT	W15	
NA	VCCINT	W16	
NA	VCCINT	W17	
NA	VCCINT	W18	
NA	VCCINT	W19	
NA	VCCINT	Y12	
NA	VCCINT	Y16	
NA	VCCINT	Y20	
NA	VCCINT	AA11	
NA	VCCINT	AA16	
NA	VCCINT	AA21	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	GND	A2	
NA	GND	A3	
NA	GND	A16	
NA	GND	A29	
NA	GND	A30	
NA	GND	B1	
NA	GND	B2	
NA	GND	B8	
NA	GND	B24	
NA	GND	B30	
NA	GND	B31	
NA	GND	C1	
NA	GND	C3	
NA	GND	C29	
NA	GND	C31	
NA	GND	D4	