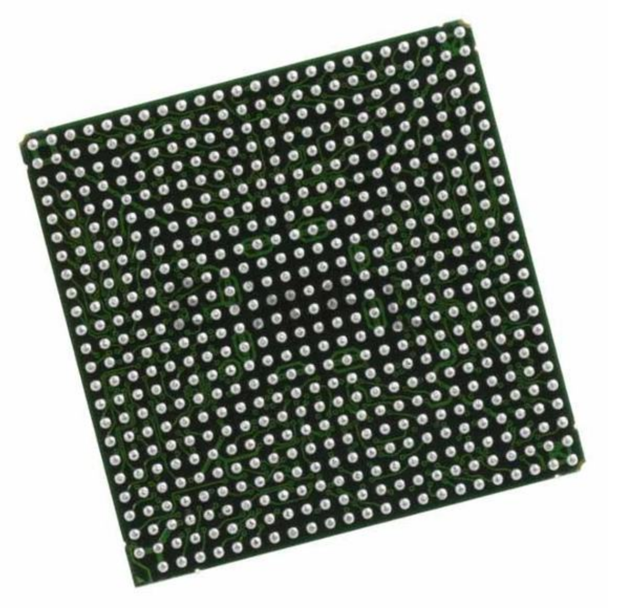
AMD Xilinx - XC2V2000-4BGG575C Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	2688
Number of Logic Elements/Cells	-
Total RAM Bits	1032192
Number of I/O	408
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v2000-4bgg575c

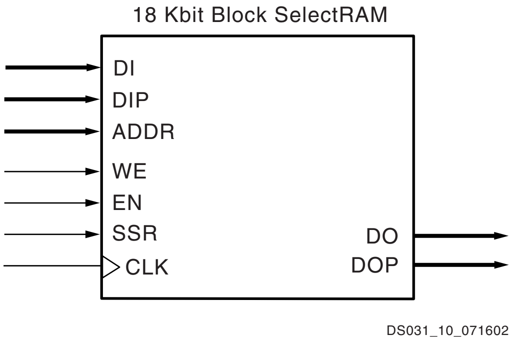


Figure 29: **18 Kbit Block SelectRAM Memory in Single-Port Mode**

Dual-Port Configuration

As a dual-port RAM, each port of block SelectRAM has access to a common 18 Kbit memory resource. These are fully synchronous ports with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

Table 15 illustrates the different configurations available on ports A and B.

If both ports are configured in either 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations, the 18 Kbit block is accessible from port A or B. If both ports are configured in either 16K x 1-bit, 8K x 2-bit. or 4K x 4-bit configurations, the 16 K-bit block is accessible from Port A or Port B. All other configurations result in one port having access to an 18 Kbit memory block and the other port having access to a 16 K-bit subset of the memory block equal to 16 Kbits.

Table 15: **Dual-Port Mode Configurations**

Port A	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1	16K x 1
Port B	16K x 1	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36
Port A	8K x 2	8K x 2	8K x 2	8K x 2	8K x 2	
Port B	8K x 2	4K x 4	2K x 9	1K x 18	512 x 36	
Port A	4K x 4	4K x 4	4K x 4	4K x 4		
Port B	4K x 4	2K x 9	1K x 18	512 x 36		
Port A	2K x 9	2K x 9	2K x 9			
Port B	2K x 9	1K x 18	512 x 36			
Port A	1K x 18	1K x 18				
Port B	1K x 18	512 x 36				
Port A	512 x 36					
Port B	512 x 36					

Each block SelectRAM cell is a fully synchronous memory, as illustrated in Figure 30. The two ports have independent inputs and outputs and are independently clocked.

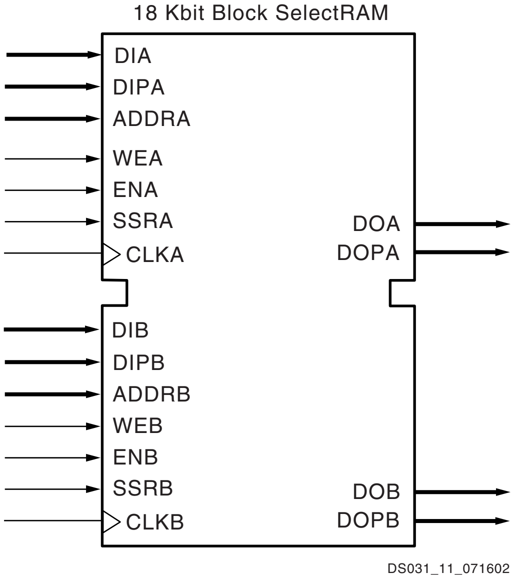


Figure 30: **18 Kbit Block SelectRAM in Dual-Port Mode**

Port Aspect Ratios

Table 16 shows the depth and the width aspect ratios for the 18 Kbit block SelectRAM. Virtex-II block SelectRAM also includes dedicated routing resources to provide an efficient interface with CLBs, block SelectRAM, and multipliers.

Table 16: **18** Kbit **Block SelectRAM Port Aspect Ratio**

Width	Depth	Address Bus	Data Bus	Parity Bus
1	16,384	ADDR[13:0]	DATA[0]	N/A
2	8,192	ADDR[12:0]	DATA[1:0]	N/A
4	4,096	ADDR[11:0]	DATA[3:0]	N/A
9	2,048	ADDR[10:0]	DATA[7:0]	Parity[0]
18	1,024	ADDR[9:0]	DATA[15:0]	Parity[1:0]
36	512	ADDR[8:0]	DATA[31:0]	Parity[3:0]

Read/Write Operations

The Virtex-II block SelectRAM read operation is fully synchronous. An address is presented, and the read operation is enabled by control signals WEA and WEB in addition to ENA or ENB. Then, depending on clock polarity, a rising or falling clock edge causes the stored data to be loaded into output registers.

The write operation is also fully synchronous. Data and address are presented, and the write operation is enabled by control signals WEA or WEB in addition to ENA or ENB. Then, again depending on the clock input mode, a rising or falling clock edge causes the data to be loaded into the memory cell addressed.

A write operation performs a simultaneous read operation. Three different options are available, selected by configuration:

1. **"WRITE_FIRST"**

   The "WRITE_FIRST" option is a transparent mode. The same clock edge that writes the data input (DI) into the memory also transfers DI into the output registers DO as shown in Figure 31.

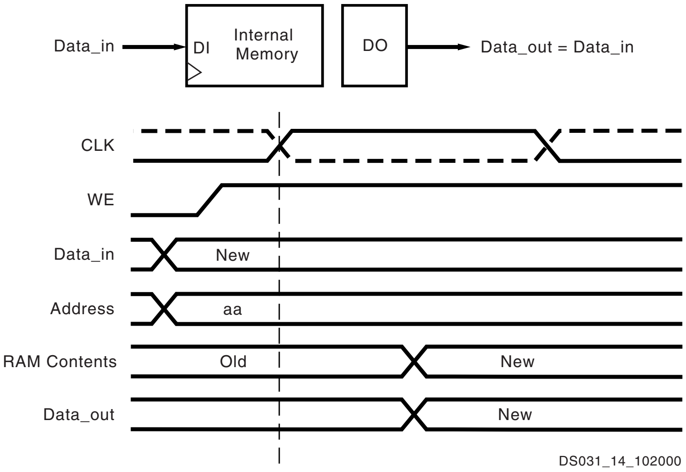


Figure 31: **WRITE_FIRST Mode**

2. **"READ_FIRST"**

   The "READ_FIRST" option is a read-before-write mode.

   The same clock edge that writes data input (DI) into the memory also transfers the prior content of the memory cell addressed into the data output registers DO, as shown in Figure 32.

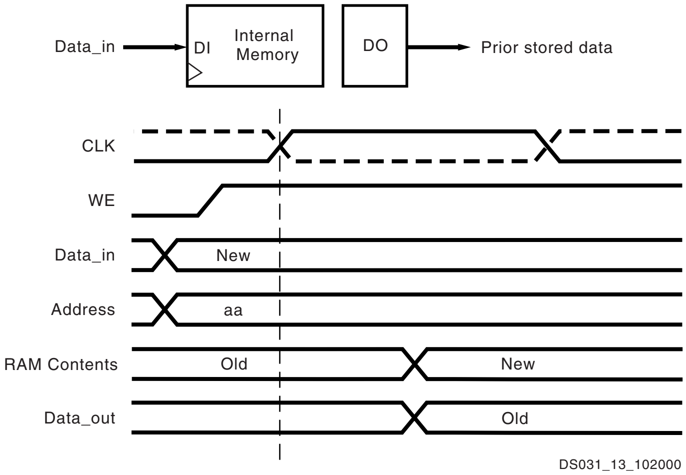


Figure 32: **READ_FIRST Mode**

3. “NO_CHANGE”

The “NO_CHANGE” option maintains the content of the output registers, regardless of the write operation. The clock edge during the write mode has no effect on the content of the data output register DO. When the port is configured as “NO_CHANGE”, only a read operation loads a new value in the output register DO, as shown in Figure 33.

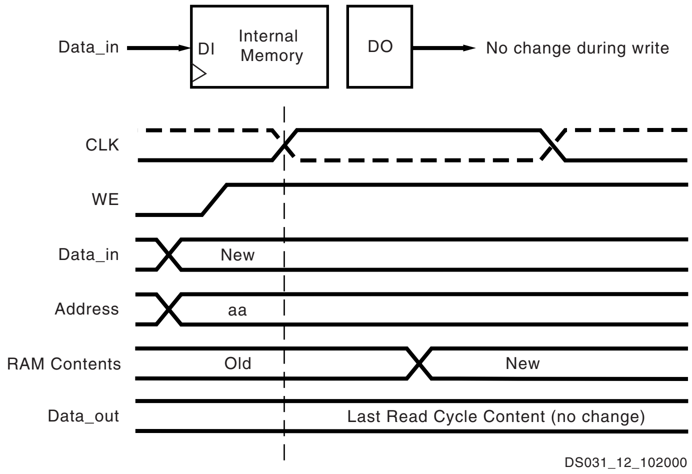


Figure 33: **NO_CHANGE Mode**

Control Pins and Attributes

Virtex-II SelectRAM memory has two independent ports with the control signals described in Table 17. All control inputs including the clock have an optional inversion.

Table 17: **Control Functions**

Control Signal	Function
CLK	Read and Write Clock
EN	Enable affects Read, Write, Set, Reset
WE	Write Enable
SSR	Set DO register to SRVAL (attribute)

Initial memory content is determined by the INIT_xx attributes. Separate attributes determine the output register value after device configuration (INIT) and SSR is asserted (SRVAL). Both attributes (INIT_B and SRVAL) are available for each port when a block SelectRAM resource is configured as dual-port RAM.

Locations

Virtex-II SelectRAM memory blocks are located in either four or six columns. The number of blocks per column depends of the device array size and is equivalent to the number of CLBs in a column divided by four. Column locations are shown in Table 18.

Table 18: **SelectRAM Memory Floor Plan**

Device	Columns	SelectRAM Blocks	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in IOB Output Switching Characteristics Standard Adjustments, page 14.

Table 16: **IOB Output Switching Characteristics**

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}	1.43	1.51	1.74	ns, Max
O input to Pad via transparent latch	T_{IOOLP}	1.72	1.83	2.11	ns, Max
3-State Delays					
T input to Pad high-impedance(1)	T_{IOTHZ}	0.51	0.56	0.64	ns, Max
T input to valid data on Pad	T_{IOTP}	1.38	1.45	1.67	ns, Max
T input to Pad high-impedance via transparent latch(1)	$T_{IOTLPHZ}$	0.80	0.88	1.01	ns, Max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.67	1.77	2.04	ns, Max
GTS to Pad high impedance(1)	T_{GTS}	4.73	5.20	5.98	ns, Max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}	1.76	1.87	2.15	ns, Max
Clock CLK to Pad high-impedance (synchronous)(1)	T_{IOCKHZ}	0.95	1.04	1.20	ns, Max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.82	1.94	2.22	ns, Max
Setup and Hold Times Before/After Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}	0.31/–0.08	0.34/–0.09	0.39/–0.11	ns, Min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
3–State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.28/–0.06	0.31/–0.07	0.35/–0.08	ns, Min
3–State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.19/–0.06	0.21/–0.07	0.24/–0.08	ns, Min
3–State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.27/–0.05	0.30/–0.06	0.34/–0.07	ns, Min
Set/Reset Delays					
Minimum Pulse Width, SR input (asynchronous)	T_{RPW}	0.61	0.67	0.77	ns, Min
SR input to Pad (asynchronous)	T_{IOSRP}	2.41	2.59	2.98	ns, Max
SR input to Pad high-impedance (asynchronous)(1)	T_{IOSRHZ}	1.52	1.67	1.92	ns, Max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.39	2.56	2.95	ns, Max
GSR to Pad	T_{IOGSRQ}	5.44	5.98	6.88	ns, Max

Notes:

1. The 3-state turn-off delays should not be adjusted.

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

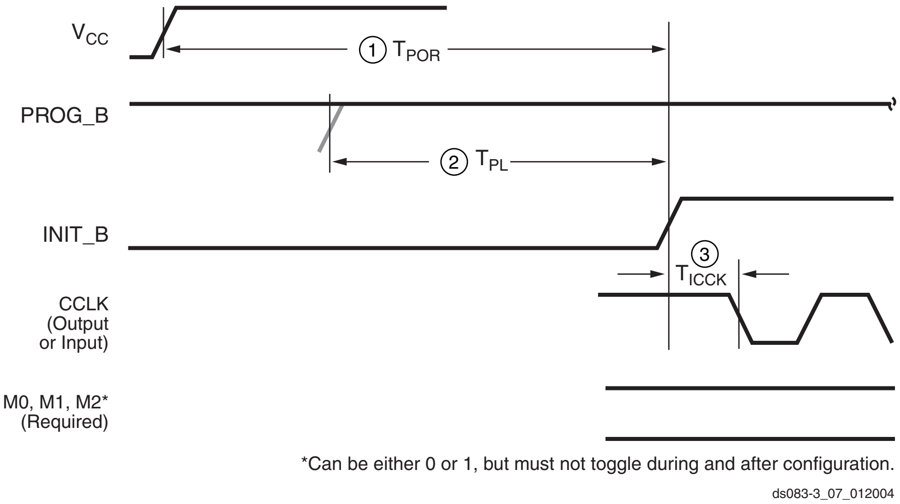


Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	µs, min
			4.0	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:

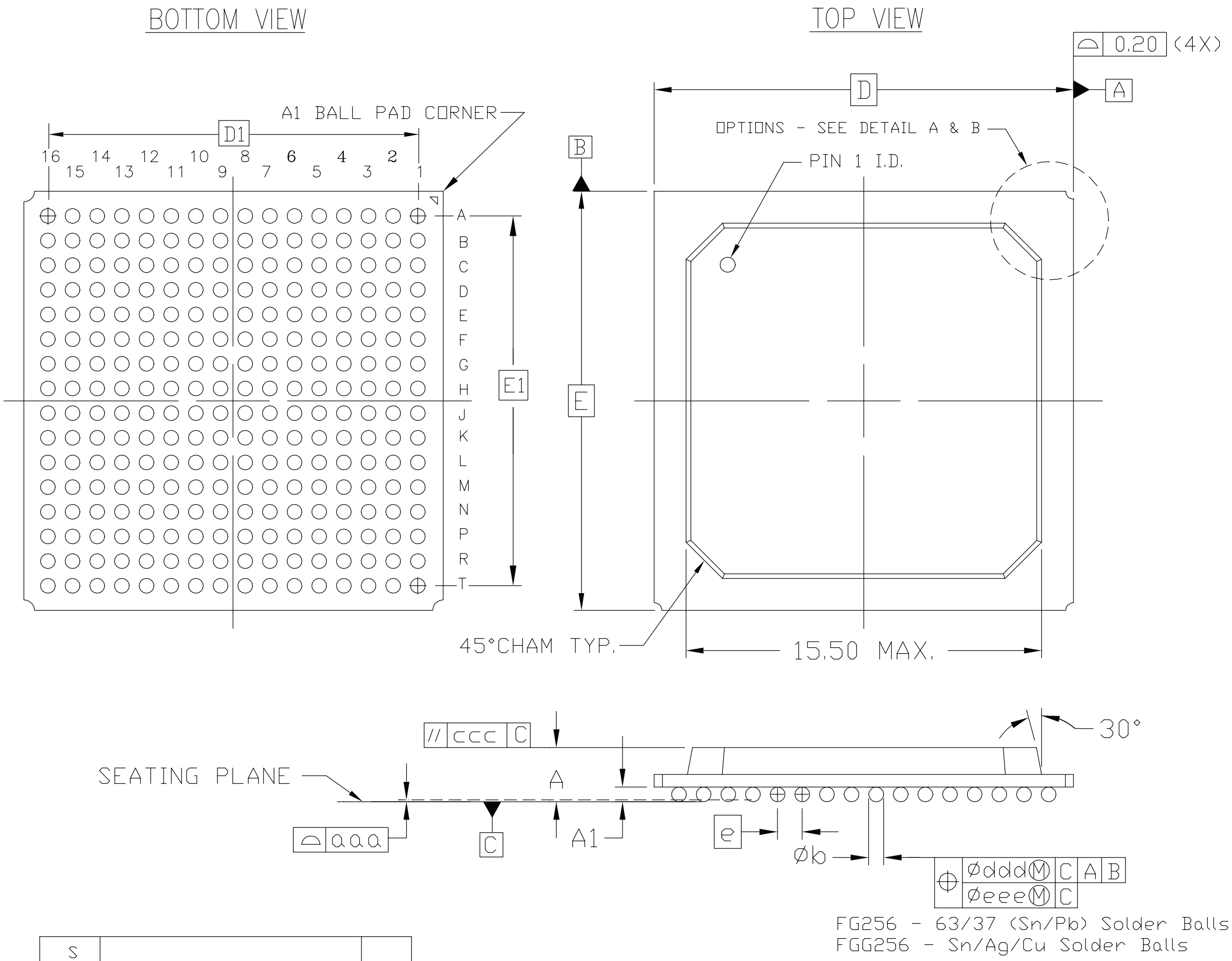
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

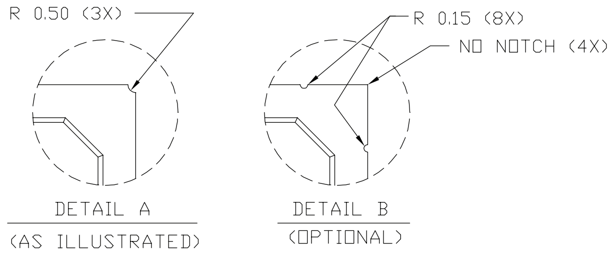
Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from "Operating junction temperature" to "Maximum junction temperature". • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word "monotonically" to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch)





SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	2.00	3
A_1	0.35	0.50	0.60	
D/E	17.00 BSC			
D_1/E_1	15.00 REF			
e	1.00 BSC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	16			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. NOMINAL DIMENSION IS TYPICALLY 1.60-1.73mm
4. CONFORMS TO JEDEC MS-034-AAF-1

256-BALL FINE PITCH BGA (FG256/FGG256)

Figure 2: **FG256/FGG256 Fine-Pitch BGA Package Specifications**

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
7	VCCO_7	H6		
7	VCCO_7	G6		
NA	CCLK	Y19		
NA	PROG_B	A2		
NA	DONE	AB20		
NA	M0	AB2		
NA	M1	W3		
NA	M2	AB3		
NA	HSWAP_EN	B3		
NA	TCK	C19		
NA	TDI	D3		
NA	TDO	D20		
NA	TMS	B20		
NA	PWRDWN_B	AB21		
NA	DXN	D5		
NA	DXP	A3		
NA	VBATT	A21		
NA	RSVD	A20		
NA	VCCAUX	AB11		
NA	VCCAUX	AA22		
NA	VCCAUX	AA1		
NA	VCCAUX	M22		
NA	VCCAUX	L1		
NA	VCCAUX	B22		
NA	VCCAUX	B1		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U6		
NA	VCCINT	T16		
NA	VCCINT	T15		
NA	VCCINT	T8		
NA	VCCINT	T7		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L21P_7/VREF_7	F3		
7	IO_L21N_7	F2		
7	IO_L19P_7	H6		
7	IO_L19N_7	H7		
7	IO_L06P_7	E1		
7	IO_L06N_7	E2		
7	IO_L04P_7	D1		
7	IO_L04N_7	D2		
7	IO_L03P_7/VREF_7	C1		
7	IO_L03N_7	C2		
7	IO_L02P_7/VRN_7	E3		
7	IO_L02N_7/VRP_7	E4		
7	IO_L01P_7	G5		
7	IO_L01N_7	F4		
0	VCCO_0	J13		
0	VCCO_0	J12		
0	VCCO_0	J11		
0	VCCO_0	H10		
0	VCCO_0	H9		
0	VCCO_0	B10		
0	VCCO_0	B7		
1	VCCO_1	B17		
1	VCCO_1	J16		
1	VCCO_1	J15		
1	VCCO_1	J14		
1	VCCO_1	H18		
1	VCCO_1	H17		
1	VCCO_1	B20		
2	VCCO_2	N18		
2	VCCO_2	M18		
2	VCCO_2	L18		
2	VCCO_2	K25		
2	VCCO_2	K19		
2	VCCO_2	J19		
2	VCCO_2	G25		
3	VCCO_3	Y25		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
1	IO_L27N_1/VREF_1	F19
1	IO_L27P_1	G19
1	IO_L25N_1	J19
1	IO_L25P_1	J20
1	IO_L24N_1	C20
1	IO_L24P_1	C21
1	IO_L22N_1	D20
1	IO_L22P_1	E21
1	IO_L21N_1/VREF_1	E20
1	IO_L21P_1	F20
1	IO_L19N_1	A21
1	IO_L19P_1	B21
1	IO_L06N_1	A22
1	IO_L06P_1	B22
1	IO_L05N_1	C22
1	IO_L05P_1	C23
1	IO_L04N_1	D22
1	IO_L04P_1/VREF_1	E22
1	IO_L03N_1/VRP_1	A23
1	IO_L03P_1/VRN_1	B23
1	IO_L02N_1	A24
1	IO_L02P_1	B24
1	IO_L01N_1	A25
1	IO_L01P_1	B25
2	IO_L01N_2	C27
2	IO_L01P_2	D27
2	IO_L02N_2/VRP_2	D25
2	IO_L02P_2/VRN_2	D26
2	IO_L03N_2	E24
2	IO_L03P_2/VREF_2	E25
2	IO_L04N_2	E26
2	IO_L04P_2	E27
2	IO_L06N_2	F23
2	IO_L06P_2	F24
2	IO_L19N_2	F25

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
7	IO_L78P_7	N6
7	IO_L78N_7	N7
7	IO_L76P_7	N9
7	IO_L76N_7	N8
7	IO_L75P_7/VREF_7	N5
7	IO_L75N_7	M6
7	IO_L73P_7	M1
7	IO_L73N_7	M2
7	IO_L72P_7	M4
7	IO_L72N_7	M5
7	IO_L70P_7	M8
7	IO_L70N_7	M9
7	IO_L69P_7/VREF_7	L1
7	IO_L69N_7	L2
7	IO_L67P_7	L3
7	IO_L67N_7	L4
7	IO_L54P_7	K1
7	IO_L54N_7	K2
7	IO_L52P_7	K4
7	IO_L52N_7	K5
7	IO_L51P_7/VREF_7	L6
7	IO_L51N_7	L7
7	IO_L49P_7	K6
7	IO_L49N_7	K7
7	IO_L48P_7	L8
7	IO_L48N_7	K8
7	IO_L46P_7	J1
7	IO_L46N_7	H1
7	IO_L45P_7/VREF_7	J2
7	IO_L45N_7	J3
7	IO_L43P_7	K3
7	IO_L43N_7	J4
7	IO_L30P_7	H3
7	IO_L30N_7	H4
7	IO_L28P_7	J5
7	IO_L28N_7	J6

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
0	IO_L22P_0	A34		
0	IO_L23N_0	K27		
0	IO_L23P_0	K26		
0	IO_L24N_0	F29		
0	IO_L24P_0	F30		
0	IO_L25N_0	B32		
0	IO_L25P_0	B33		
0	IO_L26N_0	L26		
0	IO_L26P_0	L25		
0	IO_L27N_0	G28		
0	IO_L27P_0/VREF_0	G29		
0	IO_L28N_0	C30		
0	IO_L28P_0	C31		
0	IO_L29N_0	J27		
0	IO_L29P_0	J26		
0	IO_L30N_0	D30		
0	IO_L30P_0	D31		
0	IO_L31N_0	A31	NC	
0	IO_L31P_0	A32	NC	
0	IO_L32N_0	H27	NC	
0	IO_L32P_0	H26	NC	
0	IO_L33N_0	F27	NC	
0	IO_L33P_0/VREF_0	F28	NC	
0	IO_L34N_0	B30	NC	
0	IO_L34P_0	B31	NC	
0	IO_L35N_0	M24	NC	
0	IO_L35P_0	M23	NC	
0	IO_L36N_0	D28	NC	
0	IO_L36P_0	D29	NC	
0	IO_L49N_0	C28		
0	IO_L49P_0	C29		
0	IO_L50N_0	K25		
0	IO_L50P_0	L24		
0	IO_L51N_0	E27		
0	IO_L51P_0/VREF_0	E28		
0	IO_L52N_0	A29		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L33N_1/VREF_1	D11	NC	
1	IO_L33P_1	D12	NC	
1	IO_L32N_1	H14	NC	
1	IO_L32P_1	H13	NC	
1	IO_L31N_1	A8	NC	
1	IO_L31P_1	A9	NC	
1	IO_L30N_1	F11		
1	IO_L30P_1	F12		
1	IO_L29N_1	K14		
1	IO_L29P_1	L14		
1	IO_L28N_1	C9		
1	IO_L28P_1	C10		
1	IO_L27N_1/VREF_1	G11		
1	IO_L27P_1	G12		
1	IO_L26N_1	M15		
1	IO_L26P_1	M14		
1	IO_L25N_1	B7		
1	IO_L25P_1	B8		
1	IO_L24N_1	D9		
1	IO_L24P_1	D10		
1	IO_L23N_1	J13		
1	IO_L23P_1	J12		
1	IO_L22N_1	A6		
1	IO_L22P_1	A7		
1	IO_L21N_1/VREF_1	E9		
1	IO_L21P_1	E10		
1	IO_L20N_1	D8		
1	IO_L20P_1	E7		
1	IO_L19N_1	C7		
1	IO_L19P_1	C8		
1	IO_L12N_1	F9	NC	
1	IO_L12P_1	F10	NC	
1	IO_L11N_1	H12	NC	
1	IO_L11P_1	H11	NC	
1	IO_L10N_1	B5	NC	
1	IO_L10P_1	B6	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L33P_2/VREF_2	J4	NC	
2	IO_L34N_2	K2	NC	
2	IO_L34P_2	J2	NC	
2	IO_L35N_2	P12	NC	
2	IO_L35P_2	R12	NC	
2	IO_L36N_2	M6	NC	
2	IO_L36P_2	L6	NC	
2	IO_L43N_2	L3		
2	IO_L43P_2	K3		
2	IO_L44N_2	N9		
2	IO_L44P_2	P9		
2	IO_L45N_2	M4		
2	IO_L45P_2/VREF_2	L4		
2	IO_L46N_2	L1		
2	IO_L46P_2	K1		
2	IO_L47N_2	P10		
2	IO_L47P_2	R10		
2	IO_L48N_2	N5		
2	IO_L48P_2	M5		
2	IO_L49N_2	N3		
2	IO_L49P_2	M3		
2	IO_L50N_2	N8		
2	IO_L50P_2	P8		
2	IO_L51N_2	T11		
2	IO_L51P_2/VREF_2	R11		
2	IO_L52N_2	N2		
2	IO_L52P_2	M2		
2	IO_L53N_2	T12		
2	IO_L53P_2	U12		
2	IO_L54N_2	P6		
2	IO_L54P_2	N6		
2	IO_L55N_2	N1		
2	IO_L55P_2	M1		
2	IO_L56N_2	R8		
2	IO_L56P_2	T8		
2	IO_L57N_2	R7		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L96N_7	R27	
7	IO_L95P_7	R24	
7	IO_L95N_7	N24	
7	IO_L94P_7	T29	
7	IO_L94N_7	R29	
7	IO_L93P_7/VREF_7	R31	
7	IO_L93N_7	P31	
7	IO_L92P_7	R26	
7	IO_L92N_7	P26	
7	IO_L91P_7	R30	
7	IO_L91N_7	P30	
7	IO_L78P_7	R25	
7	IO_L78N_7	P25	
7	IO_L77P_7	R28	
7	IO_L77N_7	P28	
7	IO_L76P_7	N31	
7	IO_L76N_7	M31	
7	IO_L75P_7/VREF_7	R23	
7	IO_L75N_7	P23	
7	IO_L74P_7	N30	
7	IO_L74N_7	M30	
7	IO_L73P_7	P27	
7	IO_L73N_7	N27	
7	IO_L72P_7	P22	
7	IO_L72N_7	N22	
7	IO_L71P_7	N29	
7	IO_L71N_7	M29	
7	IO_L70P_7	N28	
7	IO_L70N_7	M28	
7	IO_L69P_7/VREF_7	N26	
7	IO_L69N_7	M26	
7	IO_L68P_7	L31	
7	IO_L68N_7	K31	
7	IO_L67P_7	M27	
7	IO_L67N_7	L27	
7	IO_L54P_7	N23	
7	IO_L54N_7	M23	
7	IO_L53P_7	L30	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L53N_7	K30	
7	IO_L52P_7	L28	
7	IO_L52N_7	J28	
7	IO_L51P_7/VREF_7	M24	
7	IO_L51N_7	L24	
7	IO_L50P_7	L29	
7	IO_L50N_7	K29	
7	IO_L49P_7	M25	
7	IO_L49N_7	L25	
7	IO_L48P_7	L26	
7	IO_L48N_7	J26	
7	IO_L47P_7	J31	
7	IO_L47N_7	H31	
7	IO_L46P_7	J29	
7	IO_L46N_7	H29	
7	IO_L45P_7/VREF_7	M22	
7	IO_L45N_7	L22	
7	IO_L44P_7	J30	
7	IO_L44N_7	G30	
7	IO_L43P_7	K27	
7	IO_L43N_7	J27	
7	IO_L27P_7/VREF_7	L23	NC
7	IO_L27N_7	K23	NC
7	IO_L25P_7	G31	NC
7	IO_L25N_7	F31	NC
7	IO_L24P_7	F30	
7	IO_L24N_7	E30	
7	IO_L23P_7	K25	
7	IO_L23N_7	J25	
7	IO_L22P_7	H28	
7	IO_L22N_7	G28	
7	IO_L21P_7/VREF_7	H27	
7	IO_L21N_7	G27	
7	IO_L20P_7	K24	
7	IO_L20N_7	J24	
7	IO_L19P_7	E31	
7	IO_L19N_7	D31	
7	IO_L06P_7	F28	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	DXP	B28	
NA	VBATT	D5	
NA	RSVD	B4	
NA	VCCAUX	B16	
NA	VCCAUX	C2	
NA	VCCAUX	C30	
NA	VCCAUX	T2	
NA	VCCAUX	T30	
NA	VCCAUX	AJ2	
NA	VCCAUX	AJ30	
NA	VCCAUX	AK16	
NA	VCCINT	K15	
NA	VCCINT	K17	
NA	VCCINT	L11	
NA	VCCINT	L16	
NA	VCCINT	L21	
NA	VCCINT	M12	
NA	VCCINT	M16	
NA	VCCINT	M20	
NA	VCCINT	N13	
NA	VCCINT	N14	
NA	VCCINT	N15	
NA	VCCINT	N16	
NA	VCCINT	N17	
NA	VCCINT	N18	
NA	VCCINT	N19	
NA	VCCINT	P13	
NA	VCCINT	P19	
NA	VCCINT	R10	
NA	VCCINT	R13	
NA	VCCINT	R19	
NA	VCCINT	R22	
NA	VCCINT	T11	
NA	VCCINT	T12	
NA	VCCINT	T13	
NA	VCCINT	T19	
NA	VCCINT	T20	

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
11/22/00	1.1	Initial Xilinx release. Made the following corrections: CS144 package - Table 5, page 5: • Added missing pin D10 in Bank 1. • Changed dedicated pins A2 and B2 to RSVD (from DXN and DXP). FG256 package - Table 6, page 10: • Changed dedicated pins A3 and A4 to RSVD (from DXN and DXP). FG896 package - Table 11, page 94: • Corrected pin AG1 in Bank 4 to be AG12. FF1152 package - Table 12, page 120: • Corrected pin Y3 in Bank 6 to be Y32.
12/19/00	1.2	Reverse designations were fixed for pins in every package.
01/25/01	1.3	Data sheet divided into four modules (per current style standard). DXN and DXP pin information added for CS144 package (Table 5) and FG256 package (Table 6).
02/07/01	1.4	DXN and DXP pin information was changed back to RSVD for the CS144 package (Table 5) and the FG256 package (Table 6).
04/02/01	1.5	• ALT_VRN and ALT_VRP pin information was added for each package. • Table 8, page 34 – added No Connect designations for the XC2V1500 device in the FG676 package. • Reverted to traditional double-column format.
11/07/01	1.6	• Updated list of devices supported in the FF1152, FF1517, and BF957 packages.
09/26/02	1.7	• Updated Table 3 to reflect devices supported in the BG728 and BF957 packages. • Added mention of LVPECL to pin definition in Table 4.
10/07/02	1.8	• Corrected Table 10 heading to reflect supported devices in the BG728 package.
12/06/02	1.8.1	• Enhanced the description of the PWRDWN_B pin in Table 4.
05/07/03	1.8.2	• Added clarification to Table 4 and all device pinout tables regarding the dual-use nature of pins D0/DIN and BUSY/DOUT during configuration.
06/19/03	1.8.3	• The final GND pin in each of five pinout tables was inadvertently deleted in v1.8.2. This revision restores the deleted GND pins as follows: - Pin C5, Table 5, page 5 (CS144) - Pin A1, Table 6, page 10 (FG256) - Pin A2, Table 10, page 72 (BG728) - Pin A2, Table 12, page 120 (FF1152) - Pin AL30, Table 14, page 198 (BF957)
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	Added references to, and new package drawings for, Pb-free wire-bond packages CSG, FGG, and BGG. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	Table 4: Changed Direction for User I/O pins (IO_LXXY_#) from “Input/Output” to “Input/Output/Bidirectional”. Added requirement to V_{BATT} to connect pin to V_{CCAUX} or GND if battery is not used.
11/05/07	3.5	Updated copyright notice and legal disclaimer.