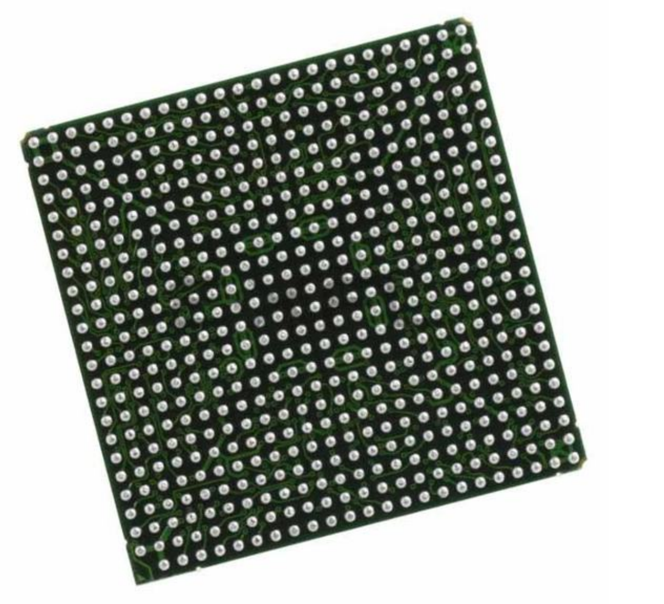
AMD Xilinx - XC2V2000-4BGG575I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	2688
Number of Logic Elements/Cells	-
Total RAM Bits	1032192
Number of I/O	408
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v2000-4bgg575i

Architecture

Virtex-II Array Overview

Virtex-II devices are user-programmable gate arrays with various configurable elements. The Virtex-II architecture is optimized for high-density and high-performance logic designs. As shown in Figure 1, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).

Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

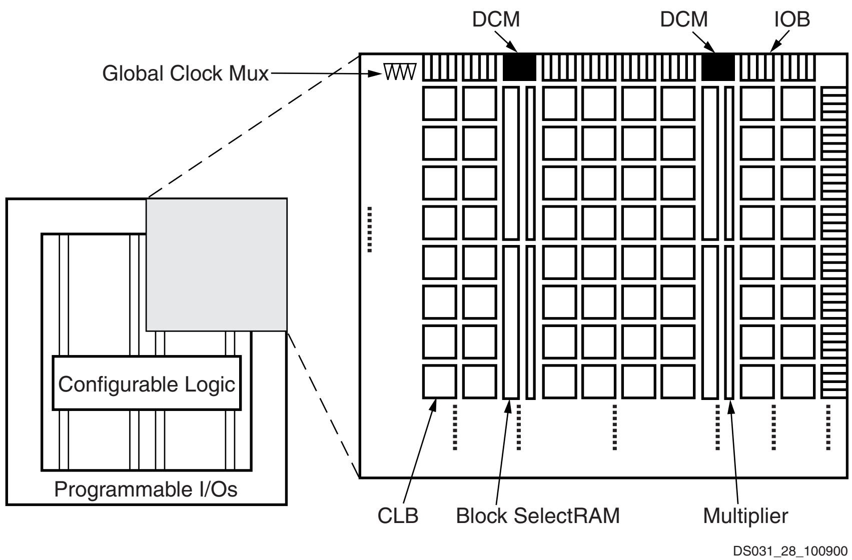


Figure 1: **Virtex-II Architecture Overview**

The internal configurable logic includes four major elements organized in a regular array.

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Virtex-II Features

This section briefly describes Virtex-II features.

Input/Output Blocks (IOBs)

IOBs are programmable and can be categorized as follows:

- Input block with an optional single-data-rate or double-data-rate (DDR) register
- Output block with an optional single-data-rate or DDR register, and an optional 3-state buffer, to be driven directly or through a single or DDR register
- Bidirectional block (any combination of input and output configurations)

These registers are either edge-triggered D-type flip-flops or level-sensitive latches.

IOBs support the following single-ended I/O standards:

- LVTTL, LVCMOS (3.3V, 2.5V, 1.8V, and 1.5V)
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- GTL and GTLP

Digitally Controlled Impedance (DCI)

Today's chip output signals with fast edge rates require termination to prevent reflections and maintain signal integrity. High pin count packages (especially ball grid arrays) can not accommodate external termination resistors.

Virtex-II XCITE DCI provides controlled impedance drivers and on-chip termination for single-ended and differential I/Os. This eliminates the need for external resistors, and improves signal integrity. The DCI feature can be used on any IOB by selecting one of the DCI I/O standards.

When applied to inputs, DCI provides input parallel termination. When applied to outputs, DCI provides controlled impedance drivers (series termination) or output parallel termination.

DCI operates independently on each I/O bank. When a DCI I/O standard is used in a particular I/O bank, external reference resistors must be connected to two dual-function pins on the bank. These resistors, voltage reference of N transistor (VRN) and the voltage reference of P transistor (VRP) are shown in Figure 9.

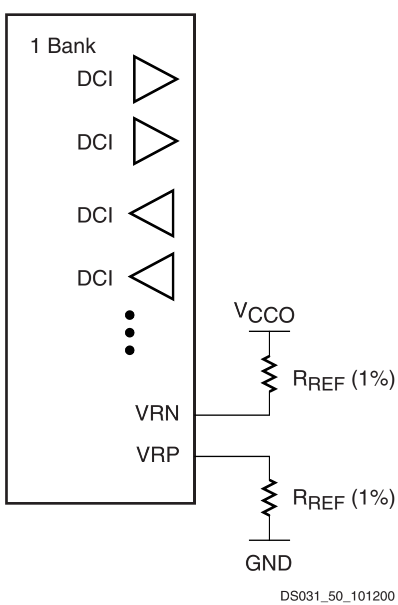


Figure 9: **DCI in a Virtex-II Bank**

When used with a terminated I/O standard, the value of resistors are specified by the standard (typically 50Ω). When used with a controlled impedance driver, the resistors set the output impedance of the driver within the specified range (25Ω to 100Ω). For all series and parallel terminations listed in Table 6 and Table 7, the reference resistors must have the same value for any given bank. One percent resistors are recommended.

The DCI system adjusts the I/O impedance to match the two external reference resistors, or half of the reference resistors, and compensates for impedance changes due to voltage and/or temperature fluctuations. The adjustment is done by turning parallel transistors in the IOB on or off.

Controlled Impedance Drivers (Series Term.)

DCI can be used to provide a buffer with a controlled output impedance. It is desirable for this output impedance to match the transmission line impedance (Z_0). Virtex-II input buffers also support LVDCI and LVDCI_DV2 I/O standards.

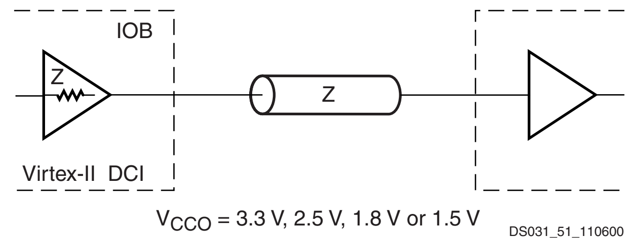


Figure 10: **Internal Series Termination**

Table 6: **SelectI/O-Ultra Controlled Impedance Buffers**

V_{CCO}	DCI	DCI Half Impedance
3.3 V	LVDCI_33	LVDCI_DV2_33
2.5 V	LVDCI_25	LVDCI_DV2_25
1.8 V	LVDCI_18	LVDCI_DV2_18
1.5 V	LVDCI_15	LVDCI_DV2_15

Controlled Impedance Drivers (Parallel)

DCI also provides on-chip termination for SSTL3, SSTL2, HSTL (Class I, II, III, or IV), and GTL/GTLP receivers or transmitters on bidirectional lines.

Table 7 and Table 8 list the on-chip parallel terminations available in Virtex-II devices. V_{CCO} must be set according to Table 3. Note that there is a V_{CCO} requirement for GTL_DCI and GTLP_DCI, due to the on-chip termination resistor.

Table 7: **SelectI/O-Ultra Buffers With On-Chip Parallel Termination**

I/O Standard Description	IOSTANDARD Attribute	
	External Termination	On-Chip Termination
SSTL3 Class I	SSTL3_I	SSTL3_I_DCI(1)
SSTL3 Class II	SSTL3_II	SSTL3_II_DCI(1)
SSTL2 Class I	SSTL2_I	SSTL2_I_DCI(1)
SSTL2 Class II	SSTL2_II	SSTL2_II_DCI(1)
HSTL Class I	HSTL_I	HSTL_I_DCI
HSTL Class II	HSTL_II	HSTL_II_DCI
HSTL Class III	HSTL_III	HSTL_III_DCI
HSTL Class IV	HSTL_IV	HSTL_IV_DCI
GTL	GTL	GTL_DCI
GTLP	GTLP	GTLP_DCI

Notes:
1. SSTL-compatible

Routing

DCM Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: **DCM Organization**

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All routing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 47.

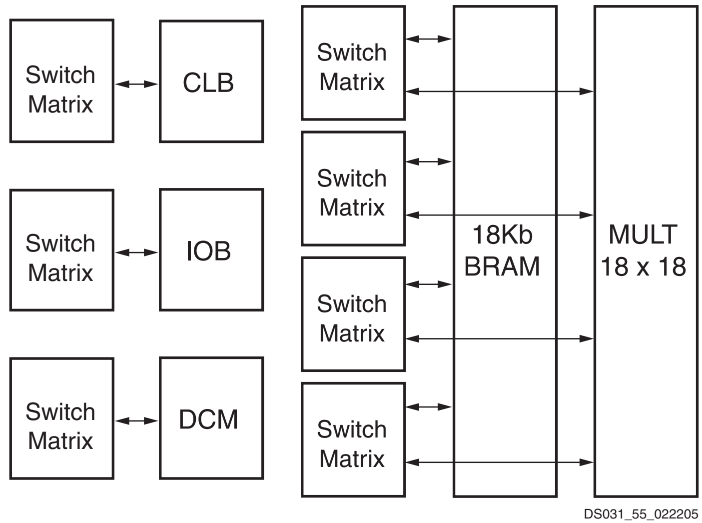


Figure 47: **Active Interconnect Technology**

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 48.

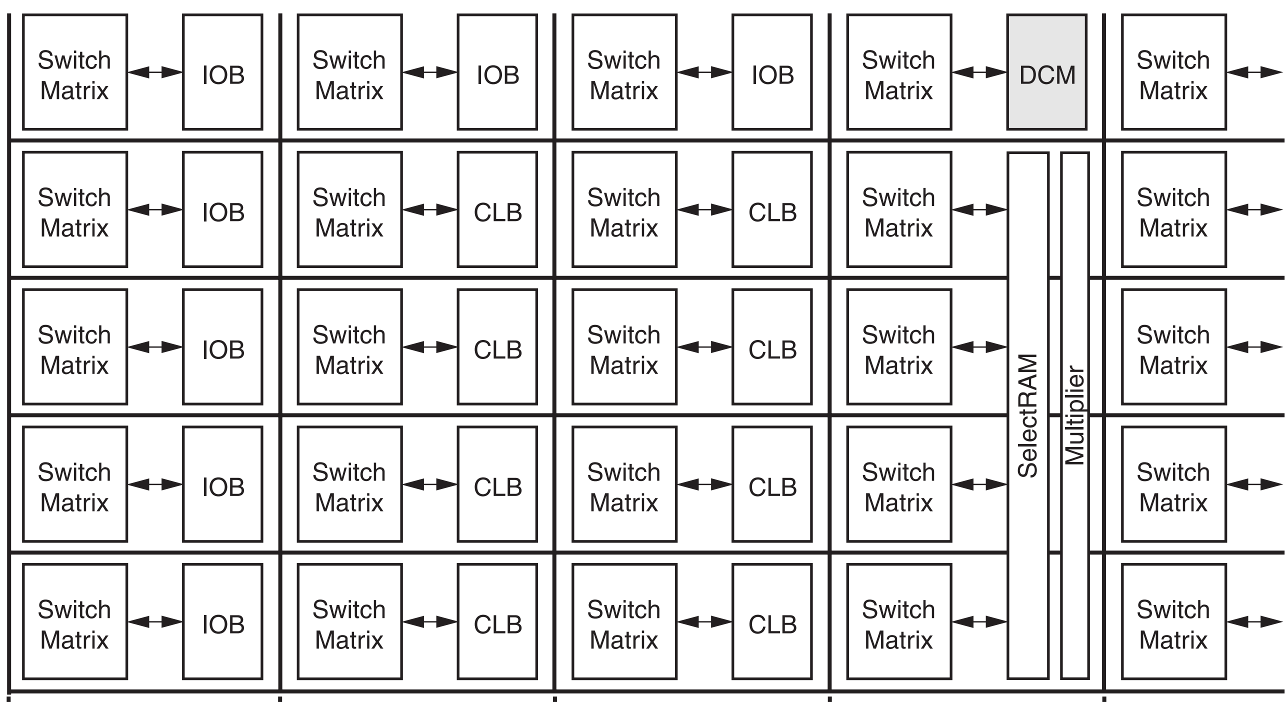


Figure 48: **Routing Resources**

Virtex-II FPGA device. Timing is similar to the Slave SerialMAP mode except that CCLK is supplied by the Virtex-II FPGA.

Boundary-Scan (JTAG, IEEE 1532) Mode

In Boundary-Scan mode, dedicated pins are used for configuring the Virtex-II device. The configuration is done entirely through the IEEE 1149.1 Test Access Port (TAP). Virtex-II device configuration using Boundary-Scan is compatible with the IEEE 1149.1-1993 standard and the new IEEE 1532 standard for In-System Configurable (ISC) devices. The IEEE 1532 standard is backward compliant with the IEEE 1149.1-1993 TAP and state machine. The IEEE Standard 1532 for In-System Configurable (ISC) devices is intended to be programmed, reprogrammed, or tested on the board via a physical and logical protocol.

Configuration through the Boundary-Scan port is always available, independent of the mode selection. Selecting the Boundary-Scan mode simply turns off the other modes.

Table 25: **Virtex-II Configuration Mode Pin Settings**

Configuration Mode(1)	M2	M1	M0	CCLK Direction	Data Width	Serial D_{OUT}(2)
Master Serial	0	0	0	Out	1	Yes
Slave Serial	1	1	1	In	1	Yes
Master SelectMAP	0	1	1	Out	8	No
Slave SelectMAP	1	1	0	In	8	No
Boundary-Scan	1	0	1	N/A	1	No

Notes:
1. The HSWAP_EN pin controls the pull-ups. Setting M2, M1, and M0 selects the configuration mode, while the HSWAP_EN pin controls whether or not the pull-ups are used.
2. Daisy chaining is possible only in modes where Serial D_{OUT} is used. For example, in SelectMAP modes, the first device does NOT support daisy chaining of downstream devices.

Table 26 lists the total number of bits required to configure each device.

Table 26: **Virtex-II Bitstream Lengths**

Device	# of Configuration Bits
XC2V40	338,976
XC2V80	598,816
XC2V250	1,593,632
XC2V500	2,560,544
XC2V1000	4,082,592
XC2V1500	5,170,208
XC2V2000	6,812,960
XC2V3000	10,494,368
XC2V4000	15,659,936
XC2V6000	21,849,504
XC2V8000	26,194,208

Configuration Sequence

The configuration of Virtex-II devices is a three-phase process after Power On Reset or POR. POR occurs when V_{CCINT} is greater than 1.2V, V_{CCAUX} is greater than 2.5V, and V_{CCO} (bank 4) is greater than 1.5V. Once the POR voltages have been reached, the three-phase process begins.

First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user. The INIT_B pin can be held Low using an open-drain driver. An open-drain is required since INIT_B is a bidirectional open-drain pin that is held Low by a Virtex-II FPGA device while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

The configuration process can also be initiated by asserting the PROG_B pin. The end of the memory-clearing phase is signaled by the INIT_B pin going High, and the completion of the entire process is signaled by the DONE pin going High. The Global Set/Reset (GSR) signal is pulsed after the last frame of configuration data is written but before the start-up sequence. The GSR signal resets all flip-flops on the device.

The default start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary. One CCLK cycle later, the Global Write Enable (GWE) signal is released. This permits the internal storage ele-

Multiplier Switching Characteristics

Table 24: **Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

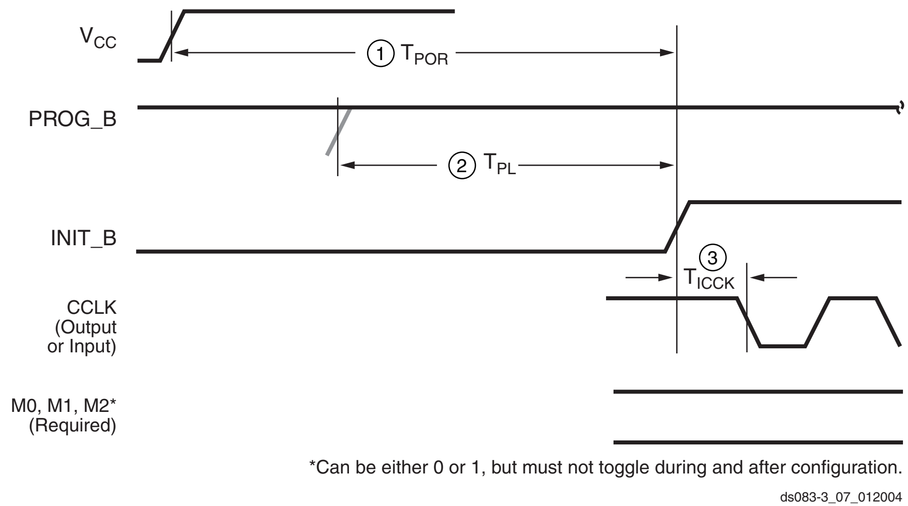


Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	μs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	μs, min
			4.0	μs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

Virtex-II Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Setup and Hold for LVTTL Standard, *With* DCM

Table 36: **Global Clock Setup and Hold for LVTTL Standard, *With* DCM**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/T_{PHDCM}	XC2V40	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V80	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V250	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1000	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V1500	1.60/–0.90	1.60/–0.90	1.84/–0.76	ns
		XC2V2000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V3000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V4000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V6000	1.70/–0.90	1.70/–0.90	1.96/–0.76	ns
		XC2V8000		1.70/–0.90	1.96/–0.76	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

Table 47: **Sample Window**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Sampling Error at Receiver Pins(1)	T_{SAMP}	XC2V40	500	500	550	ps
		XC2V80	500	500	550	ps
		XC2V250	500	500	550	ps
		XC2V500	500	500	550	ps
		XC2V1000	500	500	550	ps
		XC2V1500	500	500	550	ps
		XC2V2000	500	500	550	ps
		XC2V3000	500	500	550	ps
		XC2V4000	500	500	550	ps
		XC2V6000	500	500	550	ps
		XC2V8000		500	550	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-II DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 and CLK180 DCM jitter
   - Worst-case Duty-Cycle Distortion - T_{DCD_CLK180}
   - DCM accuracy (phase offset)
   - DCM phase shift resolution.

   These measurements do not include package or clock tree skew.

Table 48: **Pin-to-Pin Setup/Hold: Source-Synchronous Configuration**

Description	Symbol	Device	Speed Grade			Units
			-6	-5	-4	
Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Input Switching Characteristics Standard Adjustments, page 11.						
No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}	XC2V40	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V80	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V250	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V1500	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V2000	0.2/0.5	0.2/0.5	0.2/0.5	ns
		XC2V3000	0.2/0.5	0.2/0.5	0.2/0.6	ns
		XC2V4000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V6000	0.2/0.5	0.2/0.6	0.2/0.6	ns
		XC2V8000		0.2/0.6	0.2/0.7	ns

Notes:

1. IFF = Input Flip-Flop
2. The timing values were measured using the fine-phase adjustment feature of the DCM.
3. The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
6	VCCO_6	J5		
7	VCCO_7	H6		
7	VCCO_7	H5		
7	VCCO_7	G6		
NA	CCLK	P15		
NA	PROG_B	A2		
NA	DONE	R14		
NA	M0	T2		
NA	M1	P2		
NA	M2	R3		
NA	HSWAP_EN	B3		
NA	TCK	A15		
NA	TDI	C2		
NA	TDO	C15		
NA	TMS	B14		
NA	PWRDWN_B	T15		
NA	RSVD	A4		
NA	RSVD	A3		
NA	VBATT	A14		
NA	RSVD	A13		
NA	VCCAUX	R16		
NA	VCCAUX	R1		
NA	VCCAUX	B16		
NA	VCCAUX	B1		
NA	VCCINT	N13		
NA	VCCINT	N4		
NA	VCCINT	M12		
NA	VCCINT	M5		
NA	VCCINT	E12		
NA	VCCINT	E5		
NA	VCCINT	D13		
NA	VCCINT	D4		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
6	IO_L46P_6	R2		
6	IO_L46N_6	R1		
6	IO_L48P_6	P6		
6	IO_L48N_6	P5		
6	IO_L49P_6	P4	NC	
6	IO_L49N_6	P3	NC	
6	IO_L51P_6	P2	NC	
6	IO_L51N_6/VREF_6	P1	NC	
6	IO_L52P_6	N6	NC	
6	IO_L52N_6	N5	NC	
6	IO_L54P_6	N4	NC	
6	IO_L54N_6	N3	NC	
6	IO_L91P_6	N2		
6	IO_L91N_6	N1		
6	IO_L93P_6	M6		
6	IO_L93N_6/VREF_6	M5		
6	IO_L94P_6	M4		
6	IO_L94N_6	M3		
6	IO_L96P_6	M2		
6	IO_L96N_6	M1		
7	IO_L96P_7	L2		
7	IO_L96N_7	L3		
7	IO_L94P_7	L4		
7	IO_L94N_7	L5		
7	IO_L93P_7/VREF_7	K1		
7	IO_L93N_7	K2		
7	IO_L91P_7	K3		
7	IO_L91N_7	K4		
7	IO_L54P_7	L6	NC	
7	IO_L54N_7	K6	NC	
7	IO_L52P_7	K5	NC	
7	IO_L52N_7	J5	NC	
7	IO_L51P_7/VREF_7	J1	NC	

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
3	IO_L19N_3	AB26
3	IO_L19P_3	AB25
3	IO_L06N_3	AB24
3	IO_L06P_3	AB23
3	IO_L04N_3	AC27
3	IO_L04P_3	AC26
3	IO_L03N_3/VREF_3	AC25
3	IO_L03P_3	AC24
3	IO_L02N_3/VRP_3	AD27
3	IO_L02P_3/VRN_3	AE27
3	IO_L01N_3	AD26
3	IO_L01P_3	AD25
4	IO_L01N_4/BUSY/DOUT[(1)]	AF25
4	IO_L01P_4/INIT_B	AG25
4	IO_L02N_4/D0/DIN[(1)]	AF24
4	IO_L02P_4/D1	AG24
4	IO_L03N_4/D2/ALT_VRP_4	AD23
4	IO_L03P_4/D3/ALT_VRN_4	AE23
4	IO_L04N_4/VREF_4	AF23
4	IO_L04P_4	AG23
4	IO_L05N_4/VRP_4	AD22
4	IO_L05P_4/VRN_4	AE22
4	IO_L06N_4	AF22
4	IO_L06P_4	AG22
4	IO_L19N_4	AC21
4	IO_L19P_4	AB21
4	IO_L21N_4	AE21
4	IO_L21P_4/VREF_4	AE20
4	IO_L22N_4	AF21
4	IO_L22P_4	AG21
4	IO_L24N_4	AB20
4	IO_L24P_4	AA20
4	IO_L25N_4	AC20
4	IO_L25P_4	AD20
4	IO_L27N_4	AG20

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
4	IO_L94P_4	AE14
4	IO_L95N_4/GCLK3S	AF15
4	IO_L95P_4/GCLK2P	AG15
4	IO_L96N_4/GCLK1S	Y14
4	IO_L96P_4/GCLK0P	AA14
5	IO_L96N_5/GCLK7S	AC14
5	IO_L96P_5/GCLK6P	AB14
5	IO_L95N_5/GCLK5S	AG13
5	IO_L95P_5/GCLK4P	AF13
5	IO_L94N_5	AE13
5	IO_L94P_5/VREF_5	AD13
5	IO_L93N_5	AC13
5	IO_L93P_5	AB13
5	IO_L92N_5	AA13
5	IO_L92P_5	Y13
5	IO_L91N_5	W13
5	IO_L91P_5/VREF_5	W12
5	IO_L78N_5	AG12
5	IO_L78P_5	AF12
5	IO_L76N_5	AD12
5	IO_L76P_5	AC12
5	IO_L75N_5/VREF_5	AB12
5	IO_L75P_5	AB11
5	IO_L73N_5	Y12
5	IO_L73P_5	Y11
5	IO_L72N_5	AG11
5	IO_L72P_5	AF11
5	IO_L70N_5	AE11
5	IO_L70P_5	AD11
5	IO_L69N_5/VREF_5	AA10
5	IO_L69P_5	AA11
5	IO_L67N_5	AG10
5	IO_L67P_5	AF10
5	IO_L54N_5	AE10
5	IO_L54P_5	AD10

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	V19	
NA	GND	V18	
NA	GND	V17	
NA	GND	V16	
NA	GND	V15	
NA	GND	V14	
NA	GND	U21	
NA	GND	U20	
NA	GND	U19	
NA	GND	U18	
NA	GND	U17	
NA	GND	U16	
NA	GND	U15	
NA	GND	U14	
NA	GND	T26	
NA	GND	T21	
NA	GND	T20	
NA	GND	T19	
NA	GND	T18	
NA	GND	T17	
NA	GND	T16	
NA	GND	T15	
NA	GND	T14	
NA	GND	T9	
NA	GND	R33	
NA	GND	R21	
NA	GND	R20	
NA	GND	R19	
NA	GND	R18	
NA	GND	R17	
NA	GND	R16	
NA	GND	R15	
NA	GND	R14	
NA	GND	R2	
NA	GND	P28	
NA	GND	P21	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
5	IO_L25N_5	AV33		
5	IO_L25P_5	AV32		
5	IO_L24N_5	AR31		
5	IO_L24P_5	AR30		
5	IO_L23N_5	AL27		
5	IO_L23P_5	AL28		
5	IO_L22N_5	AW34		
5	IO_L22P_5	AW33		
5	IO_L21N_5/VREF_5	AN30		
5	IO_L21P_5	AP30		
5	IO_L20N_5	AM28		
5	IO_L20P_5	AM29		
5	IO_L19N_5	AU33		
5	IO_L19P_5	AU32		
5	IO_L12N_5	AT33	NC	
5	IO_L12P_5	AT32	NC	
5	IO_L11N_5	AK27	NC	
5	IO_L11P_5	AK28	NC	
5	IO_L10N_5	AV35	NC	
5	IO_L10P_5	AV34	NC	
5	IO_L09N_5/VREF_5	AP32	NC	
5	IO_L09P_5	AP31	NC	
5	IO_L08N_5	AL29	NC	
5	IO_L08P_5	AK29	NC	
5	IO_L07N_5	AW36	NC	
5	IO_L07P_5	AW35	NC	
5	IO_L06N_5	AR33		
5	IO_L06P_5	AR32		
5	IO_L05N_5/VRP_5	AM30		
5	IO_L05P_5/VRN_5	AL30		
5	IO_L04N_5	AU35		
5	IO_L04P_5/VREF_5	AU34		
5	IO_L03N_5/D4/ALT_VRP_5	AR34		
5	IO_L03P_5/D5/ALT_VRN_5	AT34		
5	IO_L02N_5/D6	AN31		
5	IO_L02P_5/D7	AM31		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	VCCO_3	AA13		
4	VCCO_4	AV14		
4	VCCO_4	AU18		
4	VCCO_4	AR11		
4	VCCO_4	AN13		
4	VCCO_4	AL15		
4	VCCO_4	AJ17		
4	VCCO_4	AG19		
4	VCCO_4	AG18		
4	VCCO_4	AG17		
4	VCCO_4	AG16		
4	VCCO_4	AG15		
4	VCCO_4	AG14		
4	VCCO_4	AF19		
4	VCCO_4	AF18		
4	VCCO_4	AF17		
4	VCCO_4	AF16		
4	VCCO_4	AF15		
5	VCCO_5	AV26		
5	VCCO_5	AU22		
5	VCCO_5	AR29		
5	VCCO_5	AN27		
5	VCCO_5	AL25		
5	VCCO_5	AJ23		
5	VCCO_5	AG26		
5	VCCO_5	AG25		
5	VCCO_5	AG24		
5	VCCO_5	AG23		
5	VCCO_5	AG22		
5	VCCO_5	AG21		
5	VCCO_5	AF25		
5	VCCO_5	AF24		
5	VCCO_5	AF23		
5	VCCO_5	AF22		
5	VCCO_5	AF21		
6	VCCO_6	AJ35		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
1	IO_L21P_1	A4	
1	IO_L20N_1	G10	
1	IO_L20P_1	G9	
1	IO_L19N_1	B6	
1	IO_L19P_1	C5	
1	IO_L06N_1	C6	
1	IO_L06P_1	D6	
1	IO_L05N_1	H9	
1	IO_L05P_1	G8	
1	IO_L04N_1	D7	
1	IO_L04P_1/VREF_1	E6	
1	IO_L03N_1/VRP_1	E8	
1	IO_L03P_1/VRN_1	E7	
1	IO_L02N_1	F8	
1	IO_L02P_1	F7	
1	IO_L01N_1	B5	
1	IO_L01P_1	B3	
2	IO_L01N_2	F5	
2	IO_L01P_2	G4	
2	IO_L02N_2/VRP_2	G6	
2	IO_L02P_2/VRN_2	H6	
2	IO_L03N_2	D3	
2	IO_L03P_2/VREF_2	E4	
2	IO_L04N_2	K10	
2	IO_L04P_2	K9	
2	IO_L05N_2	D2	
2	IO_L05P_2	E3	
2	IO_L06N_2	F4	
2	IO_L06P_2	F3	
2	IO_L19N_2	L10	
2	IO_L19P_2	M10	
2	IO_L20N_2	H7	
2	IO_L20P_2	J8	
2	IO_L21N_2	D1	
2	IO_L21P_2/VREF_2	E1	
2	IO_L22N_2	G5	
2	IO_L22P_2	H5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
6	IO_L67P_6	AB30	
6	IO_L67N_6	AA30	
6	IO_L68P_6	W26	
6	IO_L68N_6	V26	
6	IO_L69P_6	AB31	
6	IO_L69N_6/VREF_6	AA31	
6	IO_L70P_6	AA29	
6	IO_L70N_6	Y29	
6	IO_L71P_6	Y24	
6	IO_L71N_6	W24	
6	IO_L72P_6	V25	
6	IO_L72N_6	U25	
6	IO_L73P_6	Y28	
6	IO_L73N_6	W28	
6	IO_L74P_6	W23	
6	IO_L74N_6	V23	
6	IO_L75P_6	Y30	
6	IO_L75N_6/VREF_6	W30	
6	IO_L76P_6	Y31	
6	IO_L76N_6	W31	
6	IO_L77P_6	V27	
6	IO_L77N_6	U27	
6	IO_L78P_6	W29	
6	IO_L78N_6	U29	
6	IO_L91P_6	U23	
6	IO_L91N_6	T23	
6	IO_L92P_6	U26	
6	IO_L92N_6	T26	
6	IO_L93P_6	V28	
6	IO_L93N_6/VREF_6	U28	
6	IO_L94P_6	U24	
6	IO_L94N_6	T24	
6	IO_L95P_6	V30	
6	IO_L95N_6	U30	
6	IO_L96P_6	V31	
6	IO_L96N_6	U31	
7	IO_L96P_7	T27	