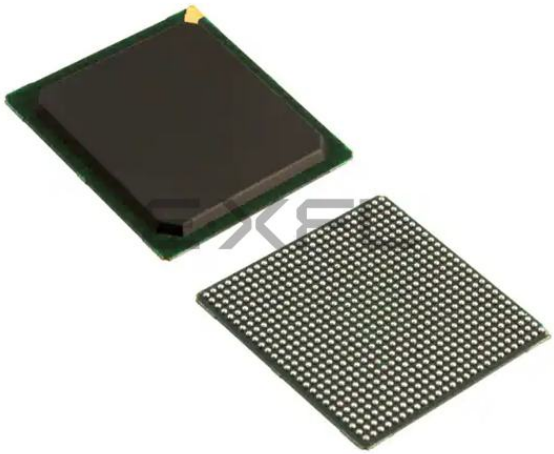

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2688
Number of Logic Elements/Cells	-
Total RAM Bits	1032192
Number of I/O	456
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v2000-4fgg676c

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under Summary of Virtex-II™ Features.
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in Table 6.
09/26/02	1.9	Updated Table 2 and Table 6 to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	*No changes in Module 1 for this revision.*
11/05/07	3.5	Updated copyright notice and legal disclaimer.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 13: **Virtex-II Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM or Shift Register (bits)	Number of Flip-Flops	Number of Carry-Chains(1)	Number of SOP Chains(1)
XC2V40	8 x 8	256	512	8,192	512	16	16
XC2V80	16 x 8	512	1,024	16,384	1,024	16	32
XC2V250	24 x 16	1,536	3,072	49,152	3,072	32	48
XC2V500	32 x 24	3,072	6,144	98,304	6,144	48	64
XC2V1000	40 x 32	5,120	10,240	163,840	10,240	64	80
XC2V1500	48 x 40	7,680	15,360	245,760	15,360	80	96
XC2V2000	56 x 48	10,752	21,504	344,064	21,504	96	112
XC2V3000	64 x 56	14,336	28,672	458,752	28,672	112	128
XC2V4000	80 x 72	23,040	46,080	737,280	46,080	144	160
XC2V6000	96 x 88	33,792	67,584	1,081,344	67,584	176	192
XC2V8000	112 x 104	46,592	93,184	1,490,944	93,184	208	224

Notes:
1. The carry-chains and SOP chains can be split or cascaded.

18 Kbit Block SelectRAM Resources

Introduction

Virtex-II devices incorporate large amounts of 18 Kbit block SelectRAM. These complement the distributed SelectRAM resources that provide shallow RAM structures implemented in CLBs. Each Virtex-II block SelectRAM is an 18 Kbit true dual-port RAM with two independently clocked and independently controlled synchronous ports that access a common storage area. Both ports are functionally identical. CLK, EN, WE, and SSR polarities are defined through configuration.

Each port has the following types of inputs: Clock and Clock Enable, Write Enable, Set/Reset, and Address, as well as separate Data/parity data inputs (for write) and Data/parity data outputs (for read).

Operation is synchronous; the block SelectRAM behaves like a register. Control, address and data inputs must (and need only) be valid during the set-up time window prior to a rising (or falling, a configuration option) clock edge. Data outputs change as a result of the same clock edge.

Configuration

The Virtex-II block SelectRAM supports various configurations, including single- and dual-port RAM and various data/address aspect ratios. Supported memory configurations for single- and dual-port modes are shown in Table 14.

Table 14: **Dual- and Single-Port Configurations**

16K x 1 bit	2K x 9 bits
8K x 2 bits	1K x 18 bits
4K x 4 bits	512 x 36 bits

Single-Port Configuration

As a single-port RAM, the block SelectRAM has access to the 18 Kbit memory locations in any of the 2K x 9-bit, 1K x 18-bit, or 512 x 36-bit configurations and to 16 Kbit memory locations in any of the 16K x 1-bit, 8K x 2-bit, or 4K x 4-bit configurations. The advantage of the 9-bit, 18-bit and 36-bit widths is the ability to store a parity bit for each eight bits. Parity bits must be generated or checked externally in user logic. In such cases, the width is viewed as 8 + 1, 16 + 2, or 32 + 4. These extra parity bits are stored and behave exactly as the other bits, including the timing parameters. Video applications can use the 9-bit ratio of Virtex-II block SelectRAM memory to advantage.

Each block SelectRAM cell is a fully synchronous memory as illustrated in Figure 29. Input data bus and output data bus widths are identical.

Each SelectRAM memory and multiplier block is tied to four switch matrices, as shown in Figure 35.

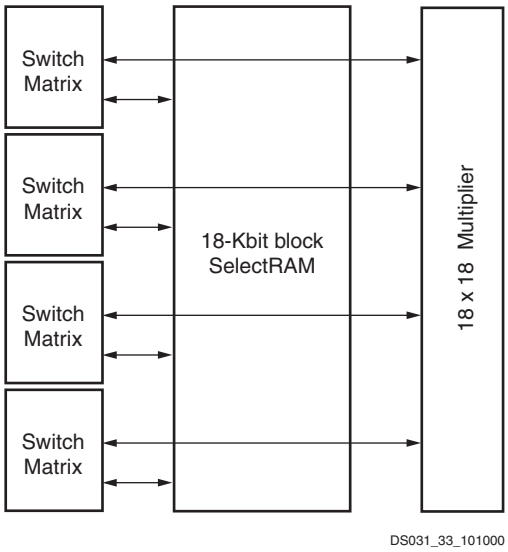


Figure 35: **SelectRAM and Multiplier Blocks**

Association With Block SelectRAM Memory

The interconnect is designed to allow SelectRAM memory and multiplier blocks to be used at the same time, but some interconnect is shared between the SelectRAM and the multiplier. Thus, SelectRAM memory can be used only up to 18 bits wide when the multiplier is used, because the multiplier shares inputs with the upper data bits of the SelectRAM memory.

This sharing of the interconnect is optimized for an 18-bit-wide block SelectRAM resource feeding the multiplier. The use of SelectRAM memory and the multiplier with an accumulator in LUTs allows for implementation of a digital signal processor (DSP) multiplier-accumulator (MAC) function, which is commonly used in finite and infinite impulse response (FIR and IIR) digital filters.

Configuration

The multiplier block is an 18-bit by 18-bit signed multiplier (2's complement). Both A and B are 18-bit-wide inputs, and the output is 36 bits. Figure 36 shows a multiplier block.

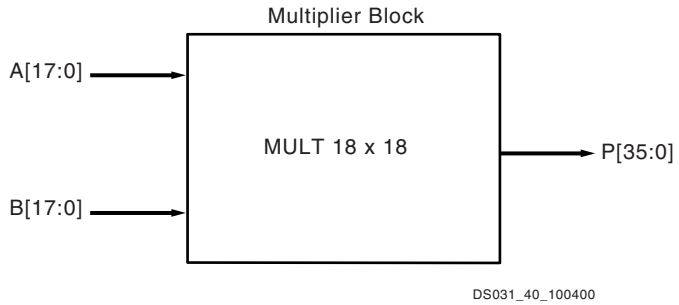


Figure 36: **Multiplier Block**

Locations / Organization

Multiplier organization is identical to the 18 Kbit SelectRAM organization, because each multiplier is associated with an 18 Kbit block SelectRAM resource.

In addition to the built-in multiplier blocks, the CLB elements have dedicated logic to implement efficient multipliers in logic. (Refer to Configurable Logic Blocks (CLBs)).

Table 20: **Multiplier Floor Plan**

Device	Columns	Multipliers	
		Per Column	Total
XC2V40	2	2	4
XC2V80	2	4	8
XC2V250	4	6	24
XC2V500	4	8	32
XC2V1000	4	10	40
XC2V1500	4	12	48
XC2V2000	4	14	56
XC2V3000	6	16	96
XC2V4000	6	20	120
XC2V6000	6	24	144
XC2V8000	6	28	168

Table 25: **Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/ 0.00	3.45/ 0.00	3.89/ 0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/ 0.00	0.80/ 0.00	0.86/ 0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T_{MULTCK_P35}	3.05	6.91	8.12	ns, Max
Clock to Pin 34	T_{MULTCK_P34}	2.95	6.75	7.93	ns, Max
Clock to Pin 33	T_{MULTCK_P33}	2.85	6.59	7.74	ns, Max
Clock to Pin 32	T_{MULTCK_P32}	2.76	6.43	7.56	ns, Max
Clock to Pin 31	T_{MULTCK_P31}	2.66	6.27	7.37	ns, Max
Clock to Pin 30	T_{MULTCK_P30}	2.56	6.11	7.19	ns, Max
Clock to Pin 29	T_{MULTCK_P29}	2.47	5.95	7.00	ns, Max
Clock to Pin 28	T_{MULTCK_P28}	2.37	5.79	6.81	ns, Max
Clock to Pin 27	T_{MULTCK_P27}	2.27	5.63	6.63	ns, Max
Clock to Pin 26	T_{MULTCK_P26}	2.17	5.47	6.44	ns, Max
Clock to Pin 25	T_{MULTCK_P25}	2.08	5.31	6.26	ns, Max
Clock to Pin 24	T_{MULTCK_P24}	1.98	5.15	6.07	ns, Max
Clock to Pin 23	T_{MULTCK_P23}	1.88	4.99	5.88	ns, Max
Clock to Pin 22	T_{MULTCK_P22}	1.79	4.83	5.70	ns, Max
Clock to Pin 21	T_{MULTCK_P21}	1.69	4.67	5.51	ns, Max
Clock to Pin 20	T_{MULTCK_P20}	1.59	4.51	5.33	ns, Max
Clock to Pin 19	T_{MULTCK_P19}	1.50	4.35	5.14	ns, Max
Clock to Pin 18	T_{MULTCK_P18}	1.40	4.19	4.95	ns, Max
Clock to Pin 17	T_{MULTCK_P17}	1.30	4.03	4.77	ns, Max
Clock to Pin 16	T_{MULTCK_P16}	1.20	3.87	4.58	ns, Max
Clock to Pin 15	T_{MULTCK_P15}	1.11	3.71	4.40	ns, Max
Clock to Pin 14	T_{MULTCK_P14}	1.01	3.55	4.21	ns, Max
Clock to Pin 13	T_{MULTCK_P13}	0.91	3.39	4.02	ns, Max
Clock to Pin 12	T_{MULTCK_P12}	0.91	3.23	3.84	ns, Max
Clock to Pin 11	T_{MULTCK_P11}	0.91	3.07	3.65	ns, Max
Clock to Pin 10	T_{MULTCK_P10}	0.91	2.91	3.47	ns, Max
Clock to Pin 9	T_{MULTCK_P9}	0.91	2.75	3.28	ns, Max
Clock to Pin 8	T_{MULTCK_P8}	0.91	2.59	3.09	ns, Max
Clock to Pin 7	T_{MULTCK_P7}	0.91	2.43	2.91	ns, Max
Clock to Pin 6	T_{MULTCK_P6}	0.91	2.27	2.72	ns, Max
Clock to Pin 5	T_{MULTCK_P5}	0.91	2.11	2.54	ns, Max
Clock to Pin 4	T_{MULTCK_P4}	0.91	1.95	2.35	ns, Max
Clock to Pin 3	T_{MULTCK_P3}	0.91	1.79	2.16	ns, Max
Clock to Pin 2	T_{MULTCK_P2}	0.91	1.63	1.98	ns, Max
Clock to Pin 1	T_{MULTCK_P1}	0.91	1.47	1.79	ns, Max
Clock to Pin 0	T_{MULTCK_P0}	0.91	1.31	1.61	ns, Max

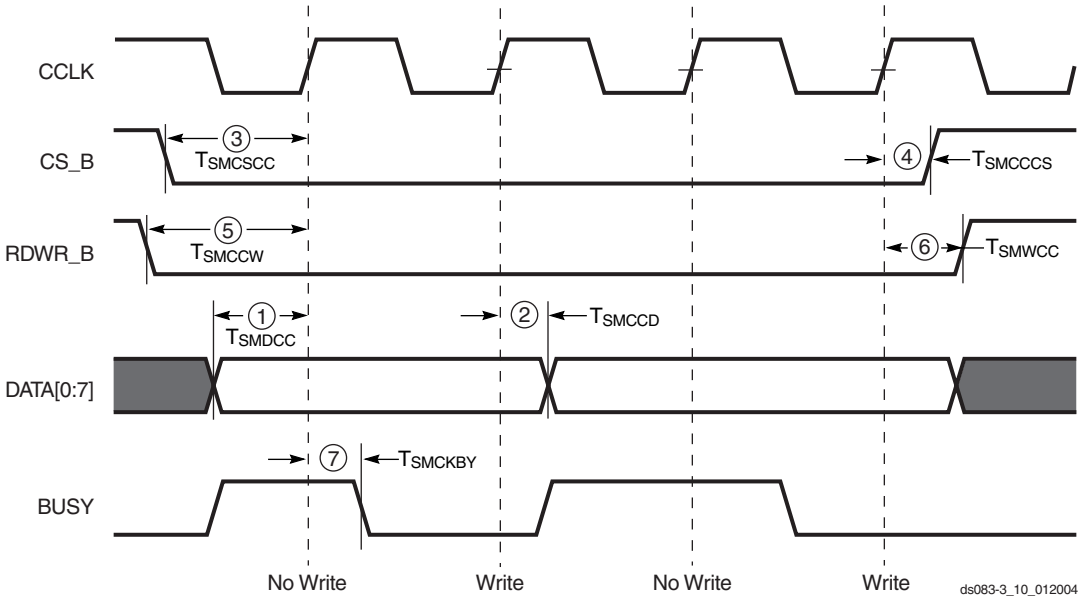


Figure 5: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 32: **SelectMAP Mode Write Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	CS_B setup/hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		$F_{CC\_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake		F_{CCNH}	50	MHz, max

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
3	IO_L96N_3	J16		
3	IO_L96P_3	J15		
3	IO_L94N_3	J14		
3	IO_L94P_3	J13		
3	IO_L93N_3/VREF_3	K16	NC	
3	IO_L93P_3	K15	NC	
3	IO_L91N_3	K14	NC	
3	IO_L91P_3	K13	NC	
3	IO_L45N_3/VREF_3	K12	NC	NC
3	IO_L45P_3	L12	NC	NC
3	IO_L43N_3	L16	NC	NC
3	IO_L43P_3	L15	NC	NC
3	IO_L06N_3	L14	NC	
3	IO_L06P_3	L13	NC	
3	IO_L04N_3	M16	NC	
3	IO_L04P_3	M15	NC	
3	IO_L03N_3/VREF_3	M14		
3	IO_L03P_3	M13		
3	IO_L02N_3/VRP_3	N15		
3	IO_L02P_3/VRN_3	N14		
3	IO_L01N_3	N16		
3	IO_L01P_3	P16		
4	IO_L01N_4/BUSY/DOUT(1)	T14		
4	IO_L01P_4/INIT_B	T13		
4	IO_L02N_4/D0/DIN(1)	P13		
4	IO_L02P_4/D1	R13		
4	IO_L03N_4/D2/ALT_VRP_4	N12		
4	IO_L03P_4/D3/ALT_VRN_4	P12		
4	IO_L04N_4/VREF_4	R12	NC	NC
4	IO_L04P_4	T12	NC	NC
4	IO_L05N_4/VRP_4	N11	NC	NC
4	IO_L05P_4/VRN_4	P11	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
0	VCCO_0	F7		
1	VCCO_1	G14		
1	VCCO_1	G13		
1	VCCO_1	G12		
1	VCCO_1	F16		
1	VCCO_1	F15		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	J16		
2	VCCO_2	H17		
2	VCCO_2	G17		
3	VCCO_3	T17		
3	VCCO_3	R17		
3	VCCO_3	P16		
3	VCCO_3	N16		
3	VCCO_3	M16		
4	VCCO_4	U16		
4	VCCO_4	U15		
4	VCCO_4	T14		
4	VCCO_4	T13		
4	VCCO_4	T12		
5	VCCO_5	U8		
5	VCCO_5	U7		
5	VCCO_5	T11		
5	VCCO_5	T10		
5	VCCO_5	T9		
6	VCCO_6	T6		
6	VCCO_6	R6		
6	VCCO_6	P7		
6	VCCO_6	N7		
6	VCCO_6	M7		
7	VCCO_7	L7		
7	VCCO_7	K7		
7	VCCO_7	J7		

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
6	IO_L06N_6	V6		
6	IO_L19P_6	U7		
6	IO_L19N_6	T8		
6	IO_L21P_6	AA1		
6	IO_L21N_6/VREF_6	Y2		
6	IO_L22P_6	Y1		
6	IO_L22N_6	W1		
6	IO_L24P_6	W2		
6	IO_L24N_6	V2		
6	IO_L43P_6	V4		
6	IO_L43N_6	V3		
6	IO_L45P_6	U6		
6	IO_L45N_6/VREF_6	U5		
6	IO_L46P_6	T7		
6	IO_L46N_6	T6		
6	IO_L48P_6	R8		
6	IO_L48N_6	R7		
6	IO_L49P_6	U2		
6	IO_L49N_6	U1		
6	IO_L51P_6	U4		
6	IO_L51N_6/VREF_6	U3		
6	IO_L52P_6	T1		
6	IO_L52N_6	R1		
6	IO_L54P_6	T3		
6	IO_L54N_6	T2		
6	IO_L67P_6	T5	NC	
6	IO_L67N_6	T4	NC	
6	IO_L69P_6	R6	NC	
6	IO_L69N_6/VREF_6	R5	NC	
6	IO_L70P_6	P8	NC	
6	IO_L70N_6	P7	NC	
6	IO_L72P_6	R2	NC	
6	IO_L72N_6	P1	NC	
6	IO_L73P_6	R3	NC	NC
6	IO_L73N_6	P3	NC	NC
6	IO_L91P_6	P5		

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
5	IO_L52N_5	AC10
5	IO_L52P_5	AB10
5	IO_L51N_5/VREF_5	Y9
5	IO_L51P_5	Y10
5	IO_L49N_5	AG9
5	IO_L49P_5	AG8
5	IO_L30N_5	AF9
5	IO_L30P_5	AE9
5	IO_L28N_5	AD9
5	IO_L28P_5	AC9
5	IO_L27N_5/VREF_5	AB9
5	IO_L27P_5	AA9
5	IO_L25N_5	AE8
5	IO_L25P_5	AE7
5	IO_L24N_5	AD8
5	IO_L24P_5	AC8
5	IO_L22N_5	AB8
5	IO_L22P_5	AA8
5	IO_L21N_5/VREF_5	AG7
5	IO_L21P_5	AF7
5	IO_L19N_5	AC7
5	IO_L19P_5	AB7
5	IO_L06N_5	AG6
5	IO_L06P_5	AF6
5	IO_L05N_5/VRP_5	AE6
5	IO_L05P_5/VRN_5	AD6
5	IO_L04N_5	AG5
5	IO_L04P_5/VREF_5	AF5
5	IO_L03N_5/D4/ALT_VRP_5	AE5
5	IO_L03P_5/D5/ALT_VRN_5	AD5
5	IO_L02N_5/D6	AG4
5	IO_L02P_5/D7	AF4
5	IO_L01N_5/RDWR_B	AG3
5	IO_L01P_5/CS_B	AF3
6	IO_L01P_6	AE1

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L53N_0	G20		
0	IO_L53P_0	G19		
0	IO_L54N_0	D21		
0	IO_L54P_0	D22		
0	IO_L67N_0	E20	NC	
0	IO_L67P_0	E21	NC	
0	IO_L68N_0	H19	NC	
0	IO_L68P_0	H18	NC	
0	IO_L69N_0	D20	NC	
0	IO_L69P_0/VREF_0	D19	NC	
0	IO_L70N_0	A20	NC	
0	IO_L70P_0	A21	NC	
0	IO_L71N_0	F19	NC	
0	IO_L71P_0	F18	NC	
0	IO_L72N_0	C19	NC	
0	IO_L72P_0	C20	NC	
0	IO_L73N_0	B18	NC	NC
0	IO_L73P_0	B19	NC	NC
0	IO_L74N_0	G18	NC	NC
0	IO_L74P_0	H17	NC	NC
0	IO_L75N_0	E18	NC	NC
0	IO_L75P_0/VREF_0	D18	NC	NC
0	IO_L76N_0	A18	NC	NC
0	IO_L76P_0	A19	NC	NC
0	IO_L77N_0	J17	NC	NC
0	IO_L77P_0	J16	NC	NC
0	IO_L78N_0	E16	NC	NC
0	IO_L78P_0	E17	NC	NC
0	IO_L91N_0/VREF_0	B17		
0	IO_L91P_0	B16		
0	IO_L92N_0	F17		
0	IO_L92P_0	F16		
0	IO_L93N_0	D16		
0	IO_L93P_0	D17		
0	IO_L94N_0/VREF_0	A17		
0	IO_L94P_0	A16		
0	IO_L95N_0/GCLK7P	H16		

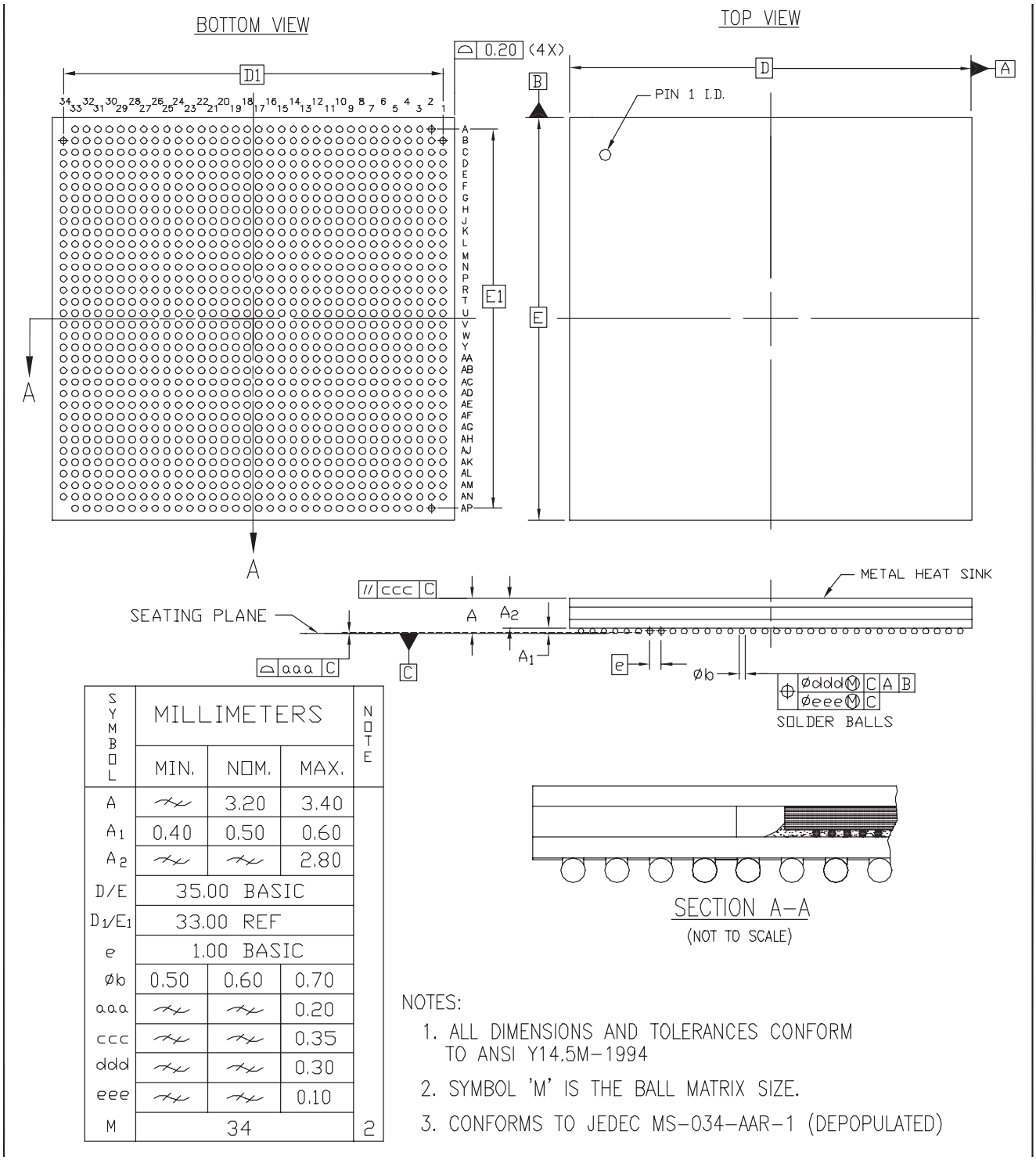
Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
2	IO_L48N_2	J5		
2	IO_L48P_2	H5		
2	IO_L49N_2	J3		
2	IO_L49P_2	H3		
2	IO_L50N_2	K7		
2	IO_L50P_2	L7		
2	IO_L51N_2	J4		
2	IO_L51P_2/VREF_2	K4		
2	IO_L52N_2	K1		
2	IO_L52P_2	J1		
2	IO_L53N_2	L6		
2	IO_L53P_2	M6		
2	IO_L54N_2	L5		
2	IO_L54P_2	K5		
2	IO_L67N_2	L2	NC	
2	IO_L67P_2	K2	NC	
2	IO_L68N_2	M8	NC	
2	IO_L68P_2	N8	NC	
2	IO_L69N_2	L4	NC	
2	IO_L69P_2/VREF_2	M4	NC	
2	IO_L70N_2	M1	NC	
2	IO_L70P_2	L1	NC	
2	IO_L71N_2	M7	NC	
2	IO_L71P_2	N7	NC	
2	IO_L72N_2	M3	NC	
2	IO_L72P_2	L3	NC	
2	IO_L73N_2	N2	NC	NC
2	IO_L73P_2	M2	NC	NC
2	IO_L74N_2	N6	NC	NC
2	IO_L74P_2	P6	NC	NC
2	IO_L75N_2	N5	NC	NC
2	IO_L75P_2/VREF_2	N4	NC	NC
2	IO_L76N_2	P1	NC	NC
2	IO_L76P_2	N1	NC	NC
2	IO_L77N_2	P9	NC	NC
2	IO_L77P_2	R9	NC	NC
2	IO_L78N_2	R5	NC	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	GND	P20	
NA	GND	P19	
NA	GND	P18	
NA	GND	P17	
NA	GND	P16	
NA	GND	P15	
NA	GND	P14	
NA	GND	P7	
NA	GND	M30	
NA	GND	M5	
NA	GND	K32	
NA	GND	K3	
NA	GND	J19	
NA	GND	J16	
NA	GND	H34	
NA	GND	H27	
NA	GND	H8	
NA	GND	H1	
NA	GND	G28	
NA	GND	G21	
NA	GND	G14	
NA	GND	G7	
NA	GND	F29	
NA	GND	F6	
NA	GND	E30	
NA	GND	E23	
NA	GND	E12	
NA	GND	E5	
NA	GND	D31	
NA	GND	D4	
NA	GND	C34	
NA	GND	C32	
NA	GND	C25	
NA	GND	C10	
NA	GND	C3	
NA	GND	C1	

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 8: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
1	IO_L69N_1/VREF_1	E15		
1	IO_L69P_1	E16		
1	IO_L68N_1	K17		
1	IO_L68P_1	K16		
1	IO_L67N_1	C15		
1	IO_L67P_1	B15		
1	IO_L60N_1	F15		
1	IO_L60P_1	F16		
1	IO_L59N_1	H16		
1	IO_L59P_1	H15		
1	IO_L58N_1	C13		
1	IO_L58P_1	C14		
1	IO_L57N_1/VREF_1	D13		
1	IO_L57P_1	D14		
1	IO_L56N_1	M17		
1	IO_L56P_1	M16		
1	IO_L55N_1	A12		
1	IO_L55P_1	A13		
1	IO_L54N_1	B12		
1	IO_L54P_1	B13		
1	IO_L53N_1	G15		
1	IO_L53P_1	G14		
1	IO_L52N_1	C11		
1	IO_L52P_1	C12		
1	IO_L51N_1/VREF_1	F13		
1	IO_L51P_1	F14		
1	IO_L50N_1	L16		
1	IO_L50P_1	L15		
1	IO_L49N_1	A10		
1	IO_L49P_1	A11		
1	IO_L36N_1	E12	NC	
1	IO_L36P_1	E13	NC	
1	IO_L35N_1	K15	NC	
1	IO_L35P_1	J14	NC	
1	IO_L34N_1	B9	NC	
1	IO_L34P_1	B10	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
2	IO_L81P_2/VREF_2	U5		
2	IO_L82N_2	V2		
2	IO_L82P_2	U2		
2	IO_L83N_2	V8		
2	IO_L83P_2	W8		
2	IO_L84N_2	W7		
2	IO_L84P_2	V7		
2	IO_L91N_2	W1		
2	IO_L91P_2	V1		
2	IO_L92N_2	Y11		
2	IO_L92P_2	Y12		
2	IO_L93N_2	W4		
2	IO_L93P_2/VREF_2	V4		
2	IO_L94N_2	W2		
2	IO_L94P_2	W3		
2	IO_L95N_2	Y8		
2	IO_L95P_2	Y9		
2	IO_L96N_2	W5		
2	IO_L96P_2	W6		
3	IO_L96N_3	AB8		
3	IO_L96P_3	AA8		
3	IO_L95N_3	Y3		
3	IO_L95P_3	AA3		
3	IO_L94N_3	Y6		
3	IO_L94P_3	AA6		
3	IO_L93N_3/VREF_3	AB9		
3	IO_L93P_3	AA9		
3	IO_L92N_3	AA1		
3	IO_L92P_3	AB1		
3	IO_L91N_3	Y5		
3	IO_L91P_3	AA5		
3	IO_L84N_3	AB10		
3	IO_L84P_3	AA10		
3	IO_L83N_3	AA2		
3	IO_L83P_3	AB2		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	D10	
NA	GND	D16	
NA	GND	D22	
NA	GND	D28	
NA	GND	E5	
NA	GND	E27	
NA	GND	F6	
NA	GND	F26	
NA	GND	G7	
NA	GND	G13	
NA	GND	G16	
NA	GND	G19	
NA	GND	G25	
NA	GND	H2	
NA	GND	H8	
NA	GND	H24	
NA	GND	H30	
NA	GND	J9	
NA	GND	J23	
NA	GND	K4	
NA	GND	K16	
NA	GND	K28	
NA	GND	N7	
NA	GND	N25	
NA	GND	P14	
NA	GND	P15	
NA	GND	P16	
NA	GND	P17	
NA	GND	P18	
NA	GND	R14	
NA	GND	R15	
NA	GND	R16	
NA	GND	R17	
NA	GND	R18	
NA	GND	T1	
NA	GND	T4	
NA	GND	T7	
NA	GND	T10	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	T14	
NA	GND	T15	
NA	GND	T16	
NA	GND	T17	
NA	GND	T18	
NA	GND	T22	
NA	GND	T25	
NA	GND	T28	
NA	GND	T31	
NA	GND	U14	
NA	GND	U15	
NA	GND	U16	
NA	GND	U17	
NA	GND	U18	
NA	GND	V14	
NA	GND	V15	
NA	GND	V16	
NA	GND	V17	
NA	GND	V18	
NA	GND	W7	
NA	GND	W25	
NA	GND	AB4	
NA	GND	AB16	
NA	GND	AB28	
NA	GND	AC9	
NA	GND	AC23	
NA	GND	AD2	
NA	GND	AD8	
NA	GND	AD24	
NA	GND	AD30	
NA	GND	AE7	
NA	GND	AE13	
NA	GND	AE16	
NA	GND	AE19	
NA	GND	AE25	
NA	GND	AF6	
NA	GND	AF26	
NA	GND	AG5	

Table 14: **BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000**

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	GND	AG27	
NA	GND	AH4	
NA	GND	AH10	
NA	GND	AH16	
NA	GND	AH22	
NA	GND	AH28	
NA	GND	AJ1	
NA	GND	AJ3	
NA	GND	AJ29	
NA	GND	AJ31	
NA	GND	AK1	
NA	GND	AK2	
NA	GND	AK8	
NA	GND	AK24	
NA	GND	AK30	
NA	GND	AK31	
NA	GND	AL2	
NA	GND	AL3	
NA	GND	AL16	
NA	GND	AL29	
NA	GND	AL30	

Notes:
1. See Table 4 for an explanation of the signals available on this pin.