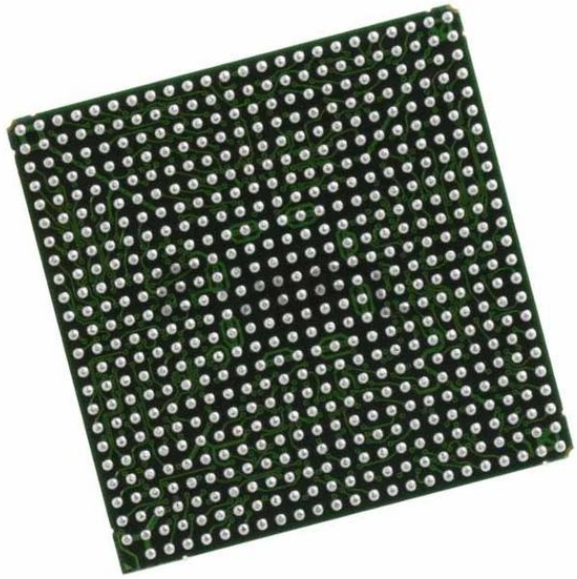
AMD Xilinx - XC2V2000-5BGG575C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2688
Number of Logic Elements/Cells	-
Total RAM Bits	1032192
Number of I/O	408
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	575-BBGA
Supplier Device Package	575-BGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v2000-5bgg575c

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

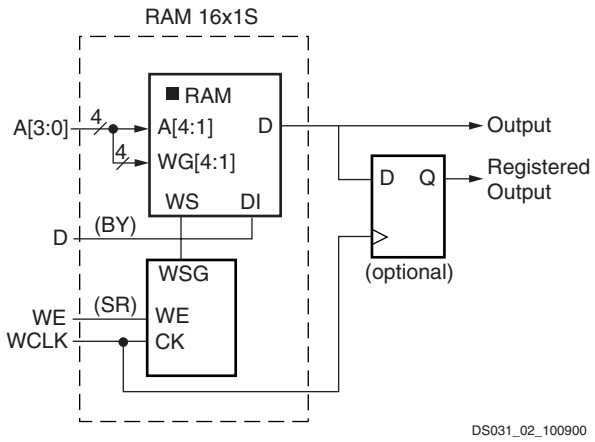


Figure 18: **Distributed SelectRAM (RAM16x1S)**

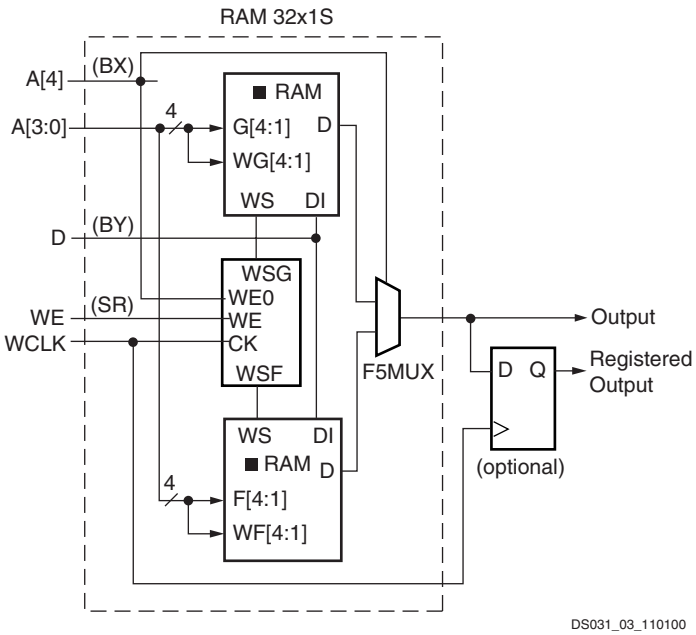


Figure 19: **Single-Port Distributed SelectRAM (RAM32x1S)**

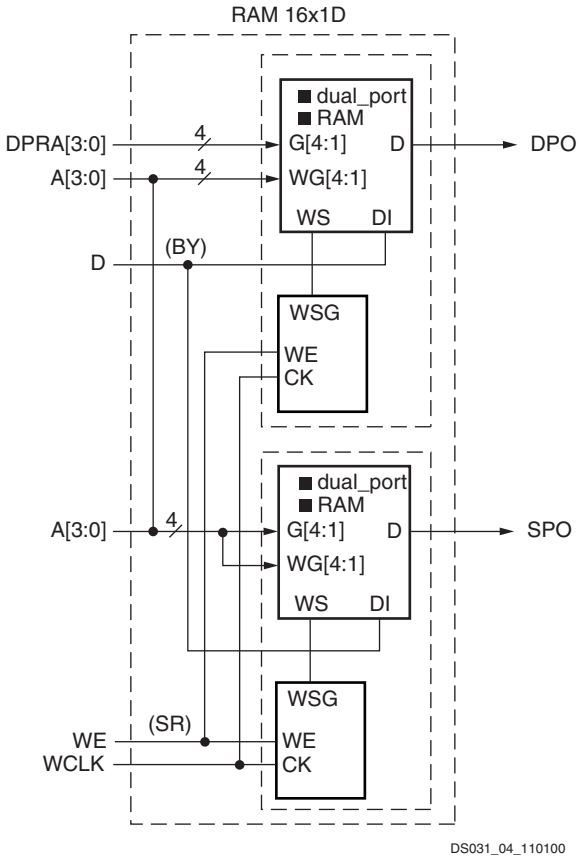


Figure 20: **Dual-Port Distributed SelectRAM (RAM16x1D)**

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: **ROM Configuration**

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Multiplexers

Virtex-II function generators and associated multiplexers can implement the following:

- 4:1 multiplexer in one slice
- 8:1 multiplexer in two slices
- 16:1 multiplexer in one CLB element (4 slices)
- 32:1 multiplexer in two CLB elements (8 slices)

Each Virtex-II slice has one MUXF5 multiplexer and one MUXFX multiplexer. The MUXFX multiplexer implements the MUXF6, MUXF7, or MUXF8, as shown in Figure 23. Each CLB element has two MUXF6 multiplexers, one MUXF7 multiplexer and one MUXF8 multiplexer. Examples of multiplexers are shown in the *Virtex-II Platform FPGA User Guide*. Any LUT can implement a 2:1 multiplexer.

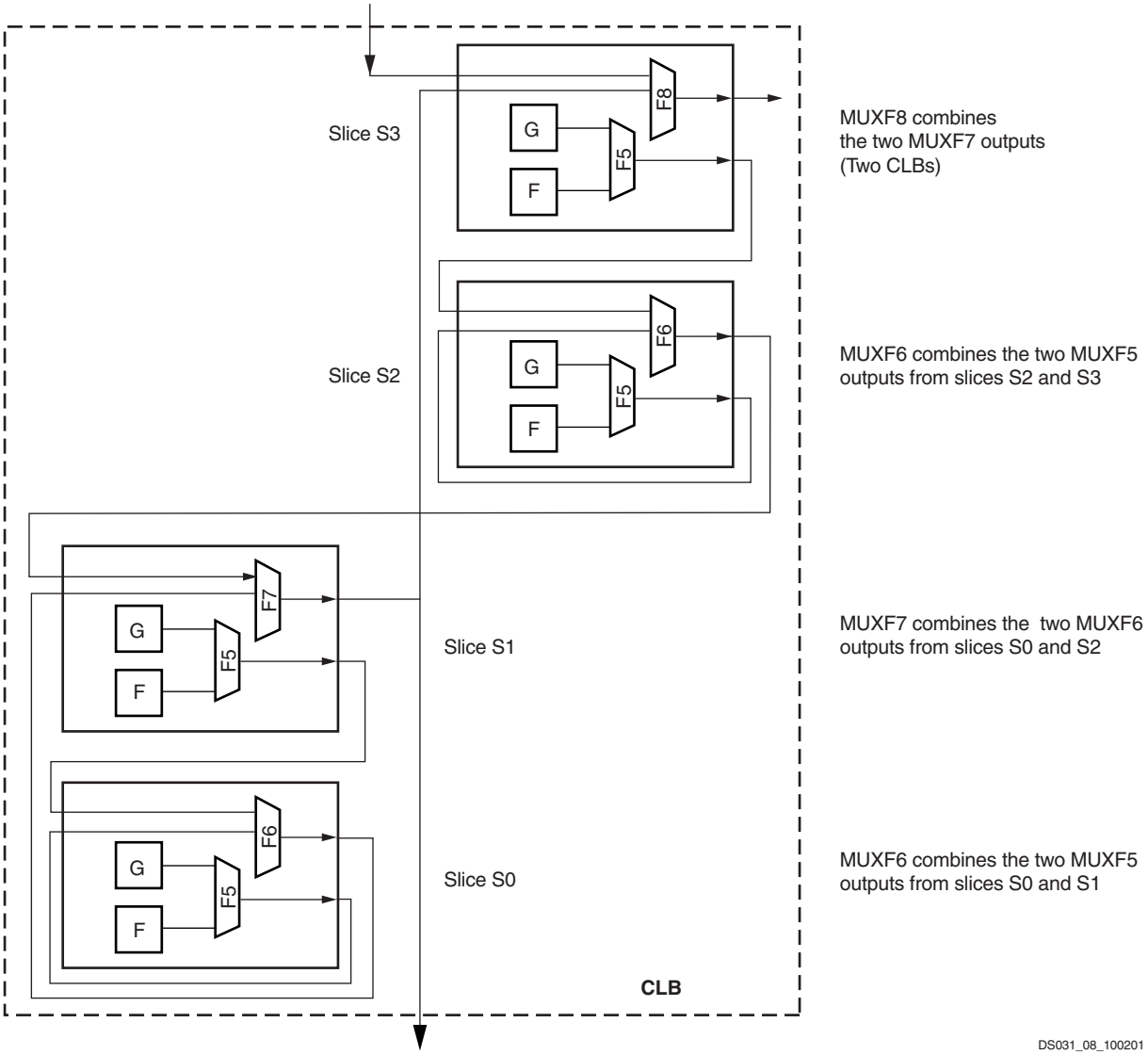


Figure 23: **MUXF5 and MUXFX multiplexers**

Fast Lookahead Carry Logic

Dedicated carry logic provides fast arithmetic addition and subtraction. The Virtex-II CLB has two separate carry chains, as shown in the Figure 24.

The height of the carry chains is two bits per slice. The carry chain in the Virtex-II device is running upward. The dedicated carry path and carry multiplexer (MUXCY) can also be used to cascade function generators for implementing wide logic functions.

Arithmetic Logic

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND (MULT_AND) gate (shown in Figure 16) improves the efficiency of multiplier implementation.

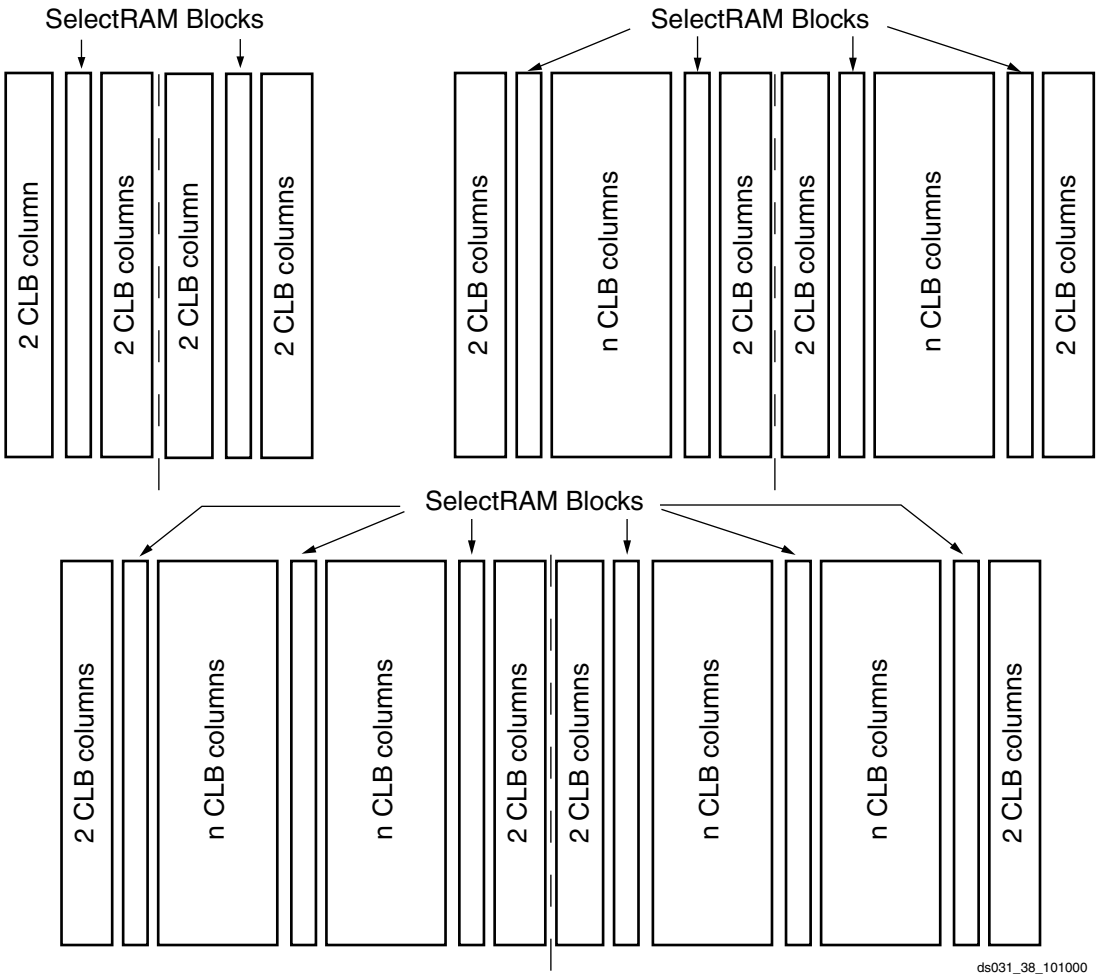


Figure 34: **Block SelectRAM (2-column, 4-column, and 6-column)**

Total Amount of SelectRAM Memory

Table 19 shows the amount of block SelectRAM memory available for each Virtex-II device. The 18 Kbit SelectRAM blocks are cascadable to implement deeper or wider single- or dual-port memory resources.

Table 19: **Virtex-II SelectRAM Memory Available**

Device	Total SelectRAM Memory		
	Blocks	in Kbits	in Bits
XC2V40	4	72	73,728
XC2V80	8	144	147,456
XC2V250	24	432	442,368
XC2V500	32	576	589,824
XC2V1000	40	720	737,280
XC2V1500	48	864	884,736
XC2V2000	56	1,008	1,032,192
XC2V3000	96	1,728	1,769,472
XC2V4000	120	2,160	2,211,840
XC2V6000	144	2,592	2,654,208
XC2V8000	168	3,024	3,096,576

18-Bit x 18-Bit Multipliers

Introduction

A Virtex-II multiplier block is an 18-bit by 18-bit 2's complement signed multiplier. Virtex-II devices incorporate many embedded multiplier blocks. These multipliers can be associated with an 18 Kbit block SelectRAM resource or can be used independently. They are optimized for high-speed operations and have a lower power consumption compared to an 18-bit x 18-bit multiplier in slices.

Table 6: **DC Input and Output Levels *(Continued)***

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.6	V_{REF} + 0.6	8	– 8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	V_{REF} – 0.8	V_{REF} + 0.8	16	– 16
SSTL2 I	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.65	V_{REF} + 0.65	7.6	– 7.6
SSTL2 II	– 0.5	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.5	V_{REF} – 0.80	V_{REF} + 0.80	15.2	– 15.2
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested. The DONE pin is always LVTTL 12 mA.
2. Tested according to the relevant specifications.
3. LVTTL and LVCMOS inputs have approximately 100 mV of hysteresis.

LDT Differential Signal DC Specifications (LDT_25)

Table 7: **LDT DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Voltage	V_{OD}	R_T = 100 Ω across Q and $\overline{Q}$ signals	500	600	700	mV
Change in V_{OD} Magnitude	ΔV_{OD}		–15		15	mV
Output Common Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	560	600	640	mV
Change in V_{OS} Magnitude	ΔV_{OCM}		–15		15	mV
Input Differential Voltage	V_{ID}		200	600	1000	mV
Change in V_{ID} Magnitude	ΔV_{ID}		–15		15	mV
Input Common Mode Voltage	V_{ICM}		500	600	700	mV
Change in V_{ICM} Magnitude	ΔV_{ICM}		–15		15	mV

LVDS DC Specifications (LVDS_33 & LVDS_25)

Table 8: **LVDS DC Specifications**

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals			1.575	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.925			V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	400	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.2	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	V_{CCO} – 0.5	V

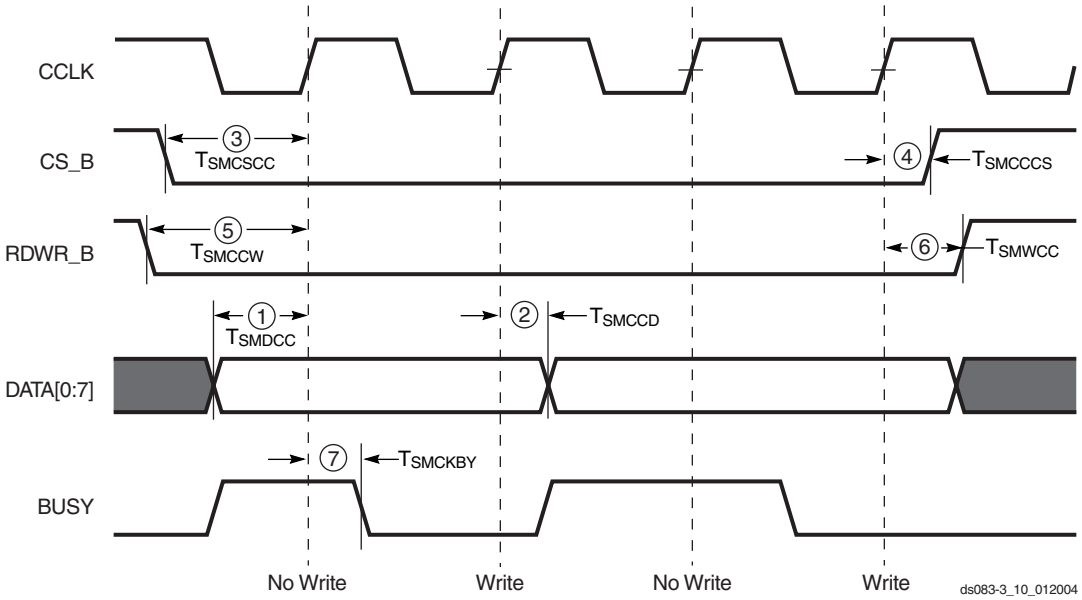


Figure 5: **SelectMAP Mode Data Loading Sequence (Generic)**

Table 32: **SelectMAP Mode Write Timing Characteristics**

	Description	Figure References	Symbol	Value	Units
CCLK	DATA[0:7] setup/hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	CS_B setup/hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	RDWR_B setup/hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY propagation delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum start-up frequency		$F_{CC\_STARTUP}$	50	MHz, max
	Maximum frequency		$F_{CC\_SELECTMAP}$	50	MHz, max
	Maximum frequency with no handshake		F_{CCNH}	50	MHz, max

Date	Version	Revision
08/01/03	3.0	• Table 13: All Virtex-II devices and speed grades now Production. • Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.116**. • Table 34 and Table 35: Revised test setup footnote to refer to Figure 1. Previously specified a capacitive load parameter. • Figure 1: Added note to figure regarding termination resistors.
10/14/03	3.1	• Table 1: Changed T_J description from “Operating junction temperature” to “Maximum junction temperature”. • In section General Power Supply Requirements, replaced reference to Answer Record 11713 with reference to **XAPP689** regarding handling of simultaneously switching outputs (SSO). • In section I/O Standard Adjustment Measurement Methodology: - Table 18 renamed Input Delay Measurement Methodology. Added footnotes. - Added new Table 19, Output Delay Measurement Methodology. - Replaced Figure 1, Generalized Test Setup, with new drawing. - Revised and extended text describing output delay measurement procedure. • Table 45, Table 47, and Table 48: All Source-Synchronous parameters for all devices now available in these tables. • XC2V8000 is no longer offered in the -6 speed grade. The following tables containing parameters or other references to this device/grade combination were corrected accordingly: Table 13, Table 14, Table 34, Table 35, Table 36, Table 37, Table 45, Table 47, and Table 48. • Table 39: For Input Clock Low/High Pulse Width, PSCLK and CLKIN, changed existing Footnote (2) to new Footnote (3).
03/29/04	3.2	• Table 4: - For XC2V40, added Maximum quiescent supply current specifications. - For all devices, updated Typical specifications for I_{CCINTQ} and I_{CCAUXQ}. • Section Power-On Power Supply Requirements, page 3: Added Footnote (1) qualifying statement that power supplies can be turned on in any sequence. • Added section Configuration Timing, page 27. This section includes new timing diagrams as well as parameter specification tables formerly included in the **Virtex-II Platform FPGA User Guide**. • Table 20, Clock Distribution Switching Characteristics: Added parameter T_{GSI}/T_{GIS} (Global Clock Buffer S Input Setup/Hold to I1 and I2 Inputs). • Table 38, Operating Frequency Ranges: Added Footnote (4) to all four CLKIN parameters. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1: Added T_{SOL} parameters for Pb-free package devices.
03/01/05	3.4	• Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from **speedsfile version 1.120**. • Table 2: Corrected Footnote (1) to require connecting V_{BATT} to V_{CCAUX} or GND if battery is not used. • Table 3: Corrected "V_{REF} current per bank" to "V_{REF} current per pin." • Section Power-On Power Supply Requirements: Added word “monotonically” to description of supply voltage ramp-on requirements. Added sentence to footnote (1) indicating that if the stated requirements are violated, no damage to the device will result, but configuration will probably fail. • Figure 3 and Figure 4: Corrected to show DOUT transitions driven by falling edge of CCLK.

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	VCCINT	R16		
NA	VCCINT	R7		
NA	VCCINT	H16		
NA	VCCINT	H7		
NA	VCCINT	G16		
NA	VCCINT	G15		
NA	VCCINT	G8		
NA	VCCINT	G7		
NA	VCCINT	F17		
NA	VCCINT	F6		
NA	GND	AB22		
NA	GND	AB1		
NA	GND	AA21		
NA	GND	AA2		
NA	GND	Y20		
NA	GND	Y3		
NA	GND	W19		
NA	GND	W4		
NA	GND	P14		
NA	GND	P13		
NA	GND	P12		
NA	GND	P11		
NA	GND	P10		
NA	GND	P9		
NA	GND	N14		
NA	GND	N13		
NA	GND	N12		
NA	GND	N11		
NA	GND	N10		
NA	GND	N9		
NA	GND	M14		
NA	GND	M13		
NA	GND	M12		
NA	GND	M11		

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
3	IO_L46P_3	Y26		
3	IO_L45N_3/VREF_3	U20		
3	IO_L45P_3	V20		
3	IO_L43N_3	W25		
3	IO_L43P_3	W24		
3	IO_L25N_3	V21	NC	NC
3	IO_L25P_3	W21	NC	NC
3	IO_L24N_3	AA26		
3	IO_L24P_3	AA25		
3	IO_L22N_3	Y24		
3	IO_L22P_3	Y23		
3	IO_L21N_3/VREF_3	W22		
3	IO_L21P_3	W23		
3	IO_L19N_3	AB26		
3	IO_L19P_3	AB25		
3	IO_L06N_3	AC26		
3	IO_L06P_3	AC25		
3	IO_L04N_3	AD26		
3	IO_L04P_3	AD25		
3	IO_L03N_3/VREF_3	AA24		
3	IO_L03P_3	AA23		
3	IO_L02N_3/VRP_3	AB24		
3	IO_L02P_3/VRN_3	AB23		
3	IO_L01N_3	Y22		
3	IO_L01P_3	AA22		
4	IO_L01N_4/BUSY/DOUT(1)	AD21		
4	IO_L01P_4/INIT_B	AC21		
4	IO_L02N_4/D0/DIN(1)	Y20		
4	IO_L02P_4/D1	Y19		
4	IO_L03N_4/D2/ALT_VRP_4	AA20		
4	IO_L03P_4/D3/ALT_VRN_4	AB20		
4	IO_L04N_4/VREF_4	AC22		
4	IO_L04P_4	AE21		
4	IO_L05N_4/VRP_4	AE26		
4	IO_L05P_4/VRN_4	AF25		
4	IO_L06N_4	W20		

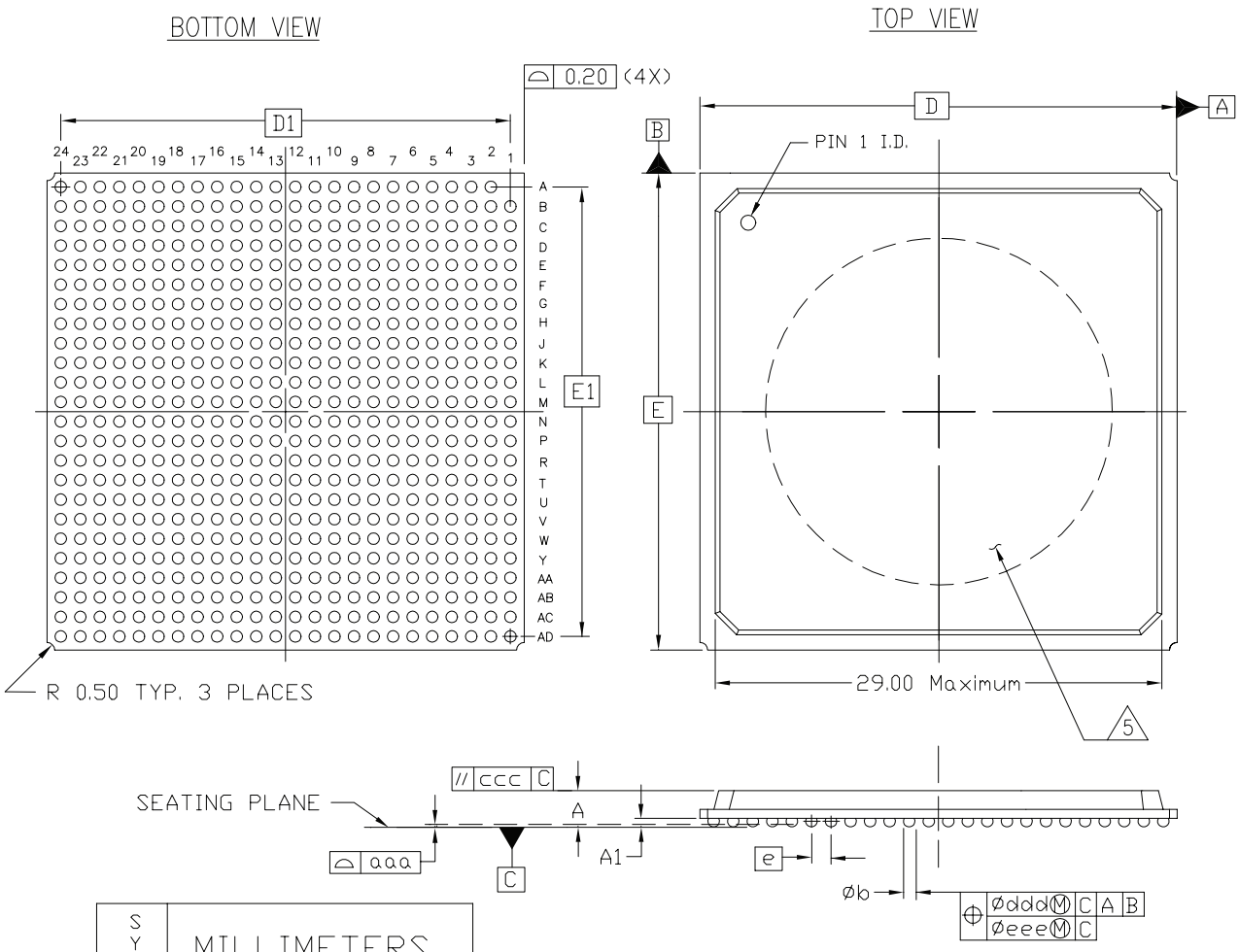
Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
6	IO_L52N_6	U1		
6	IO_L54P_6	U7		
6	IO_L54N_6	T7		
6	IO_L67P_6	U4		
6	IO_L67N_6	U3		
6	IO_L69P_6	U6		
6	IO_L69N_6/VREF_6	U5		
6	IO_L70P_6	T5		
6	IO_L70N_6	T6		
6	IO_L72P_6	T8		
6	IO_L72N_6	R8		
6	IO_L73P_6	T2	NC	
6	IO_L73N_6	T1	NC	
6	IO_L75P_6	T4	NC	
6	IO_L75N_6/VREF_6	T3	NC	
6	IO_L76P_6	R6	NC	
6	IO_L76N_6	R5	NC	
6	IO_L78P_6	R4	NC	
6	IO_L78N_6	R3	NC	
6	IO_L91P_6	R2		
6	IO_L91N_6	R1		
6	IO_L93P_6	R7		
6	IO_L93N_6/VREF_6	P7		
6	IO_L94P_6	P6		
6	IO_L94N_6	P5		
6	IO_L96P_6	P4		
6	IO_L96N_6	P3		
7	IO_L96P_7	P1		
7	IO_L96N_7	N1		
7	IO_L94P_7	N4		
7	IO_L94N_7	N5		
7	IO_L93P_7/VREF_7	N6		
7	IO_L93N_7	N7		
7	IO_L91P_7	P8		
7	IO_L91N_7	N8		
7	IO_L78P_7	M1	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
7	IO_L78N_7	M2	NC	
7	IO_L76P_7	M5	NC	
7	IO_L76N_7	M6	NC	
7	IO_L75P_7/VREF_7	M3	NC	
7	IO_L75N_7	M4	NC	
7	IO_L73P_7	M7	NC	
7	IO_L73N_7	M8	NC	
7	IO_L72P_7	L1		
7	IO_L72N_7	L2		
7	IO_L70P_7	L5		
7	IO_L70N_7	L6		
7	IO_L69P_7/VREF_7	L3		
7	IO_L69N_7	L4		
7	IO_L67P_7	K1		
7	IO_L67N_7	J1		
7	IO_L54P_7	K3		
7	IO_L54N_7	K4		
7	IO_L52P_7	K5		
7	IO_L52N_7	K6		
7	IO_L51P_7/VREF_7	L8		
7	IO_L51N_7	L7		
7	IO_L49P_7	J2		
7	IO_L49N_7	H1		
7	IO_L48P_7	J3		
7	IO_L48N_7	J4		
7	IO_L46P_7	J5		
7	IO_L46N_7	J6		
7	IO_L45P_7/VREF_7	H5		
7	IO_L45N_7	H4		
7	IO_L43P_7	K7		
7	IO_L43N_7	J7		
7	IO_L25P_7	H2	NC	NC
7	IO_L25N_7	H3	NC	NC
7	IO_L24P_7	G1		
7	IO_L24N_7	F1		
7	IO_L22P_7	G3		
7	IO_L22N_7	G4		

BG575/BGG575 Standard BGA Package Specifications (1.27mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A		2.33	2.60
A_1	0.50	0.60	0.70
D/E	31.00 BSC		
D_1/E_1	29.21 REF		
e	1.27BSC		
Øb	0.60	0.75	0.90
aaa			0.20
ccc			0.35
ddd			0.30
eee			0.15
M	24		

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-BAN-1 (DEPOPULATED)
4. NO SOLDER BALL AND LAND ON A1.

5 HEAT SINK OPTION

575-BALL MOLDED BGA (BG575/BGG575)

Figure 5: **BG575/BGG575 Standard BGA Package Specifications**

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L19P_2	F26
2	IO_L21N_2	F27
2	IO_L21P_2/VREF_2	G27
2	IO_L22N_2	G23
2	IO_L22P_2	H23
2	IO_L24N_2	G25
2	IO_L24P_2	G26
2	IO_L25N_2	H21
2	IO_L25P_2	J21
2	IO_L27N_2	H22
2	IO_L27P_2/VREF_2	J22
2	IO_L28N_2	H24
2	IO_L28P_2	H25
2	IO_L30N_2	H27
2	IO_L30P_2	J27
2	IO_L43N_2	J23
2	IO_L43P_2	J24
2	IO_L45N_2	J25
2	IO_L45P_2/VREF_2	J26
2	IO_L46N_2	K20
2	IO_L46P_2	K21
2	IO_L48N_2	K22
2	IO_L48P_2	K23
2	IO_L49N_2	K24
2	IO_L49P_2	K25
2	IO_L51N_2	K26
2	IO_L51P_2/VREF_2	K27
2	IO_L52N_2	L20
2	IO_L52P_2	M20
2	IO_L54N_2	L21
2	IO_L54P_2	L22
2	IO_L67N_2	L24
2	IO_L67P_2	L25
2	IO_L69N_2	L26
2	IO_L69P_2/VREF_2	L27
2	IO_L70N_2	M19

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
6	IO_L68N_6	Y26	NC	
6	IO_L69P_6	AA30	NC	
6	IO_L69N_6/VREF_6	Y30	NC	
6	IO_L70P_6	W24	NC	
6	IO_L70N_6	V24	NC	
6	IO_L71P_6	Y27	NC	
6	IO_L71N_6	W27	NC	
6	IO_L72P_6	W28	NC	
6	IO_L72N_6	Y28	NC	
6	IO_L73P_6	V25	NC	NC
6	IO_L73N_6	U25	NC	NC
6	IO_L74P_6	V26	NC	NC
6	IO_L74N_6	V27	NC	NC
6	IO_L75P_6	Y29	NC	NC
6	IO_L75N_6/VREF_6	W29	NC	NC
6	IO_L76P_6	U22	NC	NC
6	IO_L76N_6	T22	NC	NC
6	IO_L77P_6	U26	NC	NC
6	IO_L77N_6	T26	NC	NC
6	IO_L78P_6	V30	NC	NC
6	IO_L78N_6	W30	NC	NC
6	IO_L91P_6	U23		
6	IO_L91N_6	T23		
6	IO_L92P_6	U27		
6	IO_L92N_6	T27		
6	IO_L93P_6	V29		
6	IO_L93N_6/VREF_6	U29		
6	IO_L94P_6	T24		
6	IO_L94N_6	T25		
6	IO_L95P_6	U28		
6	IO_L95N_6	T28		
6	IO_L96P_6	T30		
6	IO_L96N_6	U30		
7	IO_L96P_7	P28		
7	IO_L96N_7	R28		
7	IO_L95P_7	R25		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L77N_0	J20	
0	IO_L77P_0	K19	
0	IO_L78N_0	D20	
0	IO_L78P_0	D21	
0	IO_L79N_0	A21	NC
0	IO_L79P_0	A22	NC
0	IO_L80N_0	L19	NC
0	IO_L80P_0	L18	NC
0	IO_L81N_0	B19	NC
0	IO_L81P_0/VREF_0	A20	NC
0	IO_L82N_0	A18	NC
0	IO_L82P_0	B18	NC
0	IO_L83N_0	H19	NC
0	IO_L83P_0	H18	NC
0	IO_L84N_0	C20	NC
0	IO_L84P_0	C21	NC
0	IO_L91N_0/VREF_0	D19	
0	IO_L91P_0	D18	
0	IO_L92N_0	G18	
0	IO_L92P_0	G19	
0	IO_L93N_0	F18	
0	IO_L93P_0	F19	
0	IO_L94N_0/VREF_0	C19	
0	IO_L94P_0	C18	
0	IO_L95N_0/GCLK7P	K18	
0	IO_L95P_0/GCLK6S	J18	
0	IO_L96N_0/GCLK5P	E19	
0	IO_L96P_0/GCLK4S	E18	
1	IO_L96N_1/GCLK3P	E17	
1	IO_L96P_1/GCLK2S	E16	
1	IO_L95N_1/GCLK1P	H17	
1	IO_L95P_1/GCLK0S	H16	
1	IO_L94N_1	D17	
1	IO_L94P_1/VREF_1	D16	
1	IO_L93N_1	F16	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L45N_7	J34	
7	IO_L44P_7	M27	
7	IO_L44N_7	L27	
7	IO_L43P_7	H31	
7	IO_L43N_7	J31	
7	IO_L30P_7	F32	
7	IO_L30N_7	G32	
7	IO_L29P_7	N25	
7	IO_L29N_7	M25	
7	IO_L28P_7	F34	
7	IO_L28N_7	G34	
7	IO_L27P_7/VREF_7	J30	
7	IO_L27N_7	H30	
7	IO_L26P_7	K28	
7	IO_L26N_7	L28	
7	IO_L25P_7	H28	
7	IO_L25N_7	J29	
7	IO_L24P_7	G29	
7	IO_L24N_7	H29	
7	IO_L23P_7	L26	
7	IO_L23N_7	K26	
7	IO_L22P_7	F33	
7	IO_L22N_7	G33	
7	IO_L21P_7/VREF_7	J28	
7	IO_L21N_7	J27	
7	IO_L20P_7	K27	
7	IO_L20N_7	J26	
7	IO_L19P_7	E31	
7	IO_L19N_7	F31	
7	IO_L06P_7	D32	
7	IO_L06N_7	E32	
7	IO_L05P_7	L25	
7	IO_L05N_7	K24	
7	IO_L04P_7	D34	
7	IO_L04N_7	E34	
7	IO_L03P_7/VREF_7	G30	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
NA	VCCINT	AB17	
NA	VCCINT	AB16	
NA	VCCINT	AB15	
NA	VCCINT	AB14	
NA	VCCINT	AB13	
NA	VCCINT	AA22	
NA	VCCINT	AA13	
NA	VCCINT	Y22	
NA	VCCINT	Y13	
NA	VCCINT	W22	
NA	VCCINT	W13	
NA	VCCINT	V22	
NA	VCCINT	V13	
NA	VCCINT	U22	
NA	VCCINT	U13	
NA	VCCINT	T22	
NA	VCCINT	T13	
NA	VCCINT	R22	
NA	VCCINT	R13	
NA	VCCINT	P22	
NA	VCCINT	P13	
NA	VCCINT	N22	
NA	VCCINT	N21	
NA	VCCINT	N20	
NA	VCCINT	N19	
NA	VCCINT	N18	
NA	VCCINT	N17	
NA	VCCINT	N16	
NA	VCCINT	N15	
NA	VCCINT	N14	
NA	VCCINT	N13	
NA	VCCINT	M23	
NA	VCCINT	M12	
NA	VCCINT	L24	
NA	VCCINT	L11	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
3	IO_L10N_3	AK7	NC	
3	IO_L10P_3	AL7	NC	
3	IO_L09N_3/VREF_3	AK11	NC	
3	IO_L09P_3	AJ10	NC	
3	IO_L08N_3	AR1	NC	
3	IO_L08P_3	AT1	NC	
3	IO_L07N_3	AM5	NC	
3	IO_L07P_3	AN5	NC	
3	IO_L06N_3	AM7		
3	IO_L06P_3	AL8		
3	IO_L05N_3	AP3		
3	IO_L05P_3	AP4		
3	IO_L04N_3	AM6		
3	IO_L04P_3	AN6		
3	IO_L03N_3/VREF_3	AJ13		
3	IO_L03P_3	AH13		
3	IO_L02N_3/VRP_3	AR3		
3	IO_L02P_3/VRN_3	AT2		
3	IO_L01N_3	AP5		
3	IO_L01P_3	AR4		
4	IO_L01N_4/BUSY/DOUT(1)	AV4		
4	IO_L01P_4/INIT_B	AU4		
4	IO_L02N_4/D0/DIN(1)	AM9		
4	IO_L02P_4/D1	AM10		
4	IO_L03N_4/D2/ALT_VRP_4	AT6		
4	IO_L03P_4/D3/ALT_VRN_4	AR6		
4	IO_L04N_4/VREF_4	AU6		
4	IO_L04P_4	AU5		
4	IO_L05N_4/VRP_4	AL10		
4	IO_L05P_4/VRN_4	AL11		
4	IO_L06N_4	AR8		
4	IO_L06P_4	AR7		
4	IO_L07N_4	AW5	NC	
4	IO_L07P_4	AW4	NC	
4	IO_L08N_4	AK12	NC	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
4	IO_L68P_4	AL17		
4	IO_L69N_4	AT16		
4	IO_L69P_4/VREF_4	AT15		
4	IO_L70N_4	AU14		
4	IO_L70P_4	AU13		
4	IO_L71N_4	AH18		
4	IO_L71P_4	AH19		
4	IO_L72N_4	AN17		
4	IO_L72P_4	AN16		
4	IO_L73N_4	AW15		
4	IO_L73P_4	AW14		
4	IO_L74N_4	AJ18		
4	IO_L74P_4	AJ19		
4	IO_L75N_4	AP17		
4	IO_L75P_4/VREF_4	AP16		
4	IO_L76N_4	AV15		
4	IO_L76P_4	AU15		
4	IO_L77N_4	AK18		
4	IO_L77P_4	AK19		
4	IO_L78N_4	AR18		
4	IO_L78P_4	AR17		
4	IO_L79N_4	AU17		
4	IO_L79P_4	AU16		
4	IO_L80N_4	AL18		
4	IO_L80P_4	AL19		
4	IO_L81N_4	AN19		
4	IO_L81P_4/VREF_4	AN18		
4	IO_L82N_4	AV17		
4	IO_L82P_4	AV16		
4	IO_L83N_4	AM18		
4	IO_L83P_4	AM19		
4	IO_L84N_4	AP19		
4	IO_L84P_4	AP18		
4	IO_L85N_4	AW17	NC	NC
4	IO_L85P_4	AW16	NC	NC
4	IO_L91N_4/VREF_4	AV19		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	Y17		
NA	GND	Y16		
NA	GND	Y10		
NA	GND	Y7		
NA	GND	Y4		
NA	GND	Y1		
NA	GND	W24		
NA	GND	W23		
NA	GND	W22		
NA	GND	W21		
NA	GND	W20		
NA	GND	W19		
NA	GND	W18		
NA	GND	W17		
NA	GND	W16		
NA	GND	V24		
NA	GND	V23		
NA	GND	V22		
NA	GND	V21		
NA	GND	V20		
NA	GND	V19		
NA	GND	V18		
NA	GND	V17		
NA	GND	V16		
NA	GND	U36		
NA	GND	U32		
NA	GND	U24		
NA	GND	U23		
NA	GND	U22		
NA	GND	U21		
NA	GND	U20		
NA	GND	U19		
NA	GND	U18		
NA	GND	U17		
NA	GND	U16		
NA	GND	U8		

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)