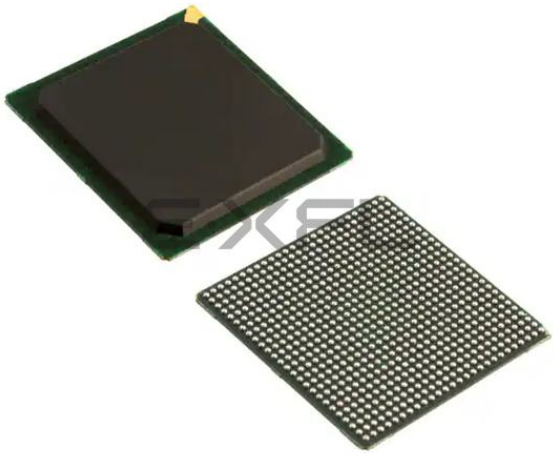

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2688
Number of Logic Elements/Cells	-
Total RAM Bits	1032192
Number of I/O	456
Number of Gates	2000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v2000-5fgg676c

ments to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the Virtex-II *Platform FPGA User Guide.*

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II Platform FPGA User Guide*. For devices that support this feature, please contact your sales representative for specific ordering part number.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). A note was added to Table 1.
04/02/01	1.5	• Under Input/Output Individual Options, the range of values for optional pull-up and pull-down resistors was changed to 10 - 60 KΩ from 50 - 100 KΩ. • Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	• Added Table 6. • Changed definition of multiply and divide integer ranges under Digital Clock Manager (DCM). • Made numerous minor edits throughout this module.
10/02/01	1.7	• Updated descriptions under Digitally Controlled Impedance (DCI), Global Clock Multiplexer Buffers, Digital Clock Manager (DCM), and Creating a Design.
10/12/01	1.8	• Made clarifying edits under Digital Clock Manager (DCM).
11/29/01	1.9	• Changed bitstream lengths for each device in Table 26.

Date	Version	Revision
07/16/02	2.0	• Updated compatible input standards listed in Table 6.
09/26/02	2.1	• Changed number of resources available to the XC2V40 device in Table 13. • Clarified Power On Reset information under Configuration Sequence.
12/06/02	2.1.1	• Cosmetic edits.
05/07/03	2.1.2	• Added qualification note to Figure 13, page 11. • Corrected sentence in section Input/Output Individual Options, page 4, to read “The optional weak-keeper circuit is connected to each *user I/O pad*.” • Corrected typographical errors in Table 3 for names of HSTL_[x]_DCI_18 standards.
06/19/03	2.2	• Removed Compatible Output Standards and Compatible Input Standards tables. • Added new Table 5, Summary of Voltage Supply Requirements for All Input and Output Standards. This table replaces deleted I/O standards tables. • Added section Rules for Combining I/O Standards in the Same Bank, page 6.
08/01/03	3.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
10/14/03	3.1	• Added section Local Clocking, page 29. • Table 1, page 1: - Added SSTL18_I and SSTL18_II. - Corrected names of 1.8V HSTL_I-IV standards to “HSTL_I-IV_18”. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. - Changed “N/A” to “N/R” (no requirement). • Table 2, page 2: - Changed “N/A” to “N/R” (no requirement). • Table 3, page 2: - Added SSTL18_I_DCI, SSTL18_II_DCI, LVDS_33_DCI, LVDSEXT_33_DCI, LVDS_25_DCI, and LVDSEXT_25_DCI. - Corrected Input V_{REF} for HSTL_III-IV_18 from 1.08V to 1.1V. • Sections Slave-Serial Mode and Master-Serial Mode, page 36: Changed "rising" to "falling" edge with respect to DOUT. • Added verbiage to section Bitstream Encryption, page 38: “For devices that support this feature, please contact your sales representative for specific ordering part number.”
03/29/04	3.2	• Table 2, page 2, and Table 5, page 7: Removed LVDS_33_DCI and LVDSEXT_33_DCI from tables. • Table 26, page 37: Updated bitstream lengths. • Section BUFGMUX, page 29: Corrected the definition of the "presently selected clock" to be I0 or I1. Corrected signal names in Figure 44 and associated text from CLK0 and CLK1 to I0 and I1. • Recompiled for backward compatibility with Acrobat 4 and above.
06/24/04	3.3	• Table 1, page 1: Added example to Footnote (1) regarding V_{CCO} rules for GTL and GTLP. • Added reference to Pb-free package types in Figure 7, page 6.
03/01/05	3.4	• Reassigned heading hierarchies for better agreement with content. • Table 2: Corrected V_{OD} output voltages. • Table 26: Updated bitstream lengths.
11/05/07	3.5	• Updated copyright statement and legal disclaimer. • Boundary-Scan (JTAG, IEEE 1532) Mode, page 37: Updated IEEE 1149.1 compliance statement.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

Table 5: **Minimum Power On Current Required for Virtex-II Devices**

	Device (mA)							
	XC2V40, XC2V80, XC2V250, XC2V500	XC2V1000	XC2V1500	XC2V2000	XC2V3000	XC2V4000	XC2V6000	XC2V8000
$I_{CCINTMIN}$	200	250	350	400	500	650	800	1100
$I_{CCAUXMIN}$	100	100	100	100	100	100	100	100
I_{CCOMIN}	50	50	100	100	100	100	100	100

Notes:
1. Values specified for power on current parameters are Commercial Grade. For Industrial Grade values, multiply Commercial Grade values by 1.25.
2. I_{CCOMIN} values listed here apply to the entire device (all banks).

General Power Supply Requirements

Proper decoupling of all FPGA power supplies is sessential. Consult Xilinx Application Note **XAPP623** for detailed information on power distribution system design.

V_{CCAUX} powers critical resources in the FPGA. Thus, V_{CCAUX} is especially susceptible to power supply noise.

Changes in V_{CCAUX} voltage outside of 200 mV peak to peak should take place at a rate no faster than 10 mV per millisecond. Techniques to help reduce jitter and period distortion are provided in Xilinx Answer Record 13756, available at **www.support.xilinx.com**.

V_{CCAUX} can share a power plane with 3.3V V_{CCO}, but only if V_{CCO} does not have excessive noise. Using simultaneously switching output (SSO) limits are essential for keeping power supply noise to a minimum. Refer to **XAPP689**, "Managing Ground Bounce in Large FPGAs," to determine the number of simultaneously switching outputs allowed per bank at the package level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 6: **DC Input and Output Levels**

Input/Output	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS33	– 0.5	0.8	2.0	3.6	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS25	– 0.5	0.7	1.7	2.7	0.4	V_{CCO} – 0.4	24	– 24
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	16	– 16
LVCMOS15	– 0.5	35% V_{CCO}	65% V_{CCO}	1.7	0.4	V_{CCO} – 0.4	16	– 16
PCI33_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI66_3	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI–X	– 0.5	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2
GTLP	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.6	n/a	36	n/a
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	V_{CCO} + 0.5	0.4	n/a	40	n/a
HSTL I	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	8	– 8
HSTL II	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	16	– 16
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	24	– 8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.5	0.4	V_{CCO} – 0.4	48	– 8

Virtex-II Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-II devices. The numbers reported here are worst-case values; they have all been fully characterized. Note that these values are subject to the same guidelines as Virtex-II Switching Characteristics, page 9 (speed files).

Table 11 provides pin-to-pin values (in nanoseconds) including IOB delays; that is, delay through the device from input pin to output pin. In the case of multiple inputs and outputs, the worst delay is reported.

Table 11: **Pin-to-Pin Performance**

Description	Device Used & Speed Grade	Pin-to-Pin (with I/O delays)	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	6.3	ns
32-bit Address Decoder	XC2V1000 -5	7.7	ns
64-bit Address Decoder	XC2V1000 -5	9.3	ns
4:1 MUX	XC2V1000 -5	5.7	ns
8:1 MUX	XC2V1000 -5	6.5	ns
16:1 MUX	XC2V1000 -5	6.7	ns
32:1 MUX	XC2V1000 -5	8.7	ns
Combinatorial (pad to LUT to pad)	XC2V1000 -5	5.0	ns
Memory			
Block RAM			
Pad to setup		1.6	ns
Clock to Pad		9.5	ns
Distributed RAM			
Pad to setup	XC2V1000 -5	2.7	ns
Clock to Pad	XC2V1000 -5	5.1 (no clk skew)	ns

Table 12 shows internal (register-to-register) performance. Values are reported in MHz.

Table 12: **Register-to-Register Performance**

Description	Device Used & Speed Grade	Register-to-Register Performance	Units
Basic Functions			
16-bit Address Decoder	XC2V1000 -5	398	MHz
32-bit Address Decoder	XC2V1000 -5	291	MHz
64-bit Address Decoder	XC2V1000 -5	274	MHz
4:1 MUX	XC2V1000 -5	563	MHz
8:1 MUX	XC2V1000 -5	454	MHz
16:1 MUX	XC2V1000 -5	414	MHz
32:1 MUX	XC2V1000 -5	323	MHz
Register to LUT to Register	XC2V1000 -5	613	MHz

Table 19: **Output Delay Measurement Methodology**

Description	IOSTANDARD Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
SSTL, Class I, 3.3V	SSTL3_I	50	0	V_{REF}	1.5
SSTL, Class II, 3.3V	SSTL3_II	25	0	V_{REF}	1.5
AGP-2X/AGP (Accelerated Graphics Port)	AGP-2X/AGP (rising edge)	50	0	0.94	0
	AGP-2X/AGP (falling edge)	50	0	2.03	3.3
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V_{REF}	1.2
LVDS, 3.3V	LVDSEXT_25	50	0	V_{REF}	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_33	50	0	V_{REF}	1.2
LVDSEXT, 3.3V	LVDSEXT_33	50	0	V_{REF}	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V_{REF}	0.6
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 3.3V	LVPECL_33	1M	0	1.23	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
SSTL, Class I & II, 3.3V, with DCI	SSTL3_I_DCI, SSTL3_II_DCI	50	0	V_{REF}	1.5
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:
1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.

Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	$T_{MULTCK1\_P35}$	3.05	3.25	3.74	ns, Max
Clock to Pin 34	$T_{MULTCK1\_P34}$	2.95	3.14	3.61	ns, Max
Clock to Pin 33	$T_{MULTCK1\_P33}$	2.85	3.04	3.49	ns, Max
Clock to Pin 32	$T_{MULTCK1\_P32}$	2.76	2.93	3.37	ns, Max
Clock to Pin 31	$T_{MULTCK1\_P31}$	2.66	2.82	3.25	ns, Max
Clock to Pin 30	$T_{MULTCK1\_P30}$	2.56	2.72	3.12	ns, Max
Clock to Pin 29	$T_{MULTCK1\_P29}$	2.47	2.61	3.00	ns, Max
Clock to Pin 28	$T_{MULTCK1\_P28}$	2.37	2.50	2.88	ns, Max
Clock to Pin 27	$T_{MULTCK1\_P27}$	2.27	2.40	2.75	ns, Max
Clock to Pin 26	$T_{MULTCK1\_P26}$	2.17	2.29	2.63	ns, Max
Clock to Pin 25	$T_{MULTCK1\_P25}$	2.08	2.18	2.51	ns, Max
Clock to Pin 24	$T_{MULTCK1\_P24}$	1.98	2.07	2.38	ns, Max
Clock to Pin 23	$T_{MULTCK1\_P23}$	1.88	1.97	2.26	ns, Max
Clock to Pin 22	$T_{MULTCK1\_P22}$	1.79	1.86	2.14	ns, Max
Clock to Pin 21	$T_{MULTCK1\_P21}$	1.69	1.75	2.02	ns, Max
Clock to Pin 20	$T_{MULTCK1\_P20}$	1.59	1.65	1.89	ns, Max
Clock to Pin 19	$T_{MULTCK1\_P19}$	1.50	1.54	1.77	ns, Max
Clock to Pin 18	$T_{MULTCK1\_P18}$	1.40	1.43	1.65	ns, Max
Clock to Pin 17	$T_{MULTCK1\_P17}$	1.30	1.33	1.52	ns, Max
Clock to Pin 16	$T_{MULTCK1\_P16}$	1.20	1.22	1.40	ns, Max
Clock to Pin 15	$T_{MULTCK1\_P15}$	1.11	1.11	1.28	ns, Max
Clock to Pin 14	$T_{MULTCK1\_P14}$	1.01	1.00	1.15	ns, Max
Clock to Pin 13	$T_{MULTCK1\_P13}$	0.91	1.00	1.15	ns, Max
Clock to Pin 12	$T_{MULTCK1\_P12}$	0.91	1.00	1.15	ns, Max
Clock to Pin 11	$T_{MULTCK1\_P11}$	0.91	1.00	1.15	ns, Max
Clock to Pin 10	$T_{MULTCK1\_P10}$	0.91	1.00	1.15	ns, Max
Clock to Pin 9	$T_{MULTCK1\_P9}$	0.91	1.00	1.15	ns, Max
Clock to Pin 8	$T_{MULTCK1\_P8}$	0.91	1.00	1.15	ns, Max
Clock to Pin 7	$T_{MULTCK1\_P7}$	0.91	1.00	1.15	ns, Max
Clock to Pin 6	$T_{MULTCK1\_P6}$	0.91	1.00	1.15	ns, Max
Clock to Pin 5	$T_{MULTCK1\_P5}$	0.91	1.00	1.15	ns, Max
Clock to Pin 4	$T_{MULTCK1\_P4}$	0.91	1.00	1.15	ns, Max
Clock to Pin 3	$T_{MULTCK1\_P3}$	0.91	1.00	1.15	ns, Max
Clock to Pin 2	$T_{MULTCK1\_P2}$	0.91	1.00	1.15	ns, Max
Clock to Pin 1	$T_{MULTCK1\_P1}$	0.91	1.00	1.15	ns, Max
Clock to Pin 0	$T_{MULTCK1\_P0}$	0.91	1.00	1.15	ns, Max

Configuration Timing

Configuration Memory Clearing Parameters

Power-up timing of configuration signals is shown in Figure 2; corresponding timing characteristics are listed in Table 30.

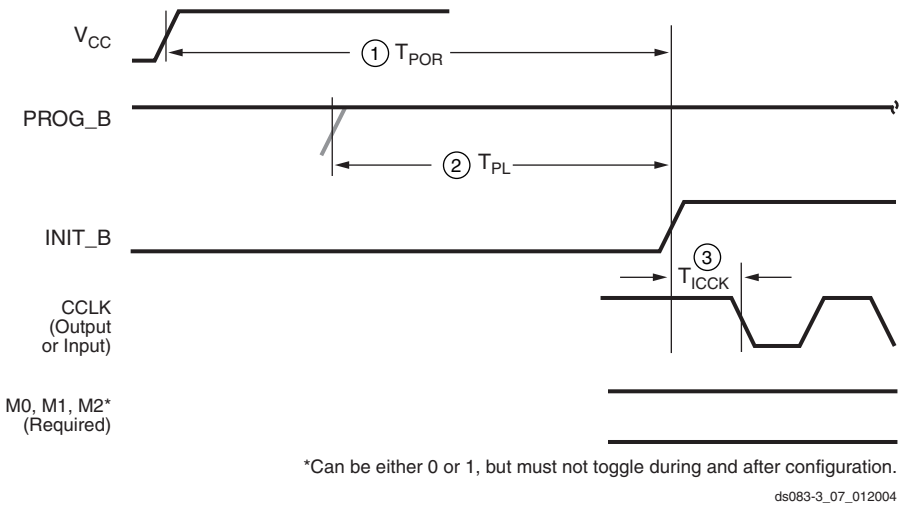

Figure 2: **Configuration Power-Up Timing**

Table 30: **Power-Up Timing Characteristics**

Description	Figure References	Symbol	Value	Units
Power-on reset	1	T_{POR}	T_{PL} + 2	ms, max
Program latency	2	T_{PL}	4	µs per frame, max
CCLK (output) delay	3	T_{ICCK}	0.5	µs, min
			4.0	µs, max
Program pulse width		$T_{PROGRAM}$	300	ns, min

Notes:
1. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or V_{CCAUX}. The mode pins should not be toggled during and after configuration.

Master/Slave Serial Mode Parameters

Clock timing for Slave Serial configuration programming is shown in Figure 3, with Master Serial clock timing shown in Figure 4. Programming parameters for both Slave and Master modes are given in Table 31.

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
NA	GND	L11		
NA	GND	L10		
NA	GND	K17		
NA	GND	K16		
NA	GND	K15		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	F21		
NA	GND	F6		
NA	GND	E22		
NA	GND	E5		
NA	GND	D23		
NA	GND	D4		
NA	GND	C24		
NA	GND	C3		
NA	GND	B25		
NA	GND	B14		
NA	GND	B13		
NA	GND	B2		
NA	GND	A26		
NA	GND	A1		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
2	IO_L01P_2	D23		
2	IO_L02N_2/VRP_2	E21		
2	IO_L02P_2/VRN_2	E22		
2	IO_L03N_2	F21		
2	IO_L03P_2/VREF_2	F20		
2	IO_L04N_2	G20		
2	IO_L04P_2	G19		
2	IO_L06N_2	H18		
2	IO_L06P_2	J17		
2	IO_L19N_2	D24		
2	IO_L19P_2	E23		
2	IO_L21N_2	E24		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	F23		
2	IO_L22P_2	G23		
2	IO_L24N_2	G21		
2	IO_L24P_2	G22		
2	IO_L43N_2	H19		
2	IO_L43P_2	H20		
2	IO_L45N_2	J18		
2	IO_L45P_2/VREF_2	J19		
2	IO_L46N_2	K17		
2	IO_L46P_2	K18		
2	IO_L48N_2	H23		
2	IO_L48P_2	H24		
2	IO_L49N_2	H21		
2	IO_L49P_2	H22		
2	IO_L51N_2	J24		
2	IO_L51P_2/VREF_2	K24		
2	IO_L52N_2	J22		
2	IO_L52P_2	J23		
2	IO_L54N_2	J20		
2	IO_L54P_2	J21		
2	IO_L67N_2	K19	NC	
2	IO_L67P_2	K20	NC	
2	IO_L69N_2	L17	NC	

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
4	IO_L02P_4/D1	AB20		
4	IO_L03N_4/D2/ALT_VRP_4	Y19		
4	IO_L03P_4/D3/ALT_VRN_4	AA19		
4	IO_L04N_4/VREF_4	W18		
4	IO_L04P_4	Y18		
4	IO_L05N_4/VRP_4	U16		
4	IO_L05P_4/VRN_4	V17		
4	IO_L06N_4	AD20		
4	IO_L06P_4	AD19		
4	IO_L19N_4	AC20		
4	IO_L19P_4	AC19		
4	IO_L21N_4	AA18		
4	IO_L21P_4/VREF_4	AB18		
4	IO_L22N_4	AC18		
4	IO_L22P_4	AC17		
4	IO_L24N_4	AA17		
4	IO_L24P_4	AB17		
4	IO_L49N_4	Y17		
4	IO_L49P_4	W17		
4	IO_L51N_4	V16		
4	IO_L51P_4/VREF_4	W16		
4	IO_L52N_4	AD17		
4	IO_L52P_4	AD16		
4	IO_L54N_4	AB16		
4	IO_L54P_4	AC16		
4	IO_L67N_4	Y16	NC	
4	IO_L67P_4	AA16	NC	
4	IO_L69N_4	W15	NC	
4	IO_L69P_4/VREF_4	Y15	NC	
4	IO_L70N_4	U15	NC	
4	IO_L70P_4	V15	NC	
4	IO_L72N_4	AD15	NC	
4	IO_L72P_4	AD14	NC	
4	IO_L73N_4	AB15	NC	NC
4	IO_L73P_4	AC15	NC	NC
4	IO_L91N_4/VREF_4	AA14		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
7	VCCO_7	F3		
NA	CCLK	AB23		
NA	PROG_B	C1		
NA	DONE	AB21		
NA	M0	AC4		
NA	M1	AB4		
NA	M2	AD3		
NA	HSWAP_EN	C2		
NA	TCK	C23		
NA	TDI	D1		
NA	TDO	C24		
NA	TMS	C21		
NA	PWRDWN_B	AC21		
NA	DXN	B4		
NA	DXP	C4		
NA	VBATT	B21		
NA	RSVD	A22		
NA	VCCAUX	AD13		
NA	VCCAUX	AC22		
NA	VCCAUX	AC3		
NA	VCCAUX	N1		
NA	VCCAUX	M24		
NA	VCCAUX	B22		
NA	VCCAUX	B3		
NA	VCCAUX	A12		
NA	VCCINT	U17		
NA	VCCINT	U8		
NA	VCCINT	T16		
NA	VCCINT	T9		
NA	VCCINT	R15		
NA	VCCINT	R14		
NA	VCCINT	R13		
NA	VCCINT	R12		
NA	VCCINT	R11		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	D15		
NA	GND	D10		
NA	GND	D4		
NA	GND	C22		
NA	GND	C3		
NA	GND	B24		
NA	GND	B23		
NA	GND	B2		
NA	GND	B1		
NA	GND	A24		
NA	GND	A23		
NA	GND	A18		
NA	GND	A7		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L53N_0	G20		
0	IO_L53P_0	G19		
0	IO_L54N_0	D21		
0	IO_L54P_0	D22		
0	IO_L67N_0	E20	NC	
0	IO_L67P_0	E21	NC	
0	IO_L68N_0	H19	NC	
0	IO_L68P_0	H18	NC	
0	IO_L69N_0	D20	NC	
0	IO_L69P_0/VREF_0	D19	NC	
0	IO_L70N_0	A20	NC	
0	IO_L70P_0	A21	NC	
0	IO_L71N_0	F19	NC	
0	IO_L71P_0	F18	NC	
0	IO_L72N_0	C19	NC	
0	IO_L72P_0	C20	NC	
0	IO_L73N_0	B18	NC	NC
0	IO_L73P_0	B19	NC	NC
0	IO_L74N_0	G18	NC	NC
0	IO_L74P_0	H17	NC	NC
0	IO_L75N_0	E18	NC	NC
0	IO_L75P_0/VREF_0	D18	NC	NC
0	IO_L76N_0	A18	NC	NC
0	IO_L76P_0	A19	NC	NC
0	IO_L77N_0	J17	NC	NC
0	IO_L77P_0	J16	NC	NC
0	IO_L78N_0	E16	NC	NC
0	IO_L78P_0	E17	NC	NC
0	IO_L91N_0/VREF_0	B17		
0	IO_L91P_0	B16		
0	IO_L92N_0	F17		
0	IO_L92P_0	F16		
0	IO_L93N_0	D16		
0	IO_L93P_0	D17		
0	IO_L94N_0/VREF_0	A17		
0	IO_L94P_0	A16		
0	IO_L95N_0/GCLK7P	H16		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
7	IO_L52P_7	J29		
7	IO_L52N_7	K29		
7	IO_L51P_7/VREF_7	K27		
7	IO_L51N_7	J27		
7	IO_L50P_7	L24		
7	IO_L50N_7	K24		
7	IO_L49P_7	H27		
7	IO_L49N_7	J28		
7	IO_L48P_7	H26		
7	IO_L48N_7	J26		
7	IO_L47P_7	K25		
7	IO_L47N_7	J25		
7	IO_L46P_7	H28		
7	IO_L46N_7	H29		
7	IO_L45P_7/VREF_7	G28		
7	IO_L45N_7	F28		
7	IO_L44P_7	L23		
7	IO_L44N_7	K23		
7	IO_L43P_7	F30		
7	IO_L43N_7	G30		
7	IO_L24P_7	F26		
7	IO_L24N_7	G27		
7	IO_L23P_7	J24		
7	IO_L23N_7	H24		
7	IO_L22P_7	F29		
7	IO_L22N_7	G29		
7	IO_L21P_7/VREF_7	G26		
7	IO_L21N_7	G25		
7	IO_L20P_7	H25		
7	IO_L20N_7	G24		
7	IO_L19P_7	D30		
7	IO_L19N_7	E30		
7	IO_L06P_7	E27		
7	IO_L06N_7	F27		
7	IO_L05P_7	J23		
7	IO_L05N_7	H22		
7	IO_L04P_7	C29		

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L30N_0	F23	
0	IO_L30P_0	F24	
0	IO_L49N_0	B28	
0	IO_L49P_0	B29	
0	IO_L50N_0	J22	
0	IO_L50P_0	J21	
0	IO_L51N_0	A28	
0	IO_L51P_0/VREF_0	A29	
0	IO_L52N_0	A26	
0	IO_L52P_0	B27	
0	IO_L53N_0	C24	
0	IO_L53P_0	D24	
0	IO_L54N_0	D22	
0	IO_L54P_0	D23	
0	IO_L60N_0	B25	NC
0	IO_L60P_0	B26	NC
0	IO_L67N_0	B23	
0	IO_L67P_0	B24	
0	IO_L68N_0	G22	
0	IO_L68P_0	G23	
0	IO_L69N_0	F22	
0	IO_L69P_0/VREF_0	F21	
0	IO_L70N_0	A23	
0	IO_L70P_0	A24	
0	IO_L71N_0	K21	
0	IO_L71P_0	K20	
0	IO_L72N_0	C22	
0	IO_L72P_0	C23	
0	IO_L73N_0	E21	
0	IO_L73P_0	E22	
0	IO_L74N_0	H21	
0	IO_L74P_0	H20	
0	IO_L75N_0	G20	
0	IO_L75P_0/VREF_0	F20	
0	IO_L76N_0	B21	
0	IO_L76P_0	B22	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
4	IO_L67N_4	AN12	
4	IO_L67P_4	AN11	
4	IO_L68N_4	AE14	
4	IO_L68P_4	AE15	
4	IO_L69N_4	AJ13	
4	IO_L69P_4/VREF_4	AJ14	
4	IO_L70N_4	AL13	
4	IO_L70P_4	AL12	
4	IO_L71N_4	AF14	
4	IO_L71P_4	AF15	
4	IO_L72N_4	AM13	
4	IO_L72P_4	AM12	
4	IO_L73N_4	AP12	
4	IO_L73P_4	AP11	
4	IO_L74N_4	AG15	
4	IO_L74P_4	AG16	
4	IO_L75N_4	AN14	
4	IO_L75P_4/VREF_4	AN13	
4	IO_L76N_4	AP14	
4	IO_L76P_4	AP13	
4	IO_L77N_4	AD16	
4	IO_L77P_4	AD17	
4	IO_L78N_4	AK14	
4	IO_L78P_4	AK13	
4	IO_L79N_4	AN16	NC
4	IO_L79P_4	AP15	NC
4	IO_L80N_4	AE16	NC
4	IO_L80P_4	AE17	NC
4	IO_L81N_4	AH15	NC
4	IO_L81P_4/VREF_4	AJ15	NC
4	IO_L82N_4	AP17	NC
4	IO_L82P_4	AN17	NC
4	IO_L83N_4	AH17	NC
4	IO_L83P_4	AH16	NC
4	IO_L84N_4	AL15	NC
4	IO_L84P_4	AL14	NC

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
6	IO_L71P_6	AD34	
6	IO_L71N_6	AC34	
6	IO_L72P_6	AC31	
6	IO_L72N_6	AD31	
6	IO_L73P_6	Y27	
6	IO_L73N_6	W27	
6	IO_L74P_6	AB29	
6	IO_L74N_6	AA29	
6	IO_L75P_6	AB31	
6	IO_L75N_6/VREF_6	AA31	
6	IO_L76P_6	Y28	
6	IO_L76N_6	Y29	
6	IO_L77P_6	AB33	
6	IO_L77N_6	AA33	
6	IO_L78P_6	AA30	
6	IO_L78N_6	AB30	
6	IO_L79P_6	W24	NC
6	IO_L79N_6	V24	NC
6	IO_L80P_6	AB34	NC
6	IO_L80N_6	AA34	NC
6	IO_L81P_6	W33	NC
6	IO_L81N_6/VREF_6	Y34	NC
6	IO_L82P_6	W25	NC
6	IO_L82N_6	V25	NC
6	IO_L83P_6	Y32	NC
6	IO_L83N_6	AA32	NC
6	IO_L84P_6	W29	NC
6	IO_L84N_6	V29	NC
6	IO_L91P_6	W28	
6	IO_L91N_6	V28	
6	IO_L92P_6	V33	
6	IO_L92N_6	V34	
6	IO_L93P_6	Y31	
6	IO_L93N_6/VREF_6	W31	
6	IO_L94P_6	V26	
6	IO_L94N_6	V27	

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	AR26		
NA	GND	AR14		
NA	GND	AR5		
NA	GND	AP34		
NA	GND	AP6		
NA	GND	AN33		
NA	GND	AN20		
NA	GND	AN7		
NA	GND	AM32		
NA	GND	AM23		
NA	GND	AM17		
NA	GND	AM8		
NA	GND	AL31		
NA	GND	AL9		
NA	GND	AK30		
NA	GND	AK20		
NA	GND	AK10		
NA	GND	AJ38		
NA	GND	AJ29		
NA	GND	AJ11		
NA	GND	AJ2		
NA	GND	AF35		
NA	GND	AF5		
NA	GND	AD23		
NA	GND	AD22		
NA	GND	AD21		
NA	GND	AD20		
NA	GND	AD19		
NA	GND	AD18		
NA	GND	AD17		
NA	GND	AC36		
NA	GND	AC32		
NA	GND	AC24		
NA	GND	AC23		
NA	GND	AC22		
NA	GND	AC21		

Table 13: **FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	GND	D4		
NA	GND	C39		
NA	GND	C38		
NA	GND	C37		
NA	GND	C3		
NA	GND	C2		
NA	GND	C1		
NA	GND	B39		
NA	GND	B38		
NA	GND	B37		
NA	GND	B29		
NA	GND	B11		
NA	GND	B3		
NA	GND	B2		
NA	GND	B1		
NA	GND	A38		
NA	GND	A37		
NA	GND	A20		
NA	GND	A3		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.