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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	92
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-4csg144c

Table 4: LVTTTL and LVC MOS Programmable Currents (Sink and Source)

SelectI/O-Ultra	Programmable Current (Worst-Case Guaranteed Minimum)						
LVTTTL	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS33	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS25	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA
LVC MOS18	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a
LVC MOS15	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	n/a

Figure 6 shows the SSTL2, SSTL3, and HSTL configurations. HSTL can sink current up to 48 mA. (HSTL IV)

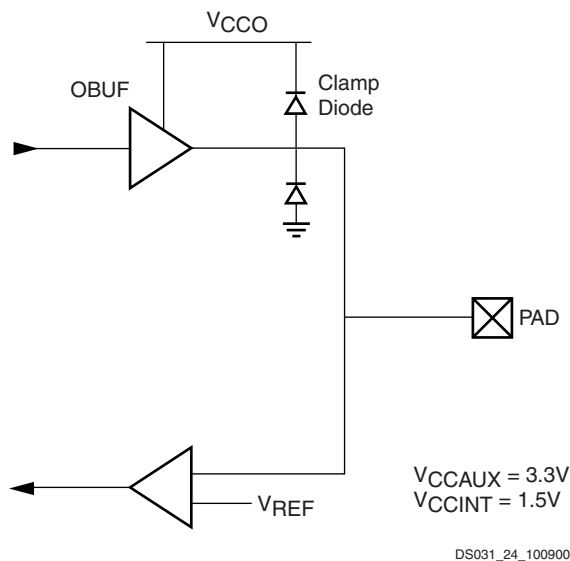


Figure 6: SSTL or HSTL SelectI/O-Ultra Standards

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Virtex-II uses two memory cells to control the configuration of an I/O as an input. This is to reduce the probability of an I/O configured as an input from flipping to an output when subjected to a single event upset (SEU) in space applications.

Prior to configuration, all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive. The dedicated pin HSWAP_EN controls the pull-up resistors prior to configuration. By default, HSWAP_EN is set high, which disables the pull-up resistors on user I/O pins. When HSWAP_EN is set low, the pull-up resistors are activated on user I/O pins.

All Virtex-II IOBs support IEEE 1149.1 compatible Boundary-Scan testing.

Input Path

The Virtex-II IOB input path routes input signals directly to internal logic and / or through an optional input flip-flop or latch, or through the DDR input registers. An optional delay element at the D-input of the storage element eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the Virtex-II device, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} . The need to supply V_{REF} imposes constraints on which standards can be used in the same bank. See I/O banking description.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output and / or the 3-state signal can be routed to the buffer directly from the internal logic or through an output / 3-state flip-flop or latch, or through the DDR output / 3-state registers.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. In most signaling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in the same bank. See I/O banking description.

I/O Banking

Some of the I/O standards described above require V_{CCO} and V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOB blocks, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from dividing each edge of the FPGA into two banks, as shown in Figure 7 and Figure 8. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Figure 18, Figure 19, and Figure 20 illustrate various example configurations.

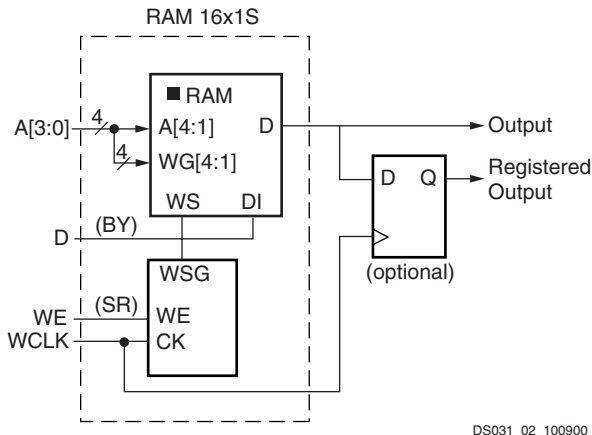


Figure 18: Distributed SelectRAM (RAM16x1S)

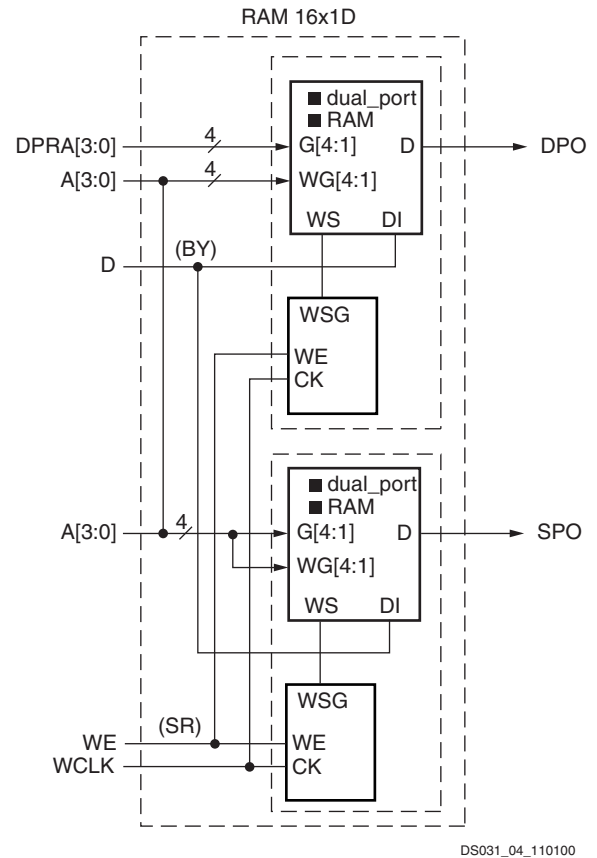


Figure 20: Dual-Port Distributed SelectRAM (RAM16x1D)

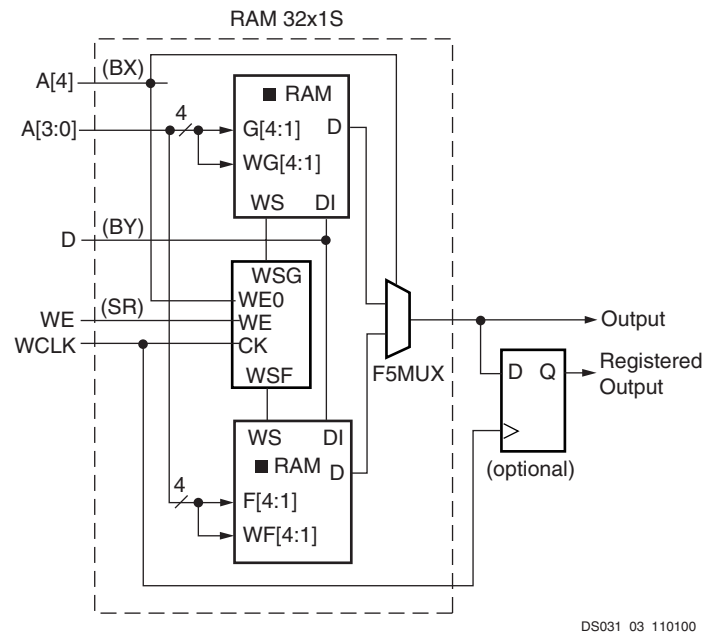


Figure 19: Single-Port Distributed SelectRAM (RAM32x1S)

Similar to the RAM configuration, each function generator (LUT) can implement a 16 x 1-bit ROM. Five configurations are available: ROM16x1, ROM32x1, ROM64x1, ROM128x1, and ROM256x1. The ROM elements are cascadable to implement wider or/and deeper ROM. ROM contents are loaded at configuration. Table 10 shows the number of LUTs occupied by each configuration.

Table 10: ROM Configuration

ROM	Number of LUTs
16 x 1	1
32 x 1	2
64 x 1	4
128 x 1	8 (1 CLB)
256 x 1	16 (2 CLBs)

Routing

DCM Locations/Organization

Virtex-II DCMs are placed on the top and bottom of each block RAM and multiplier column. The number of DCMs depends on the device size, as shown in Table 24.

Table 24: DCM Organization

Device	Columns	DCMs
XC2V40	2	4
XC2V80	2	4
XC2V250	4	8
XC2V500	4	8
XC2V1000	4	8
XC2V1500	4	8
XC2V2000	4	8
XC2V3000	6	12
XC2V4000	6	12
XC2V6000	6	12
XC2V8000	6	12

ing resources are segmented to offer the advantages of a hierarchical solution. Virtex-II logic features like CLBs, IOBs, block RAM, multipliers, and DCMs are all connected to an identical switch matrix for access to global routing resources, as shown in Figure 47.

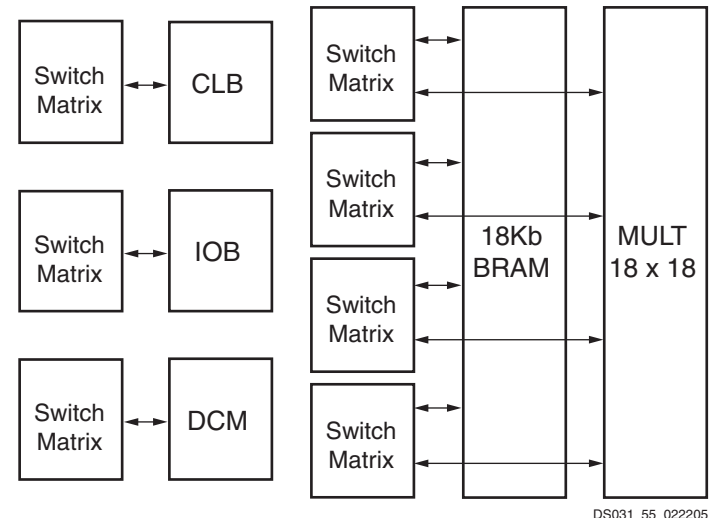


Figure 47: Active Interconnect Technology

Active Interconnect Technology

Local and global Virtex-II routing resources are optimized for speed and timing predictability, as well as to facilitate IP cores implementation. Virtex-II Active Interconnect Technology is a fully buffered programmable routing matrix. All rout-

Each Virtex-II device can be represented as an array of switch matrixes with logic blocks attached, as illustrated in Figure 48.

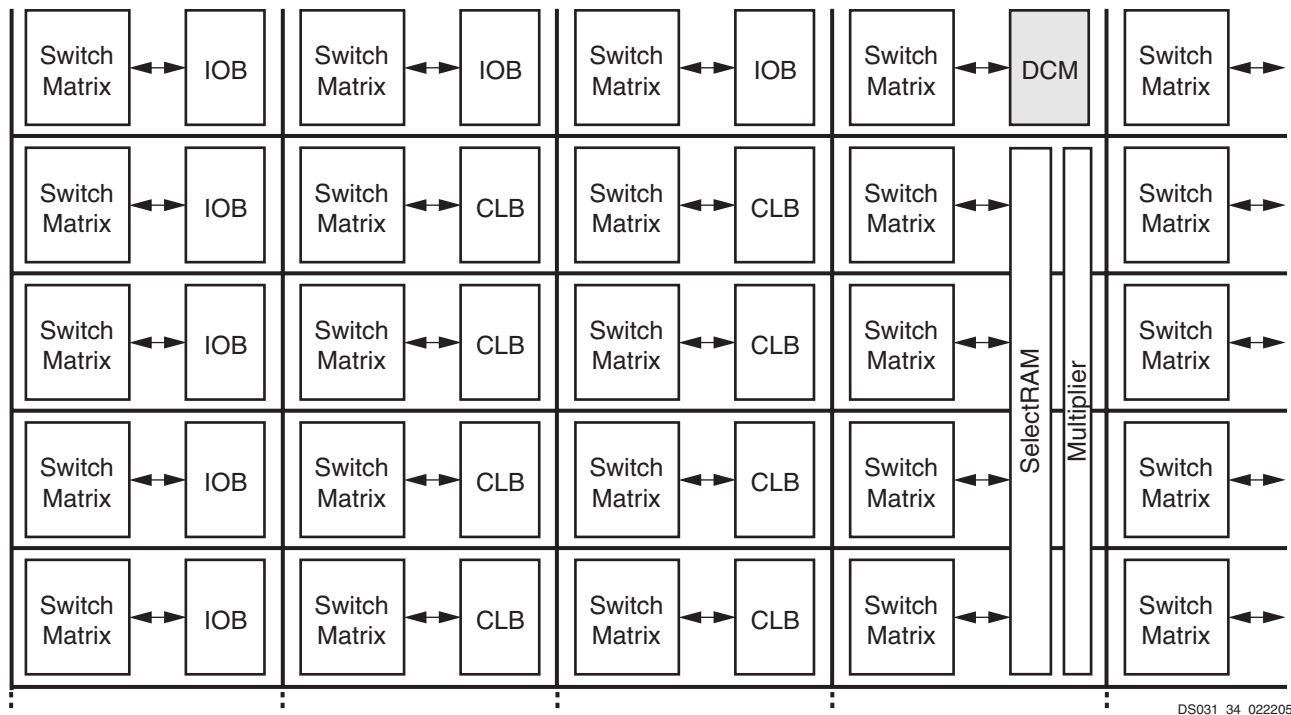


Figure 48: Routing Resources

ments to begin changing state in response to the logic and the user clock.

The relative timing of these events can be changed via configuration options in software. In addition, the GTS and GWE events can be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence can also be paused at any stage, until lock has been achieved on any or all DCMs, as well as the DCI.

Readback

In this mode, configuration data from the Virtex-II FPGA device can be read back. Readback is supported only in the SelectMAP (master and slave) and Boundary-Scan mode.

Along with the configuration data, it is possible to read back the contents of all registers, distributed SelectRAM, and block RAM resources. This capability is used for real-time debugging. For more detailed configuration information, see the *Virtex-II Platform FPGA User Guide*.

Bitstream Encryption

Virtex-II devices have an on-chip decryptor using one or two sets of three keys for triple-key Data Encryption Standard (DES) operation. Xilinx software tools offer an optional encryption of the configuration data (bitstream) with a triple-key DES determined by the designer.

The keys are stored in the FPGA by JTAG instruction and retained by a battery connected to the V_{BATT} pin, when the device is not powered. Virtex-II devices can be configured with the corresponding encrypted bitstream, using any of the configuration modes described previously.

A detailed description of how to use bitstream encryption is provided in the *Virtex-II Platform FPGA User Guide*. For devices that support this feature, please contact your sales representative for specific ordering part number.

Partial Reconfiguration

Partial reconfiguration of Virtex-II devices can be accomplished in either Slave SelectMAP mode or Boundary-Scan mode. Instead of resetting the chip and doing a full configuration, new data is loaded into a specified area of the chip, while the rest of the chip remains in operation. Data is loaded on a column basis, with the smallest load unit being a configuration “frame” of the bitstream (device size dependent).

Partial reconfiguration is useful for applications that require different designs to be loaded into the same area of a chip, or that require the ability to change portions of a design without having to reset or reconfigure the entire chip.

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard). A note was added to Table 1 .
04/02/01	1.5	- Under Input/Output Individual Options, the range of values for optional pull-up and pull-down resistors was changed to 10 - 60 KΩ from 50 - 100 KΩ. - Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	- Added Table 6. - Changed definition of multiply and divide integer ranges under Digital Clock Manager (DCM). - Made numerous minor edits throughout this module.
10/02/01	1.7	Updated descriptions under Digitally Controlled Impedance (DCI), Global Clock Multiplexer Buffers, Digital Clock Manager (DCM), and Creating a Design.
10/12/01	1.8	Made clarifying edits under Digital Clock Manager (DCM).
11/29/01	1.9	Changed bitstream lengths for each device in Table 26.

Extended LVDS DC Specifications (LVDSEXT_33 & LVDSEXT_25)

Table 9: Extended LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}			3.3 or 2.5		V
Output High voltage for Q and $\bar{Q}$	V_{OH}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals			1.785	V
Output Low voltage for Q and $\bar{Q}$	V_{OL}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	0.705			V
Differential output voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{ODIFF}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	440		820	mV
Output common-mode voltage	V_{OCM}	$R_T = 100\ \Omega$ across Q and $\bar{Q}$ signals	1.125	1.200	1.375	V
Differential input voltage (Q – $\bar{Q}$), Q = High ($\bar{Q}$ – Q), $\bar{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	N/A	mV
Input common-mode voltage	V_{ICM}	Differential input voltage = ± 350 mV	0.2	1.25	$V_{CCO} - 0.5$	V

LVPECL DC Specifications

These values are valid when driving a $100\ \Omega$ differential load only, i.e., a $100\ \Omega$ resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower

common-mode ranges. Table 10 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see the *Virtex-II User Guide*.

Table 10: LVPECL DC Specifications

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

Table 15: IOB Input Switching Characteristics Standard Adjustments (Continued)

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVDCI, 3.3V, Half-Impedance	LVDCI_DV2_33	T _{ILVDCI_DV2_33}	0.00	0.00	0.00	ns
LVDCI, 2.5V, Half-Impedance	LVDCI_DV2_25	T _{ILVDCI_DV2_25}	0.11	0.11	0.12	ns
LVDCI, 1.8V, Half-Impedance	LVDCI_DV2_18	T _{ILVDCI_DV2_18}	0.42	0.43	0.49	ns
LVDCI, 1.5V, Half-Impedance	LVDCI_DV2_15	T _{ILVDCI_DV2_15}	0.98	1.00	1.14	ns
HSLVDCI (High-Speed Low-Voltage DCI), 1.5V	HSLVDCI_15	T _{IHSLVDCI_15}	0.42	0.42	0.48	ns
HSLVDCI, 1.8V	HSLVDCI_18	T _{IHSLVDCI_18}	0.52	0.53	0.60	ns
HSLVDCI, 2.5V	HSLVDCI_25	T _{IHSLVDCI_25}	0.42	0.42	0.48	ns
HSLVDCI, 3.3V	HSLVDCI_33	T _{IHSLVDCI_33}	0.42	0.42	0.48	ns
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	T _{IGTL_DCI}	0.42	0.42	0.48	ns
GTL Plus with DCI	GTLP_DCI	T _{IGTLP_DCI}	0.42	0.42	0.48	ns
HSTL (High-Speed Transceiver Logic), Class I, with DCI	HSTL_I_DCI	T _{IHSTL_I_DCI}	0.42	0.42	0.48	ns
HSTL, Class II, with DCI	HSTL_II_DCI	T _{IHSTL_II_DCI}	0.42	0.42	0.48	ns
HSTL, Class III, with DCI	HSTL_III_DCI	T _{IHSTL_III_DCI}	0.42	0.42	0.48	ns
HSTL, Class IV, with DCI	HSTL_IV_DCI	T _{IHSTL_IV_DCI}	0.42	0.42	0.48	ns
HSTL, Class I, 1.8V, with DCI	HSTL_I_DCI_18	T _{IHSTL_I_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class II, 1.8V, with DCI	HSTL_II_DCI_18	T _{IHSTL_II_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	T _{IHSTL_III_DCI_18}	0.42	0.42	0.48	ns
HSTL, Class IV, 1.8V, with DCI	HSTL_IV_DCI_18	T _{IHSTL_IV_DCI_18}	0.42	0.42	0.48	ns
SSTL (Stub Series Terminated Logic), Class I, 1.8V, with DCI	SSTL18_I_DCI	T _{ISSTL18_I_DCI}	0.42	0.42	0.48	ns
SSTL, Class II, 1.8V, with DCI	SSTL18_II_DCI	T _{ISSTL18_II_DCI}	0.42	0.42	0.48	ns
SSTL, Class I, 2.5V, with DCI	SSTL2_I_DCI	T _{ISSTL2_I_DCI}	0.42	0.42	0.48	ns
SSTL, Class II, 2.5V, with DCI	SSTL2_II_DCI	T _{ISSTL2_II_DCI}	0.42	0.42	0.48	ns
SSTL, Class I, 3.3V, with DCI	SSTL3_I_DCI	T _{ISSTL3_I_DCI}	0.35	0.35	0.40	ns
SSTL, Class II, 3.3V, with DCI	SSTL3_II_DCI	T _{ISSTL3_II_DCI}	0.35	0.35	0.40	ns
LVDS (Low-Voltage Differential Signaling), 2.5V, with DCI	LVDS_25_DCI	T _{ILVDS_25_DCI}	0.60	0.60	0.69	ns
LVDS, 3.3V, with DCI	LVDS_33_DCI	T _{ILVDS_33_DCI}	0.60	0.60	0.69	ns
LVDSEXT (LVDS Extended Mode), 2.5V, with DCI	LVDSEXT_25_DCI	T _{ILVDSEXT_25_DCI}	0.58	0.59	0.79	ns
LVDSEXT, 3.3V, with DCI	LVDSEXT_33_DCI	T _{ILVDSEXT_33_DCI}	0.56	0.56	0.65	ns

Notes:

1. Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see [Table 18](#).

IOB Output Switching Characteristics Standard Adjustments

Table 17 gives all standard-specific adjustments for output delays terminating at pads, based on standard capacitive load, C_{REF} . Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Table 17: IOB Output Switching Characteristics Standard Adjustments

Description	IOSTANDARD Attribute	Timing Parameter	Speed Grade			Units
			-6	-5	-4	
LVTTTL (Low-Voltage Transistor-Transistor Logic), Slow, 2 mA	LVTTTL_S2	$T_{OLVTTTL_S2}$	9.42	9.71	10.68	ns
LVTTTL, Slow, 4 mA	LVTTTL_S4	$T_{OLVTTTL_S4}$	5.77	5.95	6.55	ns
LVTTTL, Slow, 6 mA	LVTTTL_S6	$T_{OLVTTTL_S6}$	4.11	4.24	4.66	ns
LVTTTL, Slow, 8 mA	LVTTTL_S8	$T_{OLVTTTL_S8}$	2.87	2.96	3.26	ns
LVTTTL, Slow, 12 mA	LVTTTL_S12	$T_{OLVTTTL_S12}$	2.32	2.39	2.63	ns
LVTTTL, Slow, 16 mA	LVTTTL_S16	$T_{OLVTTTL_S16}$	1.70	1.75	1.93	ns
LVTTTL, Slow, 24 mA	LVTTTL_S24	$T_{OLVTTTL_S24}$	1.26	1.30	1.43	ns
LVTTTL, Fast, 2 mA	LVTTTL_F2	$T_{OLVTTTL_F2}$	6.52	6.72	7.39	ns
LVTTTL, Fast, 4 mA	LVTTTL_F4	$T_{OLVTTTL_F4}$	2.80	2.88	3.17	ns
LVTTTL, Fast, 6 mA	LVTTTL_F6	$T_{OLVTTTL_F6}$	1.57	1.62	1.78	ns
LVTTTL, Fast, 8 mA	LVTTTL_F8	$T_{OLVTTTL_F8}$	0.46	0.48	0.52	ns
LVTTTL, Fast, 12 mA	LVTTTL_F12	$T_{OLVTTTL_F12}$	0.00	0.00	0.00	ns
LVTTTL, Fast, 16 mA	LVTTTL_F16	$T_{OLVTTTL_F16}$	-0.13	-0.14	-0.15	ns
LVTTTL, Fast, 24 mA	LVTTTL_F24	$T_{OLVTTTL_F24}$	-0.22	-0.23	-0.26	ns
LVC MOS (Low-Voltage CMOS), 3.3V, Slow, 2 mA	LVC MOS33_S2	$T_{OLVCMOS33_S2}$	7.67	7.91	8.70	ns
LVC MOS, 3.3V, Slow, 4 mA	LVC MOS33_S4	$T_{OLVCMOS33_S4}$	4.37	4.50	4.95	ns
LVC MOS, 3.3V, Slow, 6 mA	LVC MOS33_S6	$T_{OLVCMOS33_S6}$	3.34	3.44	3.78	ns
LVC MOS, 3.3V, Slow, 8 mA	LVC MOS33_S8	$T_{OLVCMOS33_S8}$	2.29	2.36	2.60	ns
LVC MOS, 3.3V, Slow, 12 mA	LVC MOS33_S12	$T_{OLVCMOS33_S12}$	1.91	1.97	2.16	ns
LVC MOS, 3.3V, Slow, 16 mA	LVC MOS33_S16	$T_{OLVCMOS33_S16}$	1.24	1.27	1.40	ns
LVC MOS, 3.3V, Slow, 24 mA	LVC MOS33_S24	$T_{OLVCMOS33_S24}$	1.18	1.22	1.34	ns
LVC MOS, 3.3V, Fast, 2 mA	LVC MOS33_F2	$T_{OLVCMOS33_F2}$	5.82	6.00	6.60	ns
LVC MOS, 3.3V, Fast, 4 mA	LVC MOS33_F4	$T_{OLVCMOS33_F4}$	2.48	2.55	2.81	ns
LVC MOS, 3.3V, Fast, 6 mA	LVC MOS33_F6	$T_{OLVCMOS33_F6}$	1.28	1.31	1.45	ns
LVC MOS, 3.3V, Fast, 8 mA	LVC MOS33_F8	$T_{OLVCMOS33_F8}$	0.48	0.49	0.54	ns
LVC MOS, 3.3V, Fast, 12 mA	LVC MOS33_F12	$T_{OLVCMOS33_F12}$	0.27	0.28	0.31	ns
LVC MOS, 3.3V, Fast, 16 mA	LVC MOS33_F16	$T_{OLVCMOS33_F16}$	-0.14	-0.14	-0.15	ns
LVC MOS, 3.3V, Fast, 24 mA	LVC MOS33_F24	$T_{OLVCMOS33_F24}$	-0.21	-0.21	-0.23	ns
LVC MOS, 2.5V, Slow, 2 mA	LVC MOS25_S2	$T_{OLVCMOS25_S2}$	9.11	9.39	10.33	ns
LVC MOS, 2.5V, Slow, 4 mA	LVC MOS25_S4	$T_{OLVCMOS25_S4}$	5.00	5.16	5.67	ns
LVC MOS, 2.5V, Slow, 6 mA	LVC MOS25_S6	$T_{OLVCMOS25_S6}$	4.53	4.67	5.13	ns
LVC MOS, 2.5V, Slow, 8 mA	LVC MOS25_S8	$T_{OLVCMOS25_S8}$	3.86	3.98	4.38	ns
LVC MOS, 2.5V, Slow, 12 mA	LVC MOS25_S12	$T_{OLVCMOS25_S12}$	2.84	2.93	3.22	ns
LVC MOS, 2.5V, Slow, 16 mA	LVC MOS25_S16	$T_{OLVCMOS25_S16}$	2.36	2.43	2.67	ns
LVC MOS, 2.5V, Slow, 24 mA	LVC MOS25_S24	$T_{OLVCMOS25_S24}$	2.00	2.06	2.27	ns
LVC MOS, 2.5V, Fast, 2 mA	LVC MOS25_F2	$T_{OLVCMOS25_F2}$	4.06	4.18	4.60	ns
LVC MOS, 2.5V, Fast, 4 mA	LVC MOS25_F4	$T_{OLVCMOS25_F4}$	1.15	1.18	1.30	ns
LVC MOS, 2.5V, Fast, 6 mA	LVC MOS25_F6	$T_{OLVCMOS25_F6}$	0.72	0.74	0.81	ns
LVC MOS, 2.5V, Fast, 8 mA	LVC MOS25_F8	$T_{OLVCMOS25_F8}$	0.33	0.34	0.37	ns
LVC MOS, 2.5V, Fast, 12 mA	LVC MOS25_F12	$T_{OLVCMOS25_F12}$	0.02	0.02	0.03	ns

Multiplier Switching Characteristics

Table 24: Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Propagation Delay to Output Pin					
Input to Pin 35	T_{MULT_P35}	4.66	8.50	10.36	ns, Max
Input to Pin 34	T_{MULT_P34}	4.57	8.33	10.15	ns, Max
Input to Pin 33	T_{MULT_P33}	4.47	8.16	9.95	ns, Max
Input to Pin 32	T_{MULT_P32}	4.37	7.99	9.74	ns, Max
Input to Pin 31	T_{MULT_P31}	4.28	7.82	9.53	ns, Max
Input to Pin 30	T_{MULT_P30}	4.18	7.65	9.33	ns, Max
Input to Pin 29	T_{MULT_P29}	4.08	7.48	9.12	ns, Max
Input to Pin 28	T_{MULT_P28}	3.99	7.31	8.91	ns, Max
Input to Pin 27	T_{MULT_P27}	3.89	7.14	8.70	ns, Max
Input to Pin 26	T_{MULT_P26}	3.79	6.97	8.50	ns, Max
Input to Pin 25	T_{MULT_P25}	3.69	6.80	8.29	ns, Max
Input to Pin 24	T_{MULT_P24}	3.60	6.63	8.08	ns, Max
Input to Pin 23	T_{MULT_P23}	3.50	6.46	7.88	ns, Max
Input to Pin 22	T_{MULT_P22}	3.40	6.29	7.67	ns, Max
Input to Pin 21	T_{MULT_P21}	3.31	6.12	7.46	ns, Max
Input to Pin 20	T_{MULT_P20}	3.21	5.95	7.26	ns, Max
Input to Pin 19	T_{MULT_P19}	3.11	5.78	7.05	ns, Max
Input to Pin 18	T_{MULT_P18}	3.02	5.61	6.84	ns, Max
Input to Pin 17	T_{MULT_P17}	2.92	5.44	6.63	ns, Max
Input to Pin 16	T_{MULT_P16}	2.82	5.27	6.43	ns, Max
Input to Pin 15	T_{MULT_P15}	2.72	5.10	6.22	ns, Max
Input to Pin 14	T_{MULT_P14}	2.63	4.93	6.01	ns, Max
Input to Pin 13	T_{MULT_P13}	2.53	4.76	5.81	ns, Max
Input to Pin 12	T_{MULT_P12}	2.43	4.59	5.60	ns, Max
Input to Pin 11	T_{MULT_P11}	2.34	4.42	5.39	ns, Max
Input to Pin 10	T_{MULT_P10}	2.24	4.25	5.19	ns, Max
Input to Pin 9	T_{MULT_P9}	2.14	4.08	4.98	ns, Max
Input to Pin 8	T_{MULT_P8}	2.05	3.91	4.77	ns, Max
Input to Pin 7	T_{MULT_P7}	1.95	3.74	4.56	ns, Max
Input to Pin 6	T_{MULT_P6}	1.85	3.57	4.36	ns, Max
Input to Pin 5	T_{MULT_P5}	1.75	3.40	4.15	ns, Max
Input to Pin 4	T_{MULT_P4}	1.66	3.23	3.94	ns, Max
Input to Pin 3	T_{MULT_P3}	1.56	3.06	3.74	ns, Max
Input to Pin 2	T_{MULT_P2}	1.46	2.89	3.53	ns, Max
Input to Pin 1	T_{MULT_P1}	1.37	2.72	3.32	ns, Max
Input to Pin 0	T_{MULT_P0}	1.27	2.55	3.12	ns, Max

Table 27: Enhanced Pipelined Multiplier Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	T _{MULIDCK} /T _{MULCKID}	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	T _{MULIDCK_CE} /T _{MULCKID_CE}	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	T _{MULIDCK_RST} /T _{MULCKID_RST}	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	T _{MULTCK1_P35}	3.05	3.25	3.74	ns, Max
Clock to Pin 34	T _{MULTCK1_P34}	2.95	3.14	3.61	ns, Max
Clock to Pin 33	T _{MULTCK1_P33}	2.85	3.04	3.49	ns, Max
Clock to Pin 32	T _{MULTCK1_P32}	2.76	2.93	3.37	ns, Max
Clock to Pin 31	T _{MULTCK1_P31}	2.66	2.82	3.25	ns, Max
Clock to Pin 30	T _{MULTCK1_P30}	2.56	2.72	3.12	ns, Max
Clock to Pin 29	T _{MULTCK1_P29}	2.47	2.61	3.00	ns, Max
Clock to Pin 28	T _{MULTCK1_P28}	2.37	2.50	2.88	ns, Max
Clock to Pin 27	T _{MULTCK1_P27}	2.27	2.40	2.75	ns, Max
Clock to Pin 26	T _{MULTCK1_P26}	2.17	2.29	2.63	ns, Max
Clock to Pin 25	T _{MULTCK1_P25}	2.08	2.18	2.51	ns, Max
Clock to Pin 24	T _{MULTCK1_P24}	1.98	2.07	2.38	ns, Max
Clock to Pin 23	T _{MULTCK1_P23}	1.88	1.97	2.26	ns, Max
Clock to Pin 22	T _{MULTCK1_P22}	1.79	1.86	2.14	ns, Max
Clock to Pin 21	T _{MULTCK1_P21}	1.69	1.75	2.02	ns, Max
Clock to Pin 20	T _{MULTCK1_P20}	1.59	1.65	1.89	ns, Max
Clock to Pin 19	T _{MULTCK1_P19}	1.50	1.54	1.77	ns, Max
Clock to Pin 18	T _{MULTCK1_P18}	1.40	1.43	1.65	ns, Max
Clock to Pin 17	T _{MULTCK1_P17}	1.30	1.33	1.52	ns, Max
Clock to Pin 16	T _{MULTCK1_P16}	1.20	1.22	1.40	ns, Max
Clock to Pin 15	T _{MULTCK1_P15}	1.11	1.11	1.28	ns, Max
Clock to Pin 14	T _{MULTCK1_P14}	1.01	1.00	1.15	ns, Max
Clock to Pin 13	T _{MULTCK1_P13}	0.91	1.00	1.15	ns, Max
Clock to Pin 12	T _{MULTCK1_P12}	0.91	1.00	1.15	ns, Max
Clock to Pin 11	T _{MULTCK1_P11}	0.91	1.00	1.15	ns, Max
Clock to Pin 10	T _{MULTCK1_P10}	0.91	1.00	1.15	ns, Max
Clock to Pin 9	T _{MULTCK1_P9}	0.91	1.00	1.15	ns, Max
Clock to Pin 8	T _{MULTCK1_P8}	0.91	1.00	1.15	ns, Max
Clock to Pin 7	T _{MULTCK1_P7}	0.91	1.00	1.15	ns, Max
Clock to Pin 6	T _{MULTCK1_P6}	0.91	1.00	1.15	ns, Max
Clock to Pin 5	T _{MULTCK1_P5}	0.91	1.00	1.15	ns, Max
Clock to Pin 4	T _{MULTCK1_P4}	0.91	1.00	1.15	ns, Max
Clock to Pin 3	T _{MULTCK1_P3}	0.91	1.00	1.15	ns, Max
Clock to Pin 2	T _{MULTCK1_P2}	0.91	1.00	1.15	ns, Max
Clock to Pin 1	T _{MULTCK1_P1}	0.91	1.00	1.15	ns, Max
Clock to Pin 0	T _{MULTCK1_P0}	0.91	1.00	1.15	ns, Max

Date	Version	Revision
07/30/01	1.6	- Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. - Added values to the Virtex-II Pin-to-Pin Output Parameter Guidelines and Virtex-II Pin-to-Pin Input Parameter Guidelines tables. - Added Frequency Synthesis table.
10/02/01	1.7	- Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables. - Updated the speed grade designations used in data sheets, and added Table 13, which shows the current speed grade designation for each device.
10/05/01	1.8	Corrected the speed grade designation for the XC2V1000 device in Table 13.
10/12/01	1.9	Updated values in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables.
11/28/01	2.0	Updated values in Table 3, Table 4, Table 5, Virtex-II Performance Characteristics, and Virtex-II Switching Characteristics tables.
01/03/02	2.1	- Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.96. - Changed the speed grade designation for the XC2V6000 device in Table 13.
07/16/02	2.2	- Updated values in Table 4, "Quiescent Supply Current." - Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.111. - Added Enhanced Multiplier Switching Characteristics section. - Added footnote to Table 37, "Global Clock Setup and Hold for LVTTTL Standard, Without DCM." - Added Source-Synchronous Switching Characteristics section.
09/26/02	2.3	- Removed mention of MIL-M-38510/605 specification. - Added footnotes to Table 2 and Table 6.
12/06/02	2.4	- Revised SSTL2 values in Table 6 to match the latest JEDEC specification. - Added footnote regarding V_{IN} PCI compliance to Table 1. - Added footnote regarding CLKOUT_DUTY_CYCLE_DLL to Table 41.
05/07/03	2.5	- Updated values in Virtex-II Performance Characteristics and Virtex-II Switching Characteristics tables, based on values extracted from speedsfile version 1.114. Table 4, Quiescent Supply Current, and Table 5, Minimum Power On Current Required for Virtex-II Devices: Added parameters for XC2V8000 device. Table 16, IOB Output Switching Characteristics: Changed parameter designator T_{IOTON} to T_{IOTP}. Table 26, Enhanced Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULT_P[nn]}$ to $T_{MULT1_P[nn]}$ in order to correspond with designators used in speedsfile. Table 27, Enhanced Pipelined Multiplier Switching Characteristics: Corrected all parameter designators from $T_{MULTCK_P[nn]}$ to $T_{MULTCK1_P[nn]}$ in order to correspond with designators used in speedsfile. - Removed old Table 19, Standard Capacitive Loads. - Added Figure 1, page 17, showing test configuration for measuring I/O standard adjustments.
06/19/03	2.5.1	Removed footnotes in Table 34 and Table 36 that stated DCM jitter was included in the measurements.

Pin Definitions

Table 4 provides a description of each pin type listed in Virtex-II pinout tables.

Table 4: Virtex-II Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output/ Bidirectional	All user I/O pins are capable of differential signalling and can implement LVDS, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled “IO_LXXY_#”, where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = P/N for the positive and negative sides of the differential pair. # indicates the bank number (0 through 7)
Dual-Function Pins		
IO_LXXY_#/ZZZ		The dual-function pins are labelled “IO_LXXY_#/ZZZ”, where ZZZ can be one of the following pins: Per Bank - VRP , VRN , or VREF Globally - GCLKX(S/P) , BUSY/DOUT , INIT_B , D0/DIN – D7 , RDWR_B , or CS_B
With /ZZZ:		
D0/DIN, D1, D2, D3, D4, D5, D6, D7	Input/Output	<i>In SelectMAP mode</i>, D0 through D7 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained. <i>In bit-serial modes</i>, DIN (D0) is the single-data input. This pin becomes a user I/O after configuration.
CS_B	Input	In SelectMAP mode, this is the active-low Chip Select signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
RDWR_B	Input	In SelectMAP mode, this is the active-low Write Enable signal. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained.
BUSY/DOUT	Output	<i>In SelectMAP mode</i>, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration, unless the SelectMAP port is retained. <i>In bit-serial modes</i>, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
INIT_B	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred. The pin becomes a user I/O after configuration.
GCLKx (S/P)	Input/Output	These are clock input pins that connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
VRP	Input	This pin is for the DCI voltage reference resistor of P transistor (per bank).
VRN	Input	This pin is for the DCI voltage reference resistor of N transistor (per bank).
ALT_VRP	Input	This is the alternative pin for the DCI voltage reference resistor of P transistor.
ALT_VRN	Input	This is the alternative pin for the DCI voltage reference resistor of N transistor.
V _{REF}	Input	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Dedicated Pins⁽¹⁾		
CCLK	Input/Output	Configuration clock. Output in Master mode or Input in Slave mode.

Table 5: CS144/CSG144 — XC2V40, XC2V80, and XC2V250

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

Table 7: FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
NA	GND	M10		
NA	GND	M9		
NA	GND	L14		
NA	GND	L13		
NA	GND	L12		
NA	GND	L11		
NA	GND	L10		
NA	GND	L9		
NA	GND	K14		
NA	GND	K13		
NA	GND	K12		
NA	GND	K11		
NA	GND	K10		
NA	GND	K9		
NA	GND	J14		
NA	GND	J13		
NA	GND	J12		
NA	GND	J11		
NA	GND	J10		
NA	GND	J9		
NA	GND	D19		
NA	GND	D4		
NA	GND	C20		
NA	GND	C3		
NA	GND	B21		
NA	GND	B2		
NA	GND	A22		
NA	GND	A1		

Notes:

- See Table 4 for an explanation of the signals available on this pin.

Table 10: BG728 BGA — XC2V3000

Bank	Pin Description	Pin Number
6	IO_L52N_6	V3
6	IO_L54P_6	V2
6	IO_L54N_6	V1
6	IO_L67P_6	U8
6	IO_L67N_6	T8
6	IO_L69P_6	U6
6	IO_L69N_6/VREF_6	U7
6	IO_L70P_6	U4
6	IO_L70N_6	U3
6	IO_L72P_6	U2
6	IO_L72N_6	U1
6	IO_L73P_6	T9
6	IO_L73N_6	R9
6	IO_L75P_6	T5
6	IO_L75N_6/VREF_6	T6
6	IO_L76P_6	T4
6	IO_L76N_6	R4
6	IO_L78P_6	T2
6	IO_L78N_6	T1
6	IO_L91P_6	R7
6	IO_L91N_6	R8
6	IO_L93P_6	R5
6	IO_L93N_6/VREF_6	R6
6	IO_L94P_6	R3
6	IO_L94N_6	P3
6	IO_L96P_6	R2
6	IO_L96N_6	R1
7	IO_L96P_7	P5
7	IO_L96N_7	P6
7	IO_L94P_7	P7
7	IO_L94N_7	P8
7	IO_L93P_7/VREF_7	N1
7	IO_L93N_7	N2
7	IO_L91P_7	N3
7	IO_L91N_7	N4

FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch)

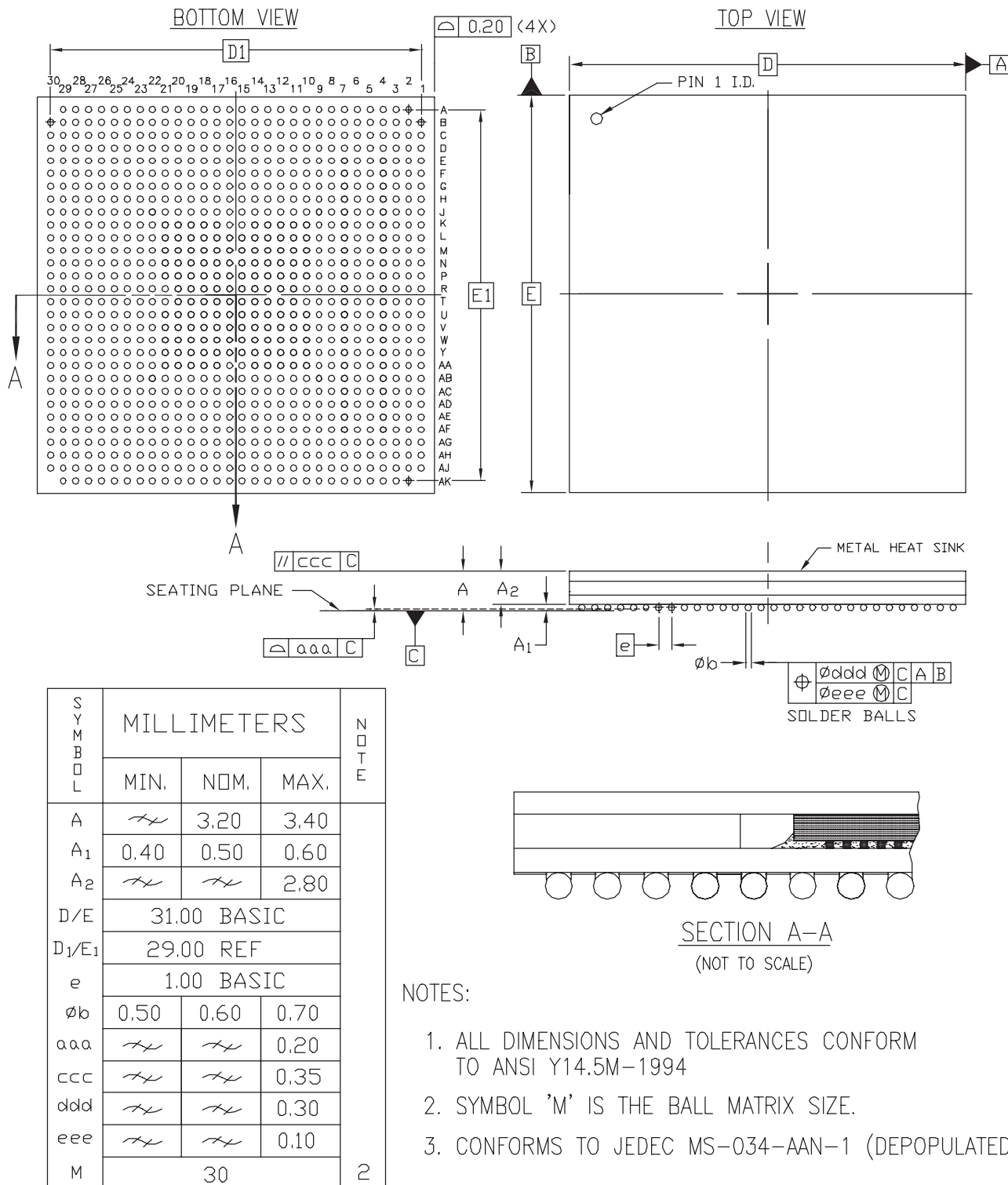


Figure 7: FF896 Flip-Chip Fine-Pitch BGA Package Specifications

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 12, XC2V3000, XC2V4000, XC2V6000, and XC2V8000 Virtex-II devices are available in the FF1152 flip-chip fine-pitch BGA package. Pins in each of these devices are the same, except for the pin differences in the XC2V3000

Table 13: FF1517 BGA — XC2V4000, XC2V6000, and XC2V8000

Bank	Pin Description	Pin Number	No Connect in the XC2V4000	No Connect in the XC2V6000
NA	DONE	AP7		
NA	M0	AN32		
NA	M1	AP33		
NA	M2	AT35		
NA	HSWAP_EN	E34		
NA	TCK	G8		
NA	TDI	D35		
NA	TDO	E6		
NA	TMS	F7		
NA	PWRDWN_B	AN8		
NA	DXN	G32		
NA	DXP	F33		
NA	VBATT	D5		
NA	RSVD	H9		
NA	VCCAUX	AV20		
NA	VCCAUX	AT37		
NA	VCCAUX	AT3		
NA	VCCAUX	Y38		
NA	VCCAUX	Y2		
NA	VCCAUX	D37		
NA	VCCAUX	D3		
NA	VCCAUX	B20		
NA	VCCINT	AG27		
NA	VCCINT	AG20		
NA	VCCINT	AG13		
NA	VCCINT	AF26		
NA	VCCINT	AF20		
NA	VCCINT	AF14		
NA	VCCINT	AE25		
NA	VCCINT	AE24		
NA	VCCINT	AE23		
NA	VCCINT	AE22		
NA	VCCINT	AE21		
NA	VCCINT	AE20		
NA	VCCINT	AE19		

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
7	IO_L06N_7	E28	
7	IO_L05P_7	K22	
7	IO_L05N_7	K21	
7	IO_L04P_7	F29	
7	IO_L04N_7	E29	
7	IO_L03P_7/VREF_7	H26	
7	IO_L03N_7	H25	
7	IO_L02P_7/VRN_7	G26	
7	IO_L02N_7/VRP_7	F27	
7	IO_L01P_7	D30	
7	IO_L01N_7	D29	
0	VCCO_0	C18	
0	VCCO_0	C25	
0	VCCO_0	F22	
0	VCCO_0	H18	
0	VCCO_0	L17	
0	VCCO_0	L18	
0	VCCO_0	L19	
0	VCCO_0	L20	
0	VCCO_0	M17	
0	VCCO_0	M18	
0	VCCO_0	M19	
1	VCCO_1	C7	
1	VCCO_1	C14	
1	VCCO_1	F10	
1	VCCO_1	H14	
1	VCCO_1	L12	
1	VCCO_1	L13	
1	VCCO_1	L14	
1	VCCO_1	L15	
1	VCCO_1	M13	
1	VCCO_1	M14	
1	VCCO_1	M15	
2	VCCO_2	G3	
2	VCCO_2	K6	
2	VCCO_2	M11	
2	VCCO_2	N11	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
5	VCCO_5	AJ18	
5	VCCO_5	AJ25	
6	VCCO_6	U20	
6	VCCO_6	U21	
6	VCCO_6	V20	
6	VCCO_6	V21	
6	VCCO_6	V24	
6	VCCO_6	V29	
6	VCCO_6	W20	
6	VCCO_6	W21	
6	VCCO_6	Y21	
6	VCCO_6	AB26	
6	VCCO_6	AE29	
7	VCCO_7	G29	
7	VCCO_7	K26	
7	VCCO_7	M21	
7	VCCO_7	N20	
7	VCCO_7	N21	
7	VCCO_7	P20	
7	VCCO_7	P21	
7	VCCO_7	P24	
7	VCCO_7	P29	
7	VCCO_7	R20	
7	VCCO_7	R21	
NA	CCLK	AJ4	
NA	PROG_B	D27	
NA	DONE	AG6	
NA	M0	AH27	
NA	M1	AJ28	
NA	M2	AG26	
NA	HSWAP_EN	E26	
NA	TCK	K11	
NA	TDI	C28	
NA	TDO	C4	
NA	TMS	J10	
NA	PWRDWN_B	AH5	
NA	DXN	F25	

Table 14: BF957 — XC2V2000, XC2V3000, XC2V4000, and XC2V6000

Bank	Pin Description	Pin Number	No Connect in XC2V2000
NA	VCCINT	T21	
NA	VCCINT	U10	
NA	VCCINT	U13	
NA	VCCINT	U19	
NA	VCCINT	U22	
NA	VCCINT	V13	
NA	VCCINT	V19	
NA	VCCINT	W13	
NA	VCCINT	W14	
NA	VCCINT	W15	
NA	VCCINT	W16	
NA	VCCINT	W17	
NA	VCCINT	W18	
NA	VCCINT	W19	
NA	VCCINT	Y12	
NA	VCCINT	Y16	
NA	VCCINT	Y20	
NA	VCCINT	AA11	
NA	VCCINT	AA16	
NA	VCCINT	AA21	
NA	VCCINT	AB15	
NA	VCCINT	AB17	
NA	GND	A2	
NA	GND	A3	
NA	GND	A16	
NA	GND	A29	
NA	GND	A30	
NA	GND	B1	
NA	GND	B2	
NA	GND	B8	
NA	GND	B24	
NA	GND	B30	
NA	GND	B31	
NA	GND	C1	
NA	GND	C3	
NA	GND	C29	
NA	GND	C31	
NA	GND	D4	

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Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- [Virtex-II Platform FPGAs: Introduction and Overview \(Module 1\)](#)
- [Virtex-II Platform FPGAs: Functional Description \(Module 2\)](#)
- [Virtex-II Platform FPGAs: DC and Switching Characteristics \(Module 3\)](#)
- [Virtex-II Platform FPGAs: Pinout Information \(Module 4\)](#)