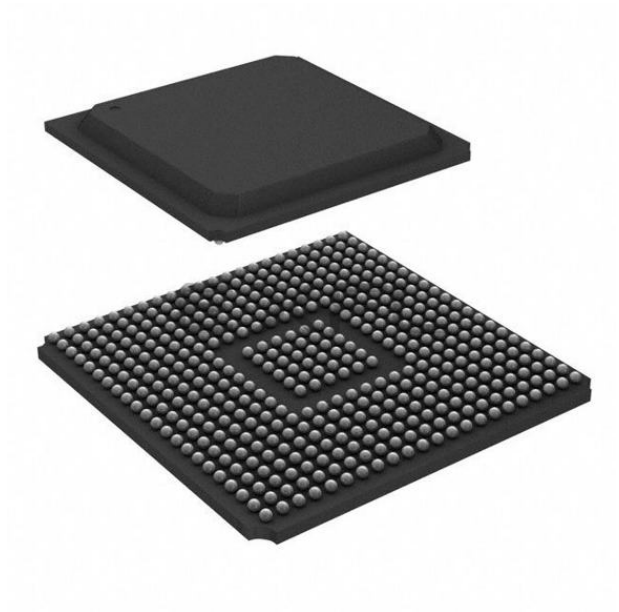
AMD Xilinx - XC2V250-4FG456I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	384
Number of Logic Elements/Cells	-
Total RAM Bits	442368
Number of I/O	200
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2v250-4fg456i

Virtex-II Platform FPGAs: Introduction and Overview

DS031-1 (v3.5) November 5, 2007 **Product Specification**

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
  - Densities from 40K to 8M system gates
  - 420 MHz internal clock speed (Advance Data)
  - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
  - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
  - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
  - DRAM interfaces
    - SDR / DDR SDRAM
    - Network FCRAM
    - Reduced Latency DRAM
  - SRAM interfaces
    - SDR / DDR SRAM
    - QDR™ SRAM
  - CAM interfaces
- Arithmetic Functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible Logic Resources
  - Up to 93,184 internal registers / latches with Clock Enable
  - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and sum-of-products support
  - Internal 3-state bussing
- High-Performance Clock Management Circuitry
  - Up to 12 DCM (Digital Clock Manager) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers
- Active Interconnect Technology
  - Fourth generation segmented routing structure
  - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
  - Up to 1,108 user I/Os
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI-X compatible (133 MHz and 66 MHz) at 3.3V
  - PCI compliant (66 MHz and 33 MHz) at 3.3V
  - CardBus compliant (33 MHz) at 3.3V
  - Differential Signaling
    - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
    - Bus LVDS I/O
    - Lightning Data Transport (LDT) I/O with current driver buffers
    - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
    - Built-in DDR input and output registers
  - Proprietary high-performance SelectLink Technology
    - High-bandwidth data path
    - Double Data Rate (DDR) link
    - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Integrated VHDL and Verilog design flows
  - Compilation of 10M system gates designs
  - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
  - Fast SelectMAP configuration
  - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
  - IEEE 1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested

Table 6: **Virtex-II Device/Package Combinations and Maximum Number of Available I/Os (Advance Information)**

Package(1,2)	Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144/CSG144	88	92	92	-	-	-	-	-	-	-	-
FG256/FGG256	88	120	172	172	172	-	-	-	-	-	-
FG456/FGG456	-	-	200	264	324	-	-	-	-	-	-
FG676/FGG676	-	-	-	-	-	392	456	484	-	-	-
FF896	-	-	-	-	432	528	624	-	-	-	-
FF1152	-	-	-	-	-	-	-	720	824	824	824
FF1517	-	-	-	-	-	-	-	-	912	1,104	1,108
BG575/BGG575	-	-	-	-	328	392	408	-	-	-	-
BG728/BGG728	-	-	-	-	-	-	-	516	-	-	-
BF957	-	-	-	-	-	-	624	684	684	684	-

Notes:
1. All devices in a particular package are pinout (footprint) compatible. In addition, the FG456/FGG456 and FG676/FGG676 packages are compatible, as are the FF896 and FF1152 packages.
2. Wire-bond packages CS144, FG256, FG456, FG676, BG575, and BG728 are also available in Pb-free versions CSG144, FGG256, FGG456, FGG676, BGG575, and BGG728. See Virtex-II Ordering Examples for details on how to order.

Virtex-II Ordering Examples

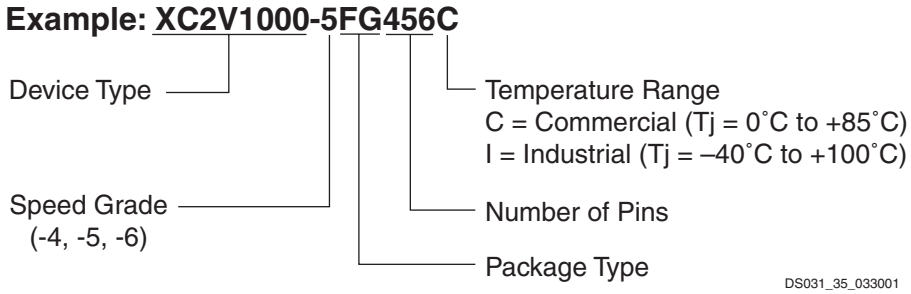


Figure 2: **Virtex-II Ordering Example. Regular Package**

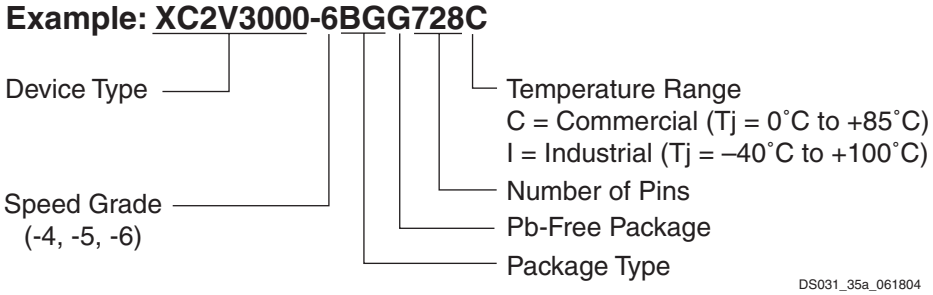


Figure 3: **Virtex-II Ordering Example. Pb-Free Package**

Revision History

This section records the change history for this module of the data sheet.

Date	Version	Revision
11/07/00	1.0	Early access draft.
12/06/00	1.1	Initial release.
01/15/01	1.2	Added values to the tables in the Virtex-II Performance Characteristics and Virtex-II Switching Characteristics sections.
01/25/01	1.3	The data sheet was divided into four modules (per the current style standard).
04/02/01	1.5	Skipped v1.4 to sync up modules. Reverted to traditional double-column format.
07/30/01	1.6	Made minor changes to items listed under Summary of Virtex-II™ Features.
10/02/01	1.7	Minor edits.
07/16/02	1.8	Updated Virtex-II Device/Package Combinations shown in Table 6.
09/26/02	1.9	Updated Table 2 and Table 6 to reflect supported Virtex-II Device/Package Combinations.
08/01/03	2.0	All Virtex-II devices and speed grades now Production. See Table 13, Module 3.
03/29/04	2.0.1	Recompiled for backward compatibility with Acrobat 4 and above. No content changes.
06/24/04	3.3	Added references to available Pb-free wire-bond packages. (Revision number advanced to level of complete data sheet.)
03/01/05	3.4	*No changes in Module 1 for this revision.*
11/05/07	3.5	Updated copyright notice and legal disclaimer.

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules:

- Virtex-II Platform FPGAs: Introduction and Overview (Module 1)
- Virtex-II Platform FPGAs: Functional Description (Module 2)
- Virtex-II Platform FPGAs: DC and Switching Characteristics (Module 3)
- Virtex-II Platform FPGAs: Pinout Information (Module 4)

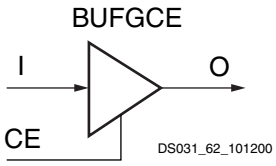


Figure 42: **Virtex-II BUFGCE Function**

If the CE input is inactive (Low) prior to the incoming rising clock edge, the following clock pulse does not pass through the clock buffer, and the output stays Low. Any level change of CE during the incoming clock High time has no effect. CE must not change during a short setup window just prior to the rising clock edge on the BUFGCE input I. Violating this setup time requirement can result in an undefined runt pulse output.

BUFGMUX

BUFGMUX can switch between two unrelated, even asynchronous clocks. Basically, a Low on S selects the I0 input, a High on S selects the I1 input. Switching from one clock to the other is done in such a way that the output High and Low time is never shorter than the shortest High or Low time of either input clock. As long as the presently selected clock is High, any level change of S has no effect .

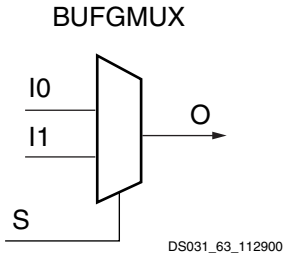


Figure 43: **Virtex-II BUFGMUX Function**

If the presently selected clock is Low while S changes, or if it goes Low after S has changed, the output is kept Low until the other ("to-be-selected") clock has made a transition from High to Low. At that instant, the new clock starts driving the output.

The two clock inputs can be asynchronous with regard to each other, and the S input can change at any time, except for a short setup time prior to the rising edge of the presently selected clock (I0 or I1). Violating this setup time requirement can result in an undefined runt pulse output.

All Virtex-II devices have 16 global clock multiplexer buffers.

Figure 44 shows a switchover from I0 to I1.

- The current clock is CLK0.
- S is activated High.
- If CLK0 is currently High, the multiplexer waits for CLK0 to go Low.
- Once CLK0 is Low, the multiplexer output stays Low until CLK1 transitions High to Low.
- When CLK1 transitions from High to Low, the output switches to CLK1.
- No glitches or short pulses can appear on the output.

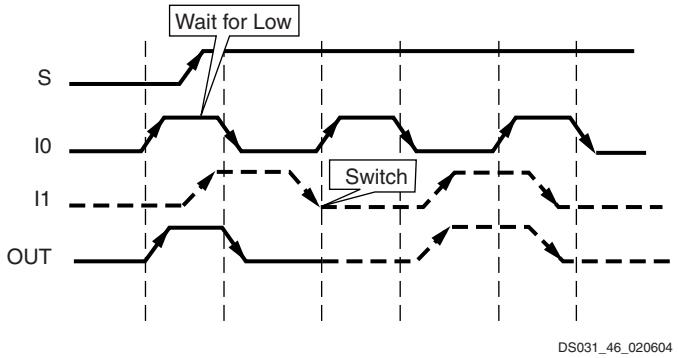


Figure 44: **Clock Multiplexer Waveform Diagram**

Local Clocking

In addition to global clocks, there are local clock resources in the Virtex-II devices. There are more than 72 local clocks in the Virtex-II family. These resources can be used for many different applications, including but not limited to memory interfaces. For example, even using only the left and right I/O banks, Virtex-II FPGAs can support up to 50 local clocks for DDR SDRAM. These interfaces can operate beyond 200 MHz on Virtex-II devices.

Digital Clock Manager (DCM)

The Virtex-II DCM offers a wide range of powerful clock management features.

- **Clock De-skew**: The DCM generates new system clocks (either internally or externally to the FPGA), which are phase-aligned to the input clock, thus eliminating clock distribution delays.
- **Frequency Synthesis**: The DCM generates a wide range of output clock frequencies, performing very flexible clock multiplication and division.
- **Phase Shifting**: The DCM provides both coarse phase shifting and fine-grained phase shifting with dynamic phase shift control.

The DCM utilizes fully digital delay lines allowing robust high-precision control of clock phase and frequency. It also utilizes fully digital feedback systems, operating dynamically to compensate for temperature and voltage variations during operation.

Up to four of the nine DCM clock outputs can drive inputs to global clock buffers or global clock multiplexer buffers simultaneously (see Figure 45). All DCM clock outputs can simultaneously drive general routing resources, including routes to output buffers.

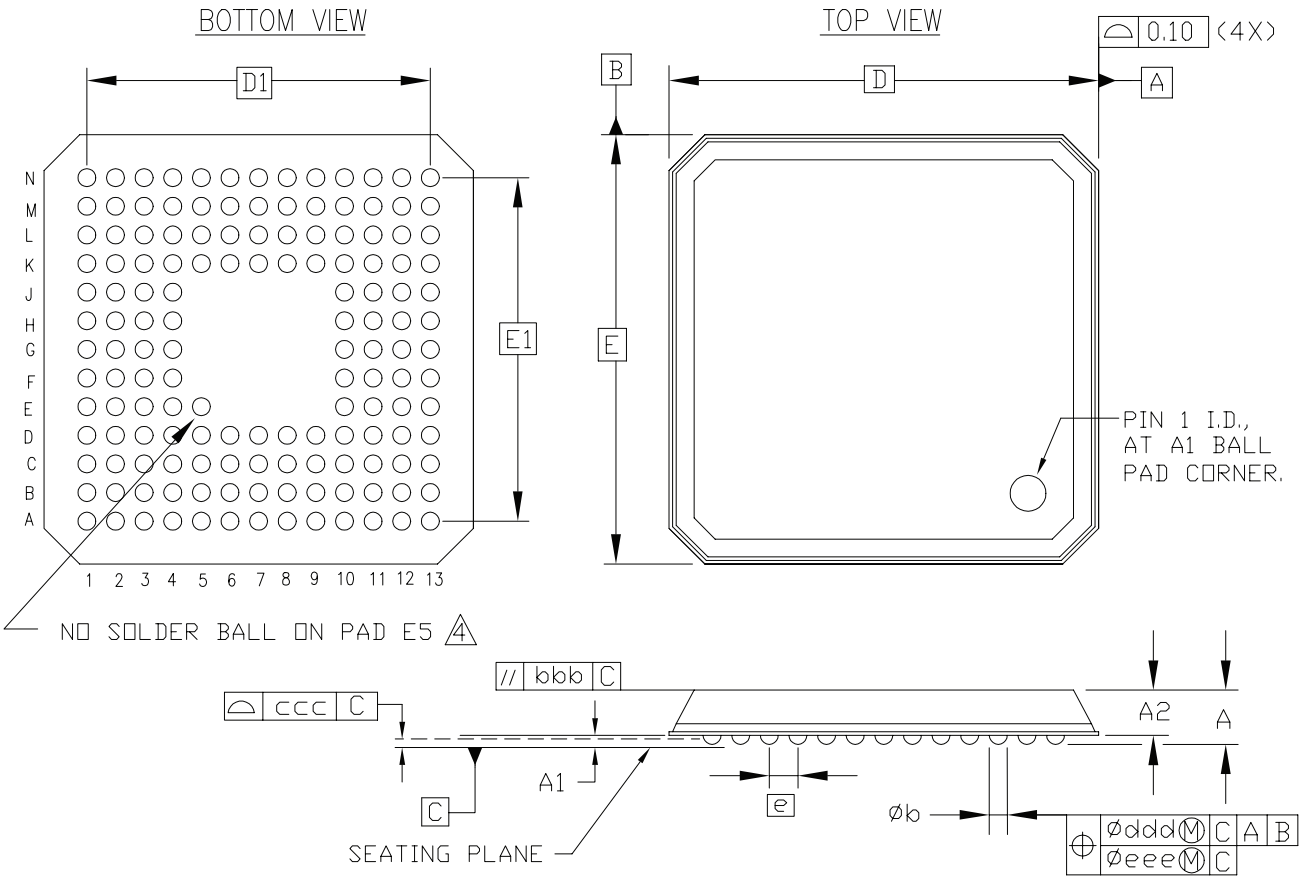
Table 27: **Enhanced Pipelined Multiplier Switching Characteristics**

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
Setup and Hold Times Before/After Clock					
Data Inputs	$T_{MULIDCK}/T_{MULCKID}$	3.00/0.00	3.45/0.00	3.89/0.00	ns, Max
Clock Enable	$T_{MULIDCK\_CE}/T_{MULCKID\_CE}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Reset	$T_{MULIDCK\_RST}/T_{MULCKID\_RST}$	0.72/0.00	0.80/0.00	0.86/0.00	ns, Max
Clock to Output Pin					
Clock to Pin 35	$T_{MULTCK1\_P35}$	3.05	3.25	3.74	ns, Max
Clock to Pin 34	$T_{MULTCK1\_P34}$	2.95	3.14	3.61	ns, Max
Clock to Pin 33	$T_{MULTCK1\_P33}$	2.85	3.04	3.49	ns, Max
Clock to Pin 32	$T_{MULTCK1\_P32}$	2.76	2.93	3.37	ns, Max
Clock to Pin 31	$T_{MULTCK1\_P31}$	2.66	2.82	3.25	ns, Max
Clock to Pin 30	$T_{MULTCK1\_P30}$	2.56	2.72	3.12	ns, Max
Clock to Pin 29	$T_{MULTCK1\_P29}$	2.47	2.61	3.00	ns, Max
Clock to Pin 28	$T_{MULTCK1\_P28}$	2.37	2.50	2.88	ns, Max
Clock to Pin 27	$T_{MULTCK1\_P27}$	2.27	2.40	2.75	ns, Max
Clock to Pin 26	$T_{MULTCK1\_P26}$	2.17	2.29	2.63	ns, Max
Clock to Pin 25	$T_{MULTCK1\_P25}$	2.08	2.18	2.51	ns, Max
Clock to Pin 24	$T_{MULTCK1\_P24}$	1.98	2.07	2.38	ns, Max
Clock to Pin 23	$T_{MULTCK1\_P23}$	1.88	1.97	2.26	ns, Max
Clock to Pin 22	$T_{MULTCK1\_P22}$	1.79	1.86	2.14	ns, Max
Clock to Pin 21	$T_{MULTCK1\_P21}$	1.69	1.75	2.02	ns, Max
Clock to Pin 20	$T_{MULTCK1\_P20}$	1.59	1.65	1.89	ns, Max
Clock to Pin 19	$T_{MULTCK1\_P19}$	1.50	1.54	1.77	ns, Max
Clock to Pin 18	$T_{MULTCK1\_P18}$	1.40	1.43	1.65	ns, Max
Clock to Pin 17	$T_{MULTCK1\_P17}$	1.30	1.33	1.52	ns, Max
Clock to Pin 16	$T_{MULTCK1\_P16}$	1.20	1.22	1.40	ns, Max
Clock to Pin 15	$T_{MULTCK1\_P15}$	1.11	1.11	1.28	ns, Max
Clock to Pin 14	$T_{MULTCK1\_P14}$	1.01	1.00	1.15	ns, Max
Clock to Pin 13	$T_{MULTCK1\_P13}$	0.91	1.00	1.15	ns, Max
Clock to Pin 12	$T_{MULTCK1\_P12}$	0.91	1.00	1.15	ns, Max
Clock to Pin 11	$T_{MULTCK1\_P11}$	0.91	1.00	1.15	ns, Max
Clock to Pin 10	$T_{MULTCK1\_P10}$	0.91	1.00	1.15	ns, Max
Clock to Pin 9	$T_{MULTCK1\_P9}$	0.91	1.00	1.15	ns, Max
Clock to Pin 8	$T_{MULTCK1\_P8}$	0.91	1.00	1.15	ns, Max
Clock to Pin 7	$T_{MULTCK1\_P7}$	0.91	1.00	1.15	ns, Max
Clock to Pin 6	$T_{MULTCK1\_P6}$	0.91	1.00	1.15	ns, Max
Clock to Pin 5	$T_{MULTCK1\_P5}$	0.91	1.00	1.15	ns, Max
Clock to Pin 4	$T_{MULTCK1\_P4}$	0.91	1.00	1.15	ns, Max
Clock to Pin 3	$T_{MULTCK1\_P3}$	0.91	1.00	1.15	ns, Max
Clock to Pin 2	$T_{MULTCK1\_P2}$	0.91	1.00	1.15	ns, Max
Clock to Pin 1	$T_{MULTCK1\_P1}$	0.91	1.00	1.15	ns, Max
Clock to Pin 0	$T_{MULTCK1\_P0}$	0.91	1.00	1.15	ns, Max

Table 5: **CS144/CSG144 — XC2V40, XC2V80, and XC2V250**

Bank	Pin Description	Pin Number	No Connect in the XC2V40
6	IO_L01P_6	L3	
6	IO_L01N_6	L2	
6	IO_L02P_6/VRN_6	L1	
6	IO_L02N_6/VRP_6	K3	
6	IO_L03P_6	K2	
6	IO_L03N_6/VREF_6	K1	
6	IO_L94P_6	J2	
6	IO_L94N_6	H4	
6	IO_L96P_6	H3	
6	IO_L96N_6	H1	
7	IO_L96P_7	G4	
7	IO_L96N_7	G3	
7	IO_L94P_7	G1	
7	IO_L94N_7	F1	
7	IO_L93P_7/VREF_7	F2	NC
7	IO_L93N_7	F4	NC
7	IO_L03P_7/VREF_7	E2	
7	IO_L03N_7	E3	
7	IO_L02P_7/VRN_7	E4	
7	IO_L02N_7/VRP_7	D1	
7	IO_L01P_7	D2	
7	IO_L01N_7	D3	
0	VCCO_0	B5	
0	VCCO_0	C3	
1	VCCO_1	A11	
1	VCCO_1	A9	
2	VCCO_2	F10	
2	VCCO_2	C12	
3	VCCO_3	L12	
3	VCCO_3	J12	
4	VCCO_4	M9	
4	VCCO_4	L11	
5	VCCO_5	N3	
5	VCCO_5	N5	
6	VCCO_6	J3	
6	VCCO_6	M1	
7	VCCO_7	D4	
7	VCCO_7	F3	

CS144/CSG144 Chip-Scale BGA Package Specifications (0.80mm pitch)



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	~	1.20
A_1	0.20	~	~
A_2	0.65	~	~
D/E	12.00 BSC		
D_1/E_1	9.60 BSC		
e	0.80 BSC		
øb	0.40	0.45	0.50
bbb	~	~	0.20
ccc	~	~	0.12
ddd	~	~	0.15
eee	~	~	0.08
M	13		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAG–2 (DEPOPULATED).
4. PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144–BALL CHIP SCALE BGA (CS144/CSG144)

Figure 1: **CS144/CSG144 Chip-Scale BGA Package Specifications**

FG256/FGG256 Fine-Pitch BGA Package

As shown in Table 6, XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000 Virtex-II devices are available in the FG256/FGG256 fine-pitch BGA package. The pins in the XC2V250, XC2V500, and XC2V1000 devices are same. The No Connect columns show pin differences for the XC2V40 and XC2V80 devices. Following this table are the FG256/FGG256 Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 6: **FG256/FGG256 BGA — XC2V40, XC2V80, XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V40	No Connect in XC2V80
0	IO_L01N_0	C4		
0	IO_L01P_0	B4		
0	IO_L02N_0	D5		
0	IO_L02P_0	C5		
0	IO_L03N_0/VRP_0	B5		
0	IO_L03P_0/VRN_0	A5		
0	IO_L04N_0/VREF_0	D6	NC	NC
0	IO_L04P_0	C6	NC	NC
0	IO_L05N_0	B6	NC	NC
0	IO_L05P_0	A6	NC	NC
0	IO_L92N_0	E6	NC	NC
0	IO_L92P_0	E7	NC	NC
0	IO_L93N_0	D7	NC	NC
0	IO_L93P_0	C7	NC	NC
0	IO_L94N_0/VREF_0	B7		
0	IO_L94P_0	A7		
0	IO_L95N_0/GCLK7P	D8		
0	IO_L95P_0/GCLK6S	C8		
0	IO_L96N_0/GCLK5P	B8		
0	IO_L96P_0/GCLK4S	A8		
1	IO_L96N_1/GCLK3P	A9		
1	IO_L96P_1/GCLK2S	B9		
1	IO_L95N_1/GCLK1P	C9		
1	IO_L95P_1/GCLK0S	D9		
1	IO_L94N_1	A10		
1	IO_L94P_1/VREF_1	B10		
1	IO_L93N_1	C10	NC	NC
1	IO_L93P_1	D10	NC	NC
1	IO_L92N_1	E10	NC	NC

Table 7: **FG456/FGG456 BGA — XC2V250, XC2V500, and XC2V1000**

Bank	Pin Description	Pin Number	No Connect in XC2V250	No Connect in XC2V500
2	IO_L45N_2	H19		
2	IO_L45P_2/VREF_2	H20		
2	IO_L46N_2	H21		
2	IO_L46P_2	H22		
2	IO_L48N_2	J17		
2	IO_L48P_2	J18		
2	IO_L49N_2	J19	NC	
2	IO_L49P_2	J20	NC	
2	IO_L51N_2	J21	NC	
2	IO_L51P_2/VREF_2	J22	NC	
2	IO_L52N_2	K17	NC	
2	IO_L52P_2	K18	NC	
2	IO_L54N_2	K19	NC	
2	IO_L54P_2	K20	NC	
2	IO_L91N_2	K21		
2	IO_L91P_2	K22		
2	IO_L93N_2	L17		
2	IO_L93P_2/VREF_2	L18		
2	IO_L94N_2	L19		
2	IO_L94P_2	L20		
2	IO_L96N_2	L21		
2	IO_L96P_2	L22		
3	IO_L96N_3	M21		
3	IO_L96P_3	M20		
3	IO_L94N_3	M19		
3	IO_L94P_3	M18		
3	IO_L93N_3/VREF_3	M17		
3	IO_L93P_3	N17		
3	IO_L91N_3	N22		
3	IO_L91P_3	N21		
3	IO_L54N_3	N20	NC	
3	IO_L54P_3	N19	NC	
3	IO_L52N_3	N18	NC	

Table 8: **FG676/FGG676 BGA — XC2V1500, XC2V2000, and XC2V3000**

Bank	Pin Description	Pin Number	No Connect in XC2V1500	No Connect in XC2V2000
1	IO_L19N_1	E20		
1	IO_L19P_1	F20		
1	IO_L06N_1	B21		
1	IO_L06P_1	B22		
1	IO_L05N_1	A22		
1	IO_L05P_1	A23		
1	IO_L04N_1	C21		
1	IO_L04P_1/VREF_1	D21		
1	IO_L03N_1/VRP_1	C20		
1	IO_L03P_1/VRN_1	D20		
1	IO_L02N_1	A24		
1	IO_L02P_1	A25		
1	IO_L01N_1	B23		
1	IO_L01P_1	B24		
2	IO_L01N_2	B26		
2	IO_L01P_2	C26		
2	IO_L02N_2/VRP_2	G20		
2	IO_L02P_2/VRN_2	H20		
2	IO_L03N_2	C25		
2	IO_L03P_2/VREF_2	D25		
2	IO_L04N_2	E23		
2	IO_L04P_2	E24		
2	IO_L06N_2	G21		
2	IO_L06P_2	G22		
2	IO_L19N_2	D26		
2	IO_L19P_2	E26		
2	IO_L21N_2	F23		
2	IO_L21P_2/VREF_2	F24		
2	IO_L22N_2	E25		
2	IO_L22P_2	F25		
2	IO_L24N_2	H22		
2	IO_L24P_2	H21		
2	IO_L25N_2	G23	NC	NC
2	IO_L25P_2	G24	NC	NC
2	IO_L43N_2	F26		
2	IO_L43P_2	G26		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
1	VCCO_1	B14		
2	VCCO_2	M16		
2	VCCO_2	L23		
2	VCCO_2	L19		
2	VCCO_2	L16		
2	VCCO_2	K16		
2	VCCO_2	F22		
3	VCCO_3	W22		
3	VCCO_3	R16		
3	VCCO_3	P23		
3	VCCO_3	P19		
3	VCCO_3	P16		
3	VCCO_3	N16		
4	VCCO_4	AC14		
4	VCCO_4	AB19		
4	VCCO_4	W14		
4	VCCO_4	T15		
4	VCCO_4	T14		
4	VCCO_4	T13		
5	VCCO_5	AC11		
5	VCCO_5	AB6		
5	VCCO_5	W11		
5	VCCO_5	T12		
5	VCCO_5	T11		
5	VCCO_5	T10		
6	VCCO_6	W3		
6	VCCO_6	R9		
6	VCCO_6	P9		
6	VCCO_6	P6		
6	VCCO_6	P2		
6	VCCO_6	N9		
7	VCCO_7	M9		
7	VCCO_7	L9		
7	VCCO_7	L6		
7	VCCO_7	L2		
7	VCCO_7	K9		

Table 9: **BG575/BGG575 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in XC2V1000	No Connect in XC2V1500
NA	GND	D15		
NA	GND	D10		
NA	GND	D4		
NA	GND	C22		
NA	GND	C3		
NA	GND	B24		
NA	GND	B23		
NA	GND	B2		
NA	GND	B1		
NA	GND	A24		
NA	GND	A23		
NA	GND	A18		
NA	GND	A7		
NA	GND	A2		

Notes:
1. See Table 4 for an explanation of the signals available on this pin.

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
2	IO_L19P_2	F26
2	IO_L21N_2	F27
2	IO_L21P_2/VREF_2	G27
2	IO_L22N_2	G23
2	IO_L22P_2	H23
2	IO_L24N_2	G25
2	IO_L24P_2	G26
2	IO_L25N_2	H21
2	IO_L25P_2	J21
2	IO_L27N_2	H22
2	IO_L27P_2/VREF_2	J22
2	IO_L28N_2	H24
2	IO_L28P_2	H25
2	IO_L30N_2	H27
2	IO_L30P_2	J27
2	IO_L43N_2	J23
2	IO_L43P_2	J24
2	IO_L45N_2	J25
2	IO_L45P_2/VREF_2	J26
2	IO_L46N_2	K20
2	IO_L46P_2	K21
2	IO_L48N_2	K22
2	IO_L48P_2	K23
2	IO_L49N_2	K24
2	IO_L49P_2	K25
2	IO_L51N_2	K26
2	IO_L51P_2/VREF_2	K27
2	IO_L52N_2	L20
2	IO_L52P_2	M20
2	IO_L54N_2	L21
2	IO_L54P_2	L22
2	IO_L67N_2	L24
2	IO_L67P_2	L25
2	IO_L69N_2	L26
2	IO_L69P_2/VREF_2	L27
2	IO_L70N_2	M19

Table 10: **BG728 BGA — XC2V3000**

Bank	Pin Description	Pin Number
6	IO_L52N_6	V3
6	IO_L54P_6	V2
6	IO_L54N_6	V1
6	IO_L67P_6	U8
6	IO_L67N_6	T8
6	IO_L69P_6	U6
6	IO_L69N_6/VREF_6	U7
6	IO_L70P_6	U4
6	IO_L70N_6	U3
6	IO_L72P_6	U2
6	IO_L72N_6	U1
6	IO_L73P_6	T9
6	IO_L73N_6	R9
6	IO_L75P_6	T5
6	IO_L75N_6/VREF_6	T6
6	IO_L76P_6	T4
6	IO_L76N_6	R4
6	IO_L78P_6	T2
6	IO_L78N_6	T1
6	IO_L91P_6	R7
6	IO_L91N_6	R8
6	IO_L93P_6	R5
6	IO_L93N_6/VREF_6	R6
6	IO_L94P_6	R3
6	IO_L94N_6	P3
6	IO_L96P_6	R2
6	IO_L96N_6	R1
7	IO_L96P_7	P5
7	IO_L96N_7	P6
7	IO_L94P_7	P7
7	IO_L94N_7	P8
7	IO_L93P_7/VREF_7	N1
7	IO_L93N_7	N2
7	IO_L91P_7	N3
7	IO_L91N_7	N4

FF896 Flip-Chip Fine-Pitch BGA Package

As shown in Table 11, XC2V1000, XC2V1500, and XC2V2000 Virtex-II devices are available in the FF896 flip-chip fine-pitch BGA package. Pins in the XC2V1000, XC2V1500, and XC2V2000 devices are the same, except for the pin differences in the XC2V1000 and XC2V1500 devices shown in the No Connect columns. Following this table are the FF896 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L01N_0	B27		
0	IO_L01P_0	A27		
0	IO_L02N_0	F24		
0	IO_L02P_0	E24		
0	IO_L03N_0/VRP_0	C26		
0	IO_L03P_0/VRN_0	C25		
0	IO_L04N_0/VREF_0	A26		
0	IO_L04P_0	A25		
0	IO_L05N_0	F23		
0	IO_L05P_0	F22		
0	IO_L06N_0	C24		
0	IO_L06P_0	D25		
0	IO_L19N_0	A24		
0	IO_L19P_0	B25		
0	IO_L20N_0	G22		
0	IO_L20P_0	G21		
0	IO_L21N_0	D24		
0	IO_L21P_0/VREF_0	D23		
0	IO_L22N_0	B23		
0	IO_L22P_0	B24		
0	IO_L23N_0	H21		
0	IO_L23P_0	H20		
0	IO_L24N_0	E22		
0	IO_L24P_0	E23		
0	IO_L49N_0	A22		
0	IO_L49P_0	B22		
0	IO_L50N_0	F21		
0	IO_L50P_0	F20		
0	IO_L51N_0	C23		
0	IO_L51P_0/VREF_0	C22		
0	IO_L52N_0	B20		
0	IO_L52P_0	B21		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L53N_0	G20		
0	IO_L53P_0	G19		
0	IO_L54N_0	D21		
0	IO_L54P_0	D22		
0	IO_L67N_0	E20	NC	
0	IO_L67P_0	E21	NC	
0	IO_L68N_0	H19	NC	
0	IO_L68P_0	H18	NC	
0	IO_L69N_0	D20	NC	
0	IO_L69P_0/VREF_0	D19	NC	
0	IO_L70N_0	A20	NC	
0	IO_L70P_0	A21	NC	
0	IO_L71N_0	F19	NC	
0	IO_L71P_0	F18	NC	
0	IO_L72N_0	C19	NC	
0	IO_L72P_0	C20	NC	
0	IO_L73N_0	B18	NC	NC
0	IO_L73P_0	B19	NC	NC
0	IO_L74N_0	G18	NC	NC
0	IO_L74P_0	H17	NC	NC
0	IO_L75N_0	E18	NC	NC
0	IO_L75P_0/VREF_0	D18	NC	NC
0	IO_L76N_0	A18	NC	NC
0	IO_L76P_0	A19	NC	NC
0	IO_L77N_0	J17	NC	NC
0	IO_L77P_0	J16	NC	NC
0	IO_L78N_0	E16	NC	NC
0	IO_L78P_0	E17	NC	NC
0	IO_L91N_0/VREF_0	B17		
0	IO_L91P_0	B16		
0	IO_L92N_0	F17		
0	IO_L92P_0	F16		
0	IO_L93N_0	D16		
0	IO_L93P_0	D17		
0	IO_L94N_0/VREF_0	A17		
0	IO_L94P_0	A16		
0	IO_L95N_0/GCLK7P	H16		

Table 11: **FF896 BGA — XC2V1000, XC2V1500, and XC2V2000**

Bank	Pin Description	Pin Number	No Connect in the XC2V1000	No Connect in the XC2V1500
0	IO_L95P_0/GCLK6S	G16		
0	IO_L96N_0/GCLK5P	C17		
0	IO_L96P_0/GCLK4S	C16		
1	IO_L96N_1/GCLK3P	C15		
1	IO_L96P_1/GCLK2S	C14		
1	IO_L95N_1/GCLK1P	F15		
1	IO_L95P_1/GCLK0S	F14		
1	IO_L94N_1	B15		
1	IO_L94P_1/VREF_1	B14		
1	IO_L93N_1	D14		
1	IO_L93P_1	D15		
1	IO_L92N_1	G15		
1	IO_L92P_1	H15		
1	IO_L91N_1	A14		
1	IO_L91P_1/VREF_1	A13		
1	IO_L78N_1	E14	NC	NC
1	IO_L78P_1	E15	NC	NC
1	IO_L77N_1	J15	NC	NC
1	IO_L77P_1	J14	NC	NC
1	IO_L76N_1	B12	NC	NC
1	IO_L76P_1	B13	NC	NC
1	IO_L75N_1/VREF_1	D13	NC	NC
1	IO_L75P_1	E13	NC	NC
1	IO_L74N_1	H14	NC	NC
1	IO_L74P_1	H13	NC	NC
1	IO_L73N_1	A11	NC	NC
1	IO_L73P_1	A12	NC	NC
1	IO_L72N_1	C11	NC	
1	IO_L72P_1	C12	NC	
1	IO_L71N_1	F13	NC	
1	IO_L71P_1	F12	NC	
1	IO_L70N_1	B10	NC	
1	IO_L70P_1	B11	NC	
1	IO_L69N_1/VREF_1	D12	NC	
1	IO_L69P_1	D11	NC	
1	IO_L68N_1	G13	NC	

device shown in the No Connect column. Following this table are the FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00mm pitch).

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
0	IO_L01N_0	D29	
0	IO_L01P_0	C29	
0	IO_L02N_0	H26	
0	IO_L02P_0	G26	
0	IO_L03N_0/VRP_0	E28	
0	IO_L03P_0/VRN_0	E27	
0	IO_L04N_0/VREF_0	F25	
0	IO_L04P_0	F26	
0	IO_L05N_0	H25	
0	IO_L05P_0	H24	
0	IO_L06N_0	E26	
0	IO_L06P_0	F27	
0	IO_L19N_0	B32	
0	IO_L19P_0	C33	
0	IO_L20N_0	J24	
0	IO_L20P_0	J23	
0	IO_L21N_0	C27	
0	IO_L21P_0/VREF_0	C28	
0	IO_L22N_0	B30	
0	IO_L22P_0	B31	
0	IO_L23N_0	K23	
0	IO_L23P_0	K22	
0	IO_L24N_0	C26	
0	IO_L24P_0	D27	
0	IO_L25N_0	A30	
0	IO_L25P_0	A31	
0	IO_L26N_0	G24	
0	IO_L26P_0	G25	
0	IO_L27N_0	E25	
0	IO_L27P_0/VREF_0	E24	
0	IO_L28N_0	D25	
0	IO_L28P_0	D26	
0	IO_L29N_0	H23	
0	IO_L29P_0	H22	

Table 12: **FF1152 BGA — XC2V3000, XC2V4000, XC2V6000, and XC2V8000**

Bank	Pin Description	Pin Number	No Connect in the XC2V3000
7	IO_L75N_7	R28	
7	IO_L74P_7	R26	
7	IO_L74N_7	P26	
7	IO_L73P_7	N31	
7	IO_L73N_7	P31	
7	IO_L72P_7	N30	
7	IO_L72N_7	P30	
7	IO_L71P_7	R25	
7	IO_L71N_7	P25	
7	IO_L70P_7	L34	
7	IO_L70N_7	M34	
7	IO_L69P_7/VREF_7	P29	
7	IO_L69N_7	N29	
7	IO_L68P_7	P27	
7	IO_L68N_7	N27	
7	IO_L67P_7	L32	
7	IO_L67N_7	M32	
7	IO_L54P_7	L31	
7	IO_L54N_7	M31	
7	IO_L53P_7	K29	
7	IO_L53N_7	L30	
7	IO_L52P_7	L33	
7	IO_L52N_7	M33	
7	IO_L51P_7/VREF_7	M29	
7	IO_L51N_7	L29	
7	IO_L50P_7	M28	
7	IO_L50N_7	N28	
7	IO_L49P_7	K30	
7	IO_L49N_7	K31	
7	IO_L48P_7	H32	
7	IO_L48N_7	J32	
7	IO_L47P_7	N26	
7	IO_L47N_7	M26	
7	IO_L46P_7	J33	
7	IO_L46N_7	K33	
7	IO_L45P_7/VREF_7	H33	

Notice of Disclaimer

Virtex-II Data Sheet

The Virtex-II Data Sheet contains the following modules: